

## **Apple**



Rev. 6-5-23



## Computer Org & ASSEMBLY Programming



## **Apple SoC**

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drjeffsoftware.com/classroom.html



email ⇒ jeffrey.drobman@csun.edu



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## Section



Early
Apple
Computers



## Original Apple I







## Apple I Computer





Robert Mudry, Retired Silicon Valley engineering geek.

Shared Feb 6

#### A Hand-Built, Original Apple 1 Computer Is Yours for Just 1.5 Million Dollars





## Early PC's



Commodore PET



The Commodore PET 2001-8 alongside its rivals, the Apple II and the TRS-80 Model I

5



## 6502 8-bit MPU

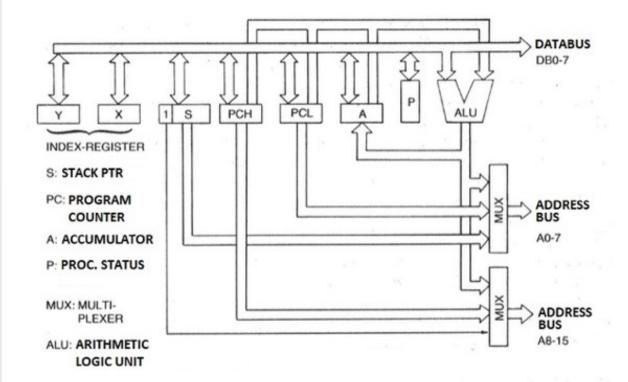


COMP122

Apple II in 1977 CISC

#### Other than ALU, what are the basic components of a CPU?

Most of the answers are for more complicated CPUs, with caches, pipelines, DMA etc. But the basic components for a working CPU are much fewer. The 8-bit 6502 microprocessor, introduced in 1975 and used in the Apple ][ computer and other early personal computers, had only 3510 transistors (compared to the many billions in today's CPUs). Its basic block diagram was fairly simple and easy to understand:



Not shown is the Instruction Register (IR) and decoder logic, which holds the instruction being executed which was fetched from memory.



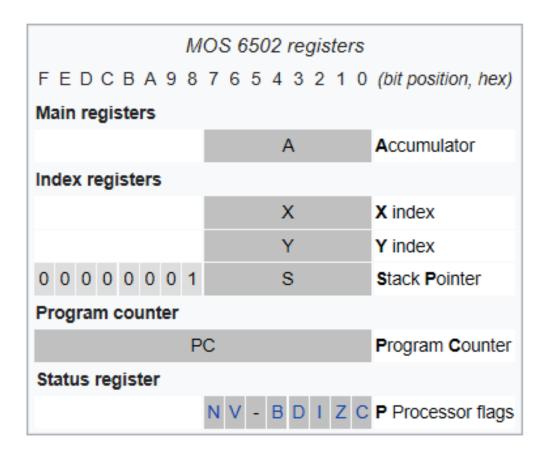
## 6502 8-bit MPU



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CISC Apple II in 1977 —

The 6502 had one 8-bit accumulator, and two 8-bit index registers, 8-bit stack pointer, and a 16-bit program counter so it could address a maximum of 65536 bytes.



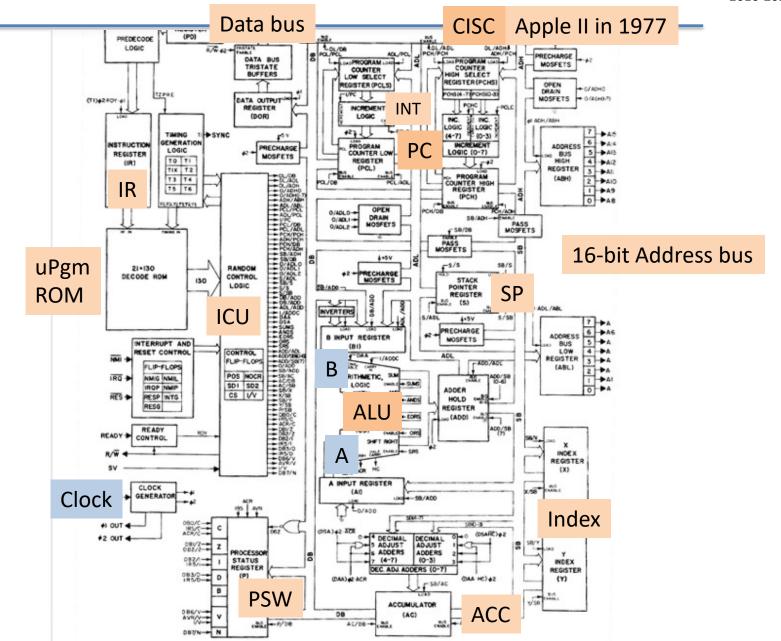
The high byte of the stack address is hardwired to 1, so stack addresses ranged from 0x1FF (initial value) to 0x100.



## 6502 8-bit MPU



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## Section



## **Apple**



## **Apple**



1984

**Steve Jobs** 

#### The MacIntosh



Wozniak

CPU: M68000

(16-bit)

RAM: 1MB





#### AAPL



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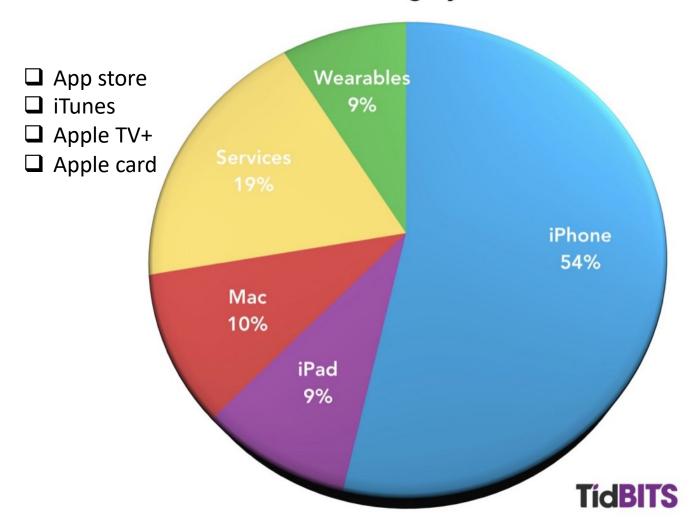




## **Apple Segments**



#### **Q2 2021 Category Revenue**





## Section



# Apple Events

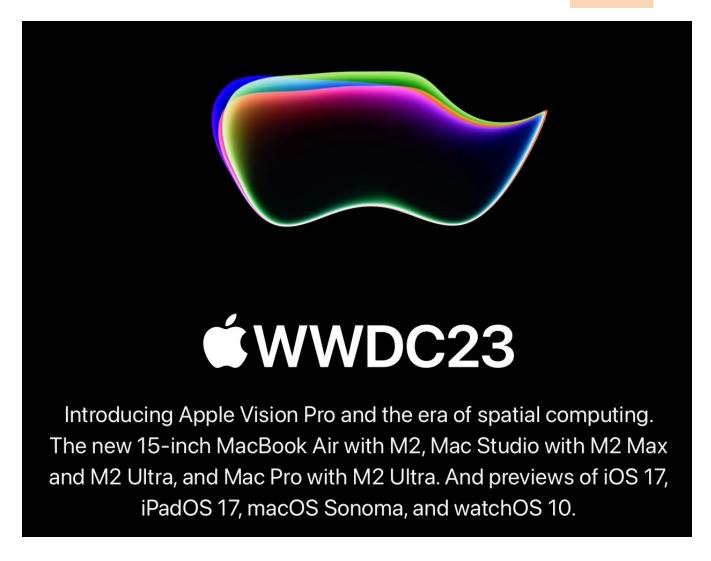




## Apple M2 Event



6-5-23





## Apple M2 Event



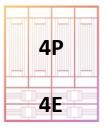
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### 12x faster

Up to

than fastest Intel-based MacBook Air



8-core

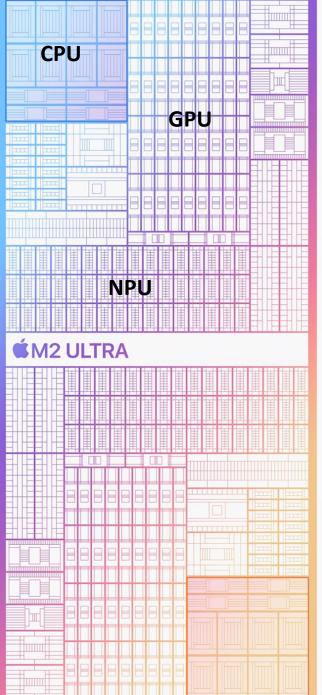


10-core









## M2 Event



6-5-23

- ❖ Each die (x2)
  - 12 **CPU** cores (8P+4E)
  - 38 **CPU** cores
  - 16 **NPU** cores
  - 67B transistors

#### M2 *Ultra* = 2x M2 *Max*









6-5-23



24-core CPU



Up to 76-core **GPU** 

Up to

20% faster CPU

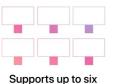
Up to

30% faster **GPU** 

Up to

192**GB** 

unified memory



**Pro Display XDRs** 



transistors



Second-generation

5 nm technology

32-core **Neural Engine** 

31.6 trillion operations per second



encode and decode

800GB/s

Memory bandwidth

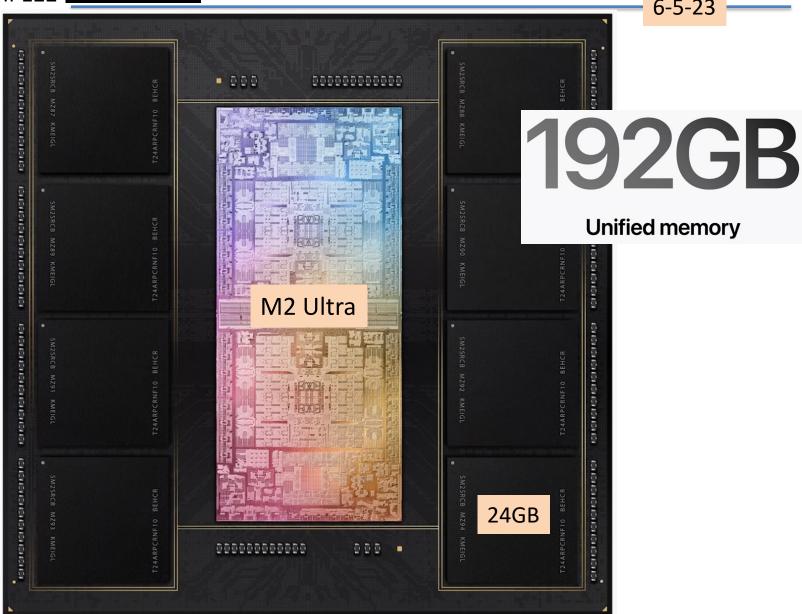


UltraFusion architecture





6-5-23









6-5-23



24-core 76-core

**CPU** 

Up to

3x faster

than fastest Intel-based Mac Pro Up to

**GPU** 

Up to

7x faster

than starting config of Intel-based Mac Pro

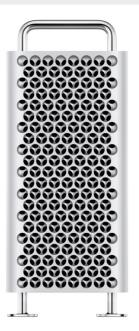
32-core

**Neural Engine** 

31.6 trillion operations per second



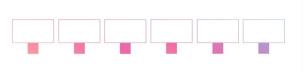








Bluetooth 5.3



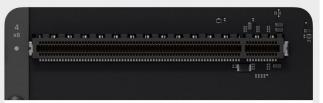
Supports up to six Pro Display XDRs



192**GB** 

Up to

unified memory



Six open PCle gen 4 slots



Rack mount available

streams

Up to

of 8K ProRes









## Apple Events Apple M2 Event: R1 COMP122 GWWDC23



6-5-23



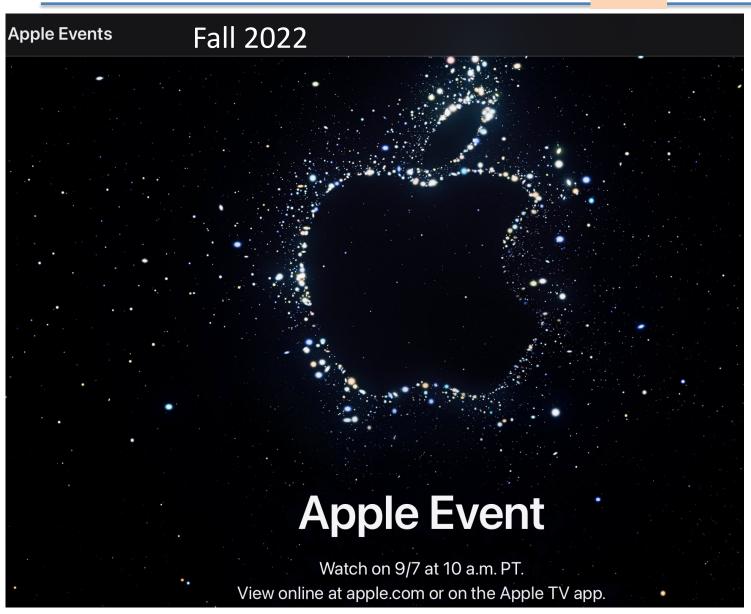
Vision Pro





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9-7-22







9-7-22



## **Apple Event**

Watch on 9/7 at 10 a.m. PT. View online at apple.com or on the Apple TV app.







9-7-22









9-7-22







































Five new colors



All you need is iPhone

Ceramic Shield

All-day battery life

5-core GPU





9-7-22

**Emergency SOS** 

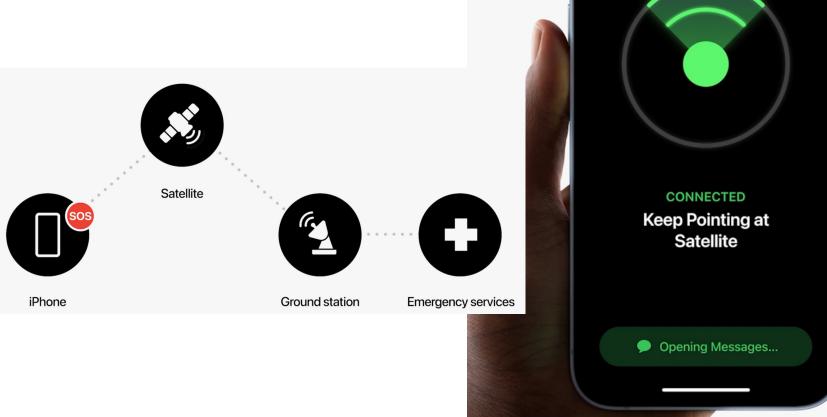
9:41

SOS 💉 🗀

End

## **Emergency SOS**

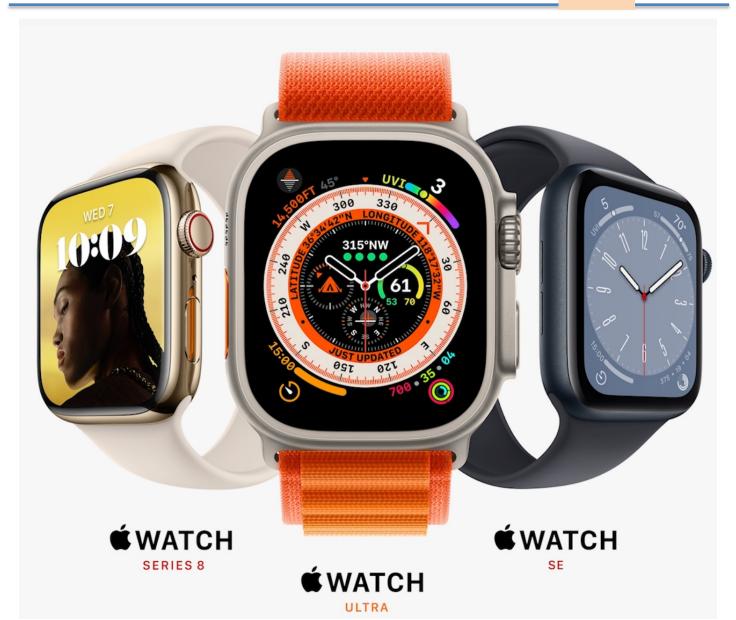
via satellite







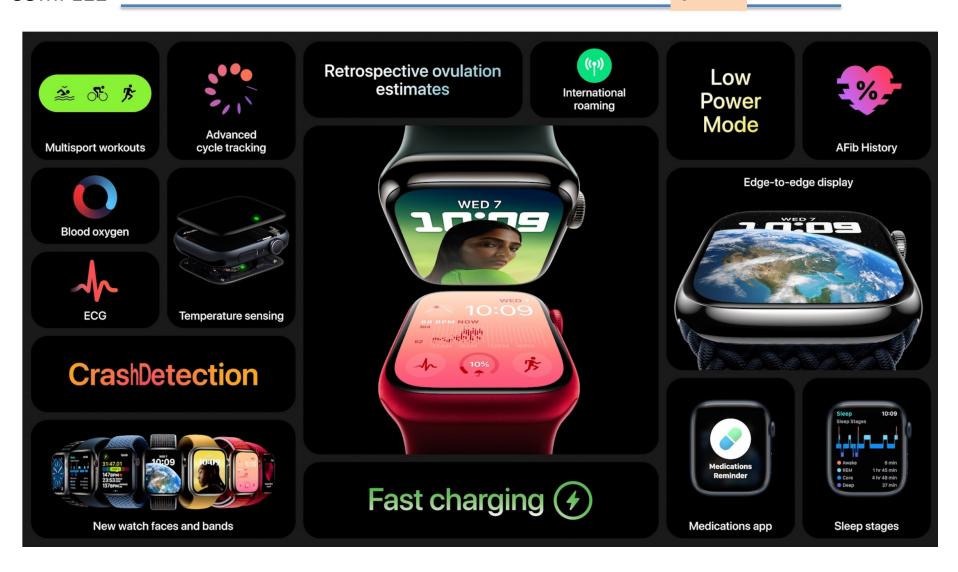
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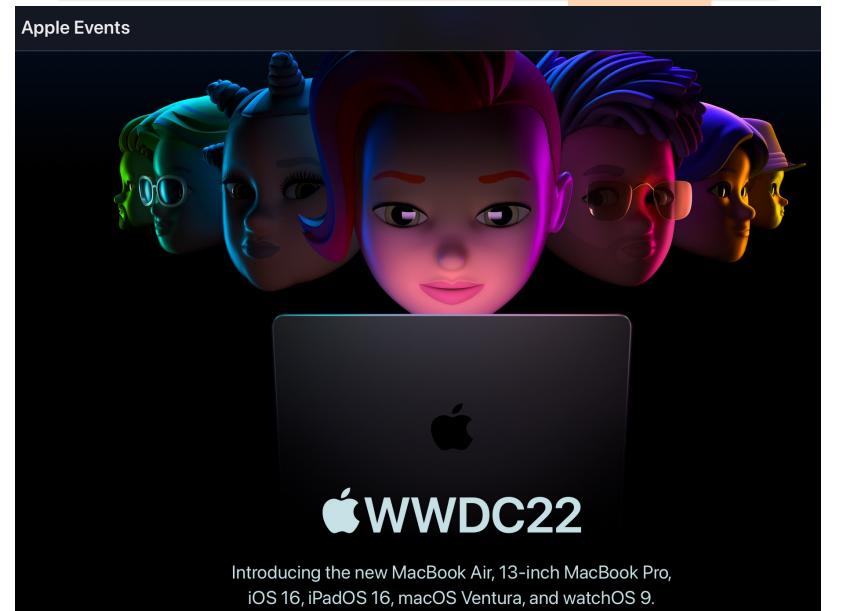


## WWDC Apple Event



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June 6, 2022





## New Apple Event



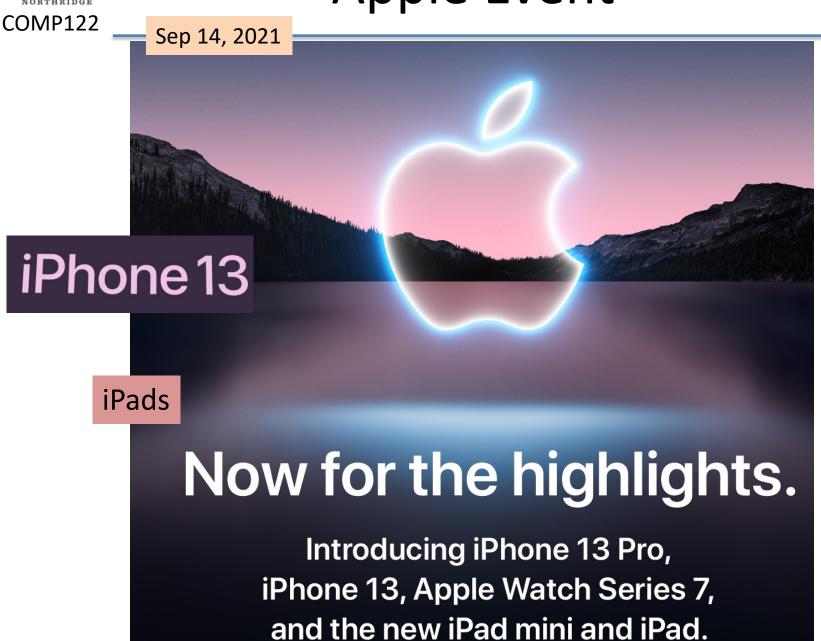
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March 8, 2022







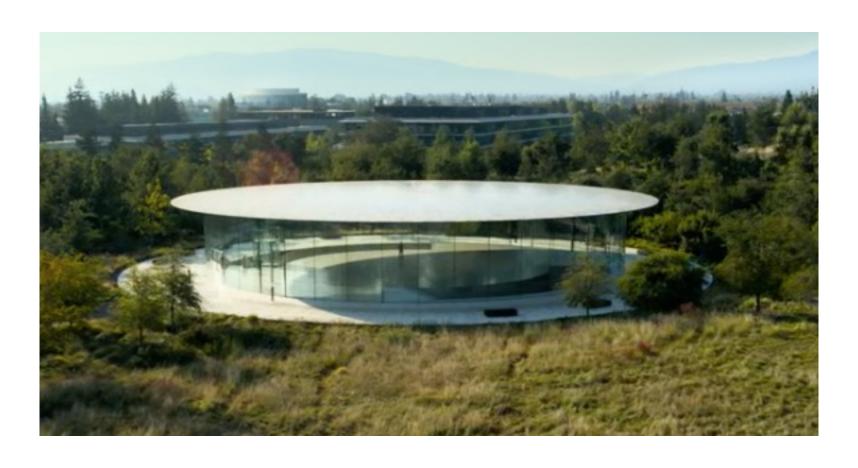




## **Apple Buildings**



— October 13, 2020 -





## **Apple Buildings**



COMP122

October 13, 2020 -





## Section



# Apple Phones



## ARM Chips (SoC)



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Quora



#### Joe Zbiciak

Developed practical algorithms actually used in production. • 6mo

#### Who makes the ARM processor?

Just about everybody but ARM.

ARM develops the architecture, and develops its own RTL implementations.

But outside of a handful of test chips, ARM does not manufacture any of the volume production ARM products out there.

All the production architecture, and develops its own RTL implementations.

But outside of a handful of test chips, ARM does not manufacture any of the volume production ARM products out there.

I know of a few custom microarchitectures that implement the ARM ISA other than Apple.

- Fujitsu A64FX ☑
- Cavium Vulcan ☑
- Ampere Siryn. ☑
- Marvell ThunderX3 
   ☐ (canceled)
- AppliedMicro Storm, ☐ Shadowcat, ☐ and Skylark ☐

All the production ARM processors come from:

- Apple
- Samsung
- Qualcomm
- Amazon
- Texas Instruments
- Microchip
- NXP / Freescale
- ST Microelectronics
- Broadcom
- AMD • Intel®

- Google
- Tesla

...and many more.



#### 1<sup>st</sup> iPhone



## **iPhone**

ANNOUNCED: Jan. 9, 2007

RELEASED: June 29, 2007

#### **KEY FEATURES:**

3.5-inch diagonal screen; 320 x 480 pixels at 163 ppi; 2-megapixel camera

PRICE: 4GB model, \$499; 8GB version, \$599 (with a two-year contract)





#### Apple Event: iPhone 14



9-7-22







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9-7-22

#### iPhone 14



Two great sizes: 6.1" and new, larger 6.7" Super Retina XDR displays.



Our best battery life ever on iPhone 14 Plus. And all-day battery life on iPhone 14.4



Dynamic Island, a magical new way to interact with your iPhone.



iPhone 14 Pro

Always-On display — the info you want, at a glance.



Emergency SOS via satellite<sup>2</sup> and Crash Detection<sup>3</sup> for help when you need it most.



Industry-leading durability features like Ceramic Shield and water resistance.<sup>6</sup>



Emergency SOS via satellite<sup>2</sup> and Crash Detection<sup>3</sup> for help when you need it most.



Amazing all-day battery life, even with so many new capabilities.<sup>4</sup>



Advanced dual-camera system for more detailed, colorful shots. Sharper selfies.



Action mode takes smooth handheld videos when you're on the move.



Pro camera system with 48MP Main camera. Four zoom options. Sharper selfies.



Action mode takes smooth handheld videos when you're on the move.



Superspeedy A15 Bionic chip with 5-core GPU.



5G cellular for superfast streaming, gaming, downloading, and more.<sup>5</sup>

A16

A16 Bionic — the ultimate smartphone chip.



5G cellular for superfast streaming, gaming, downloading, and more.<sup>5</sup>





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#### **Apple**



**COMP122** October 13, 2020

- ❖iPhone 12
  - **□** 5G
    - 2x peak data rate
  - ☐ Camera (4)
  - Mag interface
  - **□** Colors (5)













#### iPhone 12







iPhone From



iPhone X® From \$499



iPhone 11
From
\$500



iPhone 12 From \$699



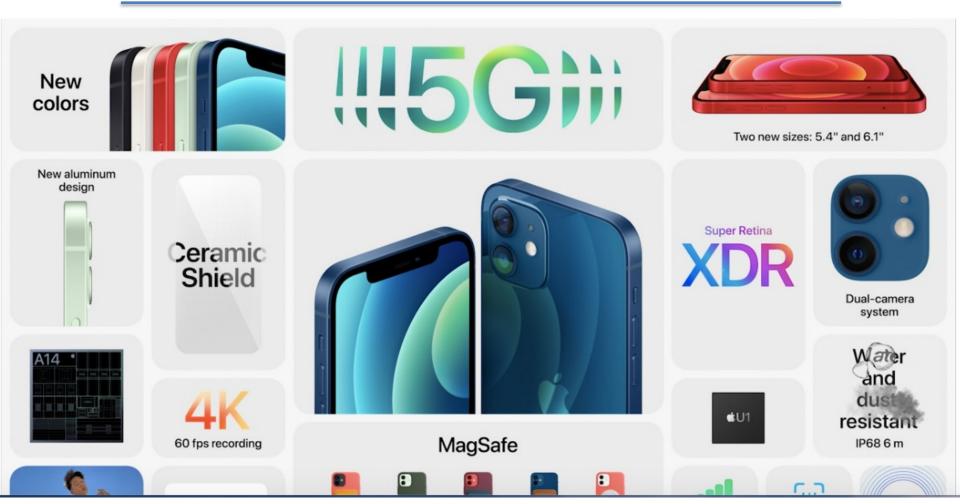
iPhone 12 Pro From \$999



#### iPhone 12



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#### iPhone 12











#### Section



# Apple iPads





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Sep 14, 2021











## Find the right iPad for you.

Compare iPad models >



iPad Pro

The ultimate iPad experience.

From \$799





Available in October

#### iPad Air

Powerful. Colorful. Wonderful.

From \$599





New

#### **iPad**

Delightfully capable. Surprisingly affordable.

From \$329





iPad mini

Small in size. Big on capability.

From \$399









The new



The new iPad is more capable than ever.

Now with the faster A12 Bionic chip,
support or Apple Pencil, and the
amazing features of iPadOS 14.









Available in October

iPad Air features an all-screen design with a 10.9-inch Liquid Retina display. The new A14 Bionic chip. And support for Apple Pencil and Magic Keyboard. Available in five finishes.





#### Chip

40% FASTER CPU PERFORMANCE

30% FASTER GRAPHICS



A14 Bionic chip with 64-bit architecture

**Neural Engine** 

A14 Bionic chip featuring 40% faster CPU, 30% faster graphics, and 2x faster machine learning with nextgeneration Neural Engine.<sup>5</sup>

10x FASTER

MACHINE LEARNING

#### Camera

12MP Wide camera

f/1.8 aperture

Five-element lens

Hybrid IR filter

60% FASTER LTE

Backside illumination sensor

Live Photos with stabilization

Autofocus with Focus Pixels

Tap to focus with Focus Pixels

Wide color capture for photos and Live Photos

Panorama (up to 63MP)

Exposure control









Available in October

iPad Air

Location

All models

Digital compass

Wi-Fi

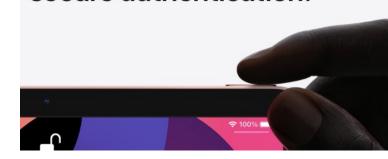
iBeacon microlocation

Wi-Fi + Cellular models

Built-in GPS/GNSS

Cellular

Touch ID integrated into the top button for fast, easy, and secure authentication.



Sensors

Touch ID

Three-axis gyro

Accelerometer

Barometer

Ambient light sensor

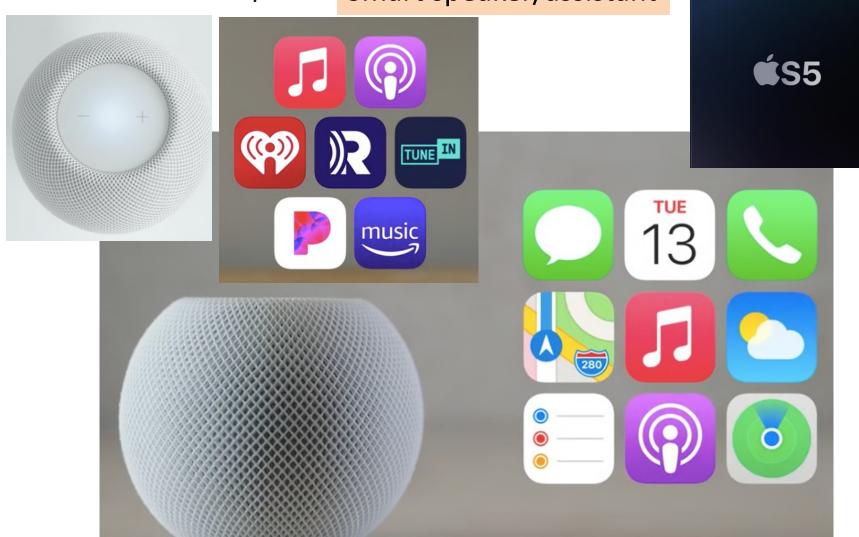


### **Apple Mini**



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October 13, 2020 - Smart speaker/assistant



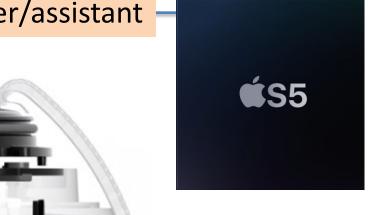


#### **Apple Mini**



COMP122

October 13, 2020 - Smart speaker/assistant





Amazing sound Intelligent assistant **Smart home** Privacy and security



#### Section









November 10, 2020







June 6, 2022

#### **New MacBooks**



MacBook Air

**€**M1

From

\$999

**M1** 



MacBook Air

**€**M2

From

\$1199

**M2** 

Education discount = \$100



MacBook Pro

**€**M2

From

\$1299

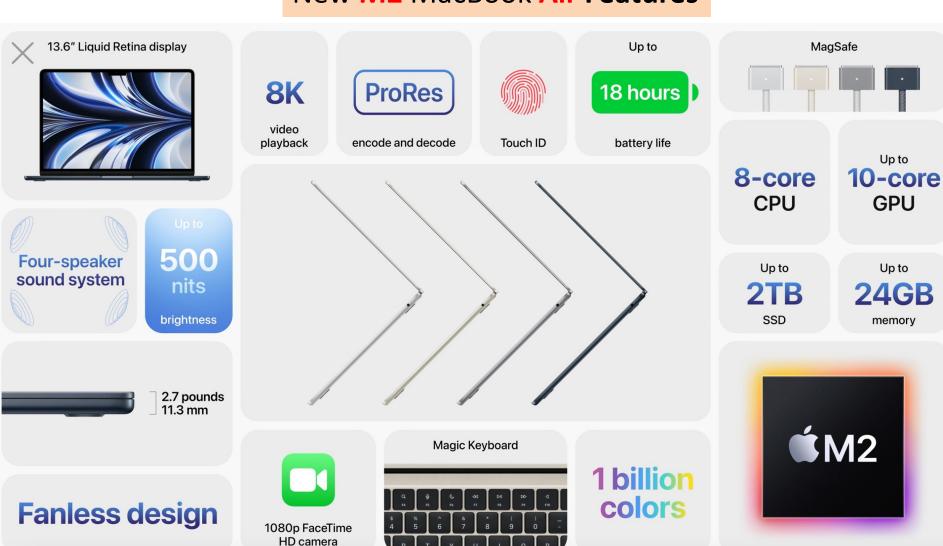
**M2** 





June 6, 2022

#### New M2 MacBook Air Features

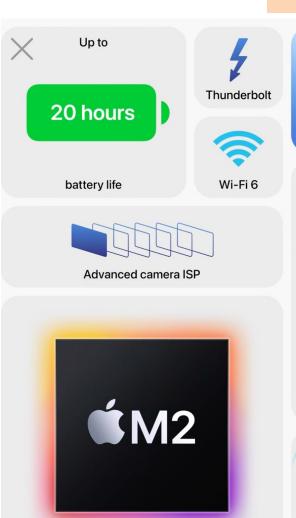






June 6, 2022

#### New M2 MacBook Pro Features















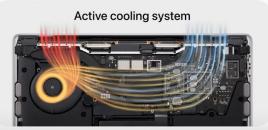
















June 6, 2022

New M2 MacBook Performance

#### Gaming performance

39% faster

MacBook Pro 13" 8th-gen Core i7

3.3x faster



## New Apple Event



March 8, 2022

New Mac Lineup





#### Mac Studio

€ M1 Ultra64GB unified memory1TB SSD

Starting at

\$3999

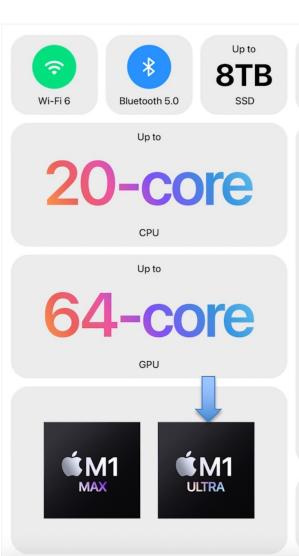


#### New Apple Event



March 8, 2022

#### **New Mac Studio**











November 10, 2020 Thunderbolt controller **CPU** DDR4 memory Apple T2 I/O chip





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COMP122

November 10, 2020





#### Section



## Apple Chips

A-series (ARM v8)



#### Apple's ARM License



#### Apple's ARM license is beyond architectural?

it look like Apple is allowed to add **proprietary ISA extensions** -- as long as they are ARM ISA compatible.

And apparently in Apple's case, they get to be a little bit incompatible (no **nVHE** mode, crazy **custom ISA extensions**, ...) Which is also obvious proof that they're their own designs, because literally nobody else could or would implement the same Apple-proprietary ISA extensions. Here, we use some of the custom instructions in **m1n1** 

Nope, you need to be compatible with the **architecture specification**, and it lays out exactly what can be implementation defined and what can't. E.g. you're allowed some freedom in what features to implement (Apple doesn't implement **EL3** and this is fine), and you can add implementation defined system **registers** (Apple has a huge number of them, e.g. to implement TSO for **Rosetta**). But you can't decide not to support **mandatory features** (Apple forces on **VHE mode**, which is not legal - VHE is optional, non-VHE mode isn't), nor can you add **extensions** to the core ISA. Apple added **AMX**, memory compression/decompression, a variant of the AT instructions that outputs to a GPR, and the whole **Guarded Execution** feature (two new parallel **exception levels** and machinery to call to/from them and lock down things to them), and possibly more, all of them in **reserved instruction encoding space**.



#### New Apple A16



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\_Quora

Why did Apple's mobile processor speed growth become slower compared to their early processor which usually doubled the performance compared to its previous generation?



**Jeff Drobman** 

Lecturer at California State University, Northridge (2016-present) · Just now

the new A16 is the 1st Apple chip to use the latest 4nm process from TSMC. that allows more transistors on the same size die. but Apple chose to use the same number of CPU and GPU cores as for the A15 SoC, and instead uses the extra transistors for other functions like media and Al/ML. so we won't see much difference in benchmarked performance vs the A15. Apple shows a performance improvement vs their A13 chip.







9-7-22

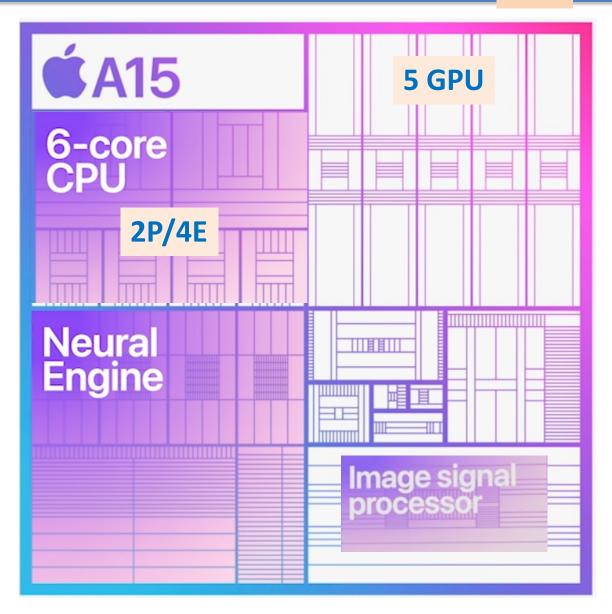








9-7-22









9-7-22

## **CPU performance A16 Bionic 2022 A13 Bionic** 2019 Nearest competitor 2022



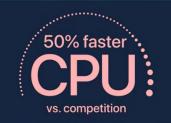




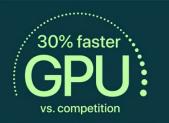
Sep 14, 2021

iPhone 13





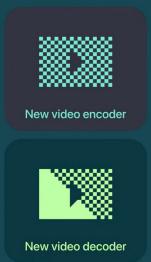




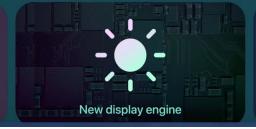
















WIILUI





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Sep 14, 2021

iPhone 13



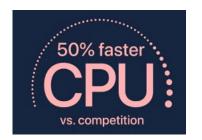
## 6-core CPU

2 high-performance cores 4 high-efficiency cores

4-core GPU

16-core Neural Engine







# New Apple A14/iPads









A14 Bionic-

October 13, 2020



5 nm

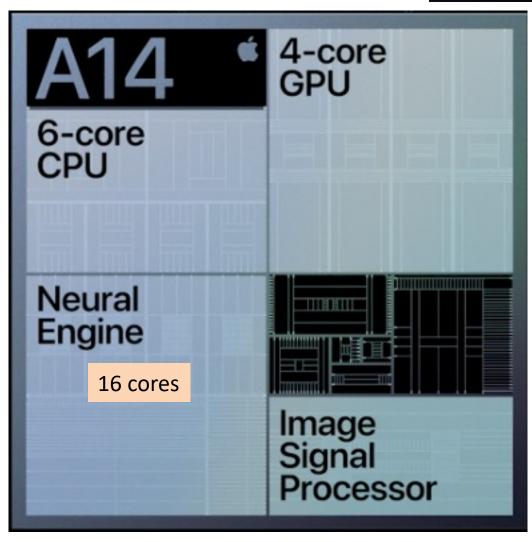




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- October 13, 2020



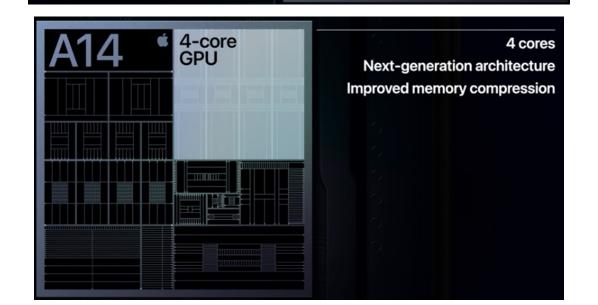






- October 13, 2020

2 high-performance cores
4 high-efficiency cores
Next-generation architecture



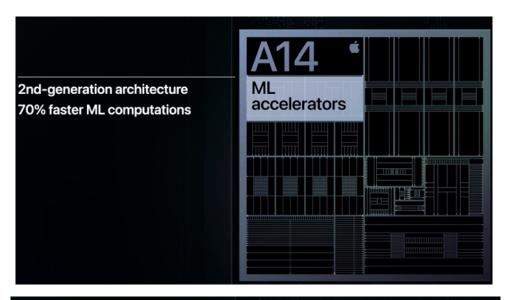




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— October 13, 2020







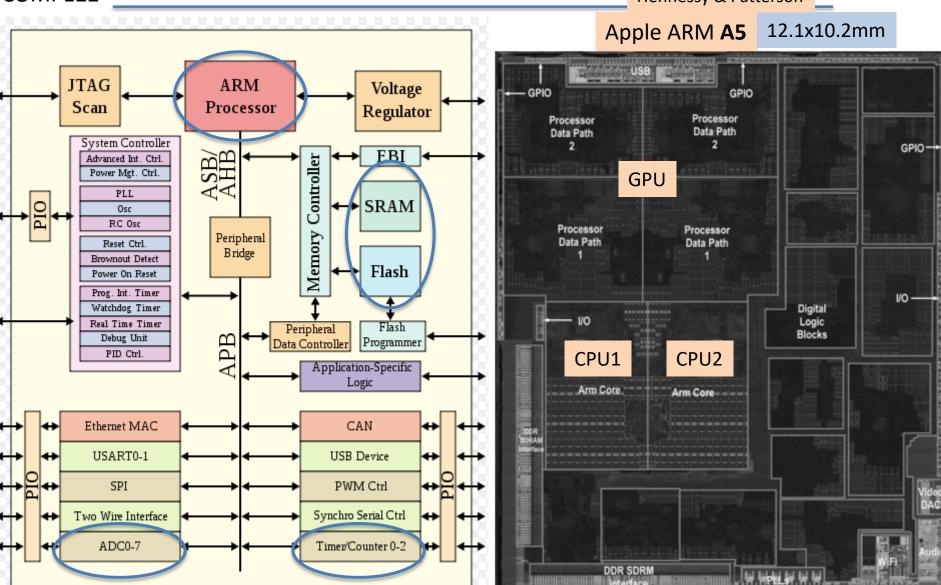


### ARM SoC/A5



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Hennessy & Patterson





### Apple ARM SoC



**COMP122** 

#### Apple ARM SoC

the first ARM designs were for LOW POWER for portable devices. to achieve low power, the CPU was designed as simple RISC ISA and low clock frequency. Apple iPhones have used ARM from day 1, since they too initially didn't need high compute performance. over time, ARM models have evolved into more powerful models, including a 64-bit ISA -- necessary for today's computers. so now the time has come to start switching to ARM, mainly due to ARM being a licensable ISA and core that can be designed into anyone's SoC like Apple and many others do. I also note that the ARM ISA has evolved from a simple RISC to a more complex, CISC-like one.

Apple has just announced they will replace x86 CPU's on their **Macs** with their own ARM-based **A13** (or next generation A14/15). makes sense for them to use their own chips now that they are powerful enough. this will also give Apple the same **AI** performance capabilities across all their hardware devices (e.g., Siri) -- way more AI power than any x86 chips.

The reason -- historically: Apple has upgraded their Macs for the same reason any company does: to be competitive they have to use a top performance CPU. so Apple switched from the 6502 (Apple II) to the M68000 in the 1st Mac, then upgraded to the Mot PPC. but then Mot stopped making PPC's, so Apple had nowhere else to go but x86 (Intel or AMD) – for Macs. note they have been making their own custom ARM-based chips (A series) for their phones.

Apple has long made their own chips with ARM CPU's since 2007 in their iPhones, designing an ever more powerful SoC (A4-A13). These new **A13** SoC's are now much better than the Intel x86 chips in overall performance -- including machine learning (ML) via on-chip GPU cores plus neural engine -- and with superior power management.



# Apple A1-5



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MP122								2007-10			
Name	Model no.	Image	Semiconductor technology	Die size	Transistor count	CPU ISA	CPU	CPU cache	GPU		
	APL0098	33950030 ARM 8900B 0719 N004BZ02 K4X18153PC-X8C3 ECC45803 716	90 nm <sup>[9]</sup>	72 mm <sup>2[6]</sup>		ARMv6	412 MHz single-core ARM11	L1i: 16 KB L1d: 16 KB	PowerVR MBX Lite @ 103 MHz		
	APL0278	33950048 ARM K4X16323PD-R6C4 6H0050A3 831 APL0278A0 N18420A1 0834	65 nm <sup>[6]</sup>	36 mm <sup>2[6]</sup>		ARMv6	412–533 MHz single-core ARM11	L1i: 16 KB L1d: 16 KB	PowerVR MBX Lite @ 133 MHz		
	APL0298	33950073ARM K2132C2PD-50-F 0N0650908 APL 0298 . NIPVNMPP 0919	65 nm <sup>[9]</sup>	71.8 mm <sup>2[19]</sup>		ARMv7	600 MHz single-core Cortex-A8	L1i: 32 KB L1d: 32 KB L2: 256 KB	PowerVR SGX535		
	APL2298	33950075 ARM KAX26303PE-56C8 YNE089AC 9328 APL2298 M232R00 0946	45 nm <sup>[6]</sup>	41.6 mm <sup>2[6]</sup>		ARMv7	600–800 MHz single-core Cortex-A8	L1i: 32 KB L1d: 32 KB L2: 256 KB	PowerVR SGX535 @ 200 MHz		
A4	APL0398	**************************************	45 nm <sup>[6][19]</sup>	53.3 mm <sup>2[6][19]</sup>		ARMv7	0.8–1.0 GHz single-core Cortex-A8	L1i: 32 KB L1d: 32 KB L2: 512 KB	PowerVR SGX535 <sup>[128]</sup>		
	APL0498	66108666 860014V	45 nm <sup>[38]</sup>	122.2 mm <sup>2[38]</sup>			0.8–1.0 GHz dual-core Cortex-A9	L1i: 32 KB L1d: 32 KB L2: 1 MB	PowerVR SGX543MP (dual-core) @ 200 MH (12.8 GFLOPS) <sup>[129]</sup>		



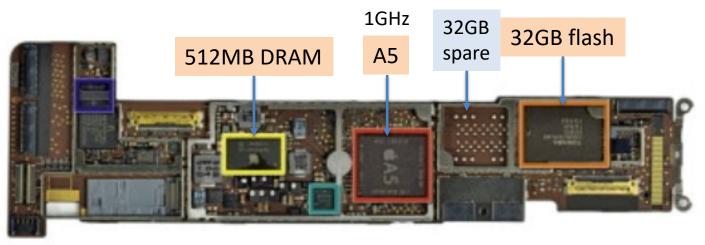
### A5 CPU on iPad2



COMP122

Hennessy & Patterson —

The logic board of Apple iPad 2 in the previous figure. The photo highlights five integrated circuits. The large integrated circuit in the middle is the Apple A5 chip, which contains dual ARM processor cores that run at 1 GHz as well as 512 MB of main memory inside the package. The next figure shows a photograph of the processor chip inside the A5 package. The similar-sized chip to the left is the 32GB flash memory chip for non-volatile storage. There is an empty space between the two chips where a second flash chip can be installed to double storage capacity of the iPad. The chips to the right of the A5 include power controller and I/O controller chips. (Courtesy iFixit, www.ifixit.com)





### A Series: A4-7



COMP122



The **Apple A4** is a 32-bit package on package (PoP) system on a chip (SoC) designed by Apple Inc. and manufactured by Samsung. It was the first SoC Apple designed in-house. The first product to feature the A4 was the first-generation iPad, followed by the iPhone 4, fourth-generation iPod Touch, and sec

32/64-bit

The Apple A5 is a 32-bit system on a chip (SoC) designed by Apple Inc. and manufactured by Samsung. The first product Apple featured an A5 in was the iPad 2. Apple claimed during their media event on March 2, 2011 that the ARM Cortex-A9 central processing unit (CPU) in the A

Ö





1st Apple design

- ❖ iPad 1
- iPhone 4

❖ iPhone 5S

The Apple A7 is a 64-bit system on a chip (SoC) designed by Apple Inc. It first appeared in the iPhone 5S, which was announced on September 10, 2013, and the iPad Air, announced October 22, 2013. Apple states that it is up to twice as fast and has up to twice the graphics power compared





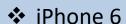
### A8-11



COMP122

64-bit

The Apple A8 is a 64-bit ARM-based system on a chip (SoC) designed by Apple Inc. It first appeared in the iPhone 6 and iPhone 6 Plus, which were introduced on September 9, 2014. Apple states that it has 25% more CPU performance and 50% more graphics performance while





The Apple A10 Fusion is a 64-bit ARM-based system on a chip (SoC), designed by Apple Inc. and manufactured by TSMC. It first appeared in the iPhone 7 and 7 Plus which were introduced on September 7, 2016, and is used in the sixth-generation iPad, seventh-generation iPad, and





#### iPhone 6S

The Apple A9 is a 64-bit ARM-based system-on-chip (SoC), designed by Apple Inc.

Manufactured for Apple by both TSMC and Samsung, it first appeared in the iPhone 6S and 6S Plus which were introduced on September 9, 2015. Apple states that it has 70% more CPU



#### ❖ iPhone 8

The Apple A11 Bionic is a 64-bit ARM-based system on a chip (SoC), designed by Apple Inc. and manufactured by TSMC. It first appeared in the iPhone 8, iPhone 8 Plus, and iPhone X which were introduced on September 12, 2017. Apple states that the two high-performance cores are 2.





### A12-14 + M1



**COMP122** 

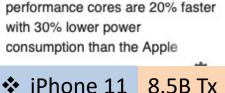
64-bit

The Apple A12 Bionic is a 64-bit ARM-based

system on a chip (SoC) designed by Apple Inc. It first appeared in the iPhone XS, XS Max, XR, the 2019 versions of the iPad Air and iPad Mini, and the iPad (2020). Apple states that the two high-performance cores are 15% faster and 50% more energy-ef



The Apple A13 Bionic is a 64-bit ARM-based system on a chip (SoC), designed by Apple Inc. It appears in the iPhone 11, 11 Pro/Pro Max and the iPhone SE. Apple states that the two high with 30% lower power





❖ iPad Air/Mini

iPhone XS

❖ iPhone 12 11.8B Tx

The Apple A14 Bionic is a 64-bit ARM-based System on a Chip (SoC), designed by Apple Inc. It appears in the fourth generation iPad Air, as well as iPhone 12 Mini, iPhone 12, iPhone 12 Pro, and iPhone 12 Pro Max. Apple states that the Central Processing Unit (CPU) performs up to 40%



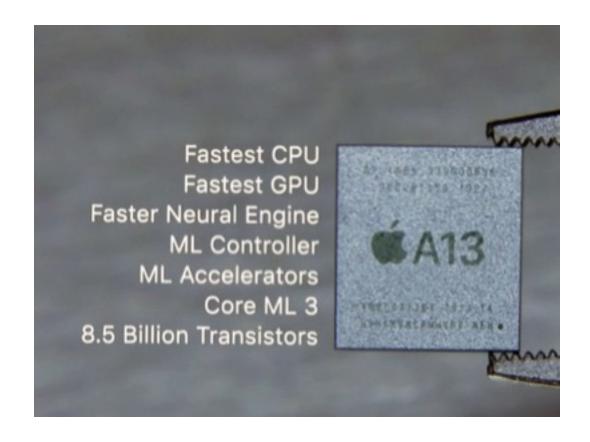
#### MacBook Air/Pro 16B Tx

The Apple M1 is the first ARMbased system on a chip (SoC) designed by Apple Inc. as a central processing unit (CPU) for its line of Macintosh computers. It is deployed in the MacBook Air, Mac mini, and the MacBook Pro. It is the first personal computer chip built using a 5 nm process. Ap













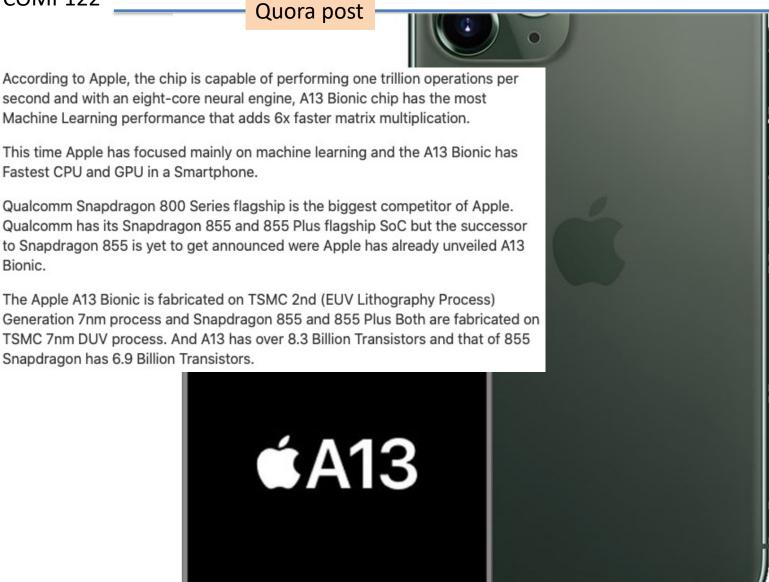
#### iPhone12,3

Single-Core Score		Multi-Core Score					
5472 Geekbench 4.4.1 for iOS AArch64		13769					
Result Information							
Upload Date	September 11 2019 11:03 PM						
Views	3591						
System Information							
System Information							
Operating System	IOS 13.0						
Model	iPhone12,3						
Motherboard	D421AP						
Memory	3759 MB						
Processor Information							
Name	ARM						
Topology	1 Processor, 6 Cores						
Identifier	ARM						
Base Frequency	2.66 GHz						
L1 Instruction Cache	48.0 KB x 1						
L1 Data Cache	48.0 KB x 1						
L2 Cache	4.00 MB x 1	4.00 MB x 1					



## Apple ARM A Series







# Apple ARM A12/13 SoC



This is a block diagram of the Apple A12X with 10 billion transistors. Of that amount, only 25% is dedicated to the two CPU clusters:

- ❖ 8 CPU❖ 7 GPU
- ♣ 1 NPU
- ❖ 2 MCU

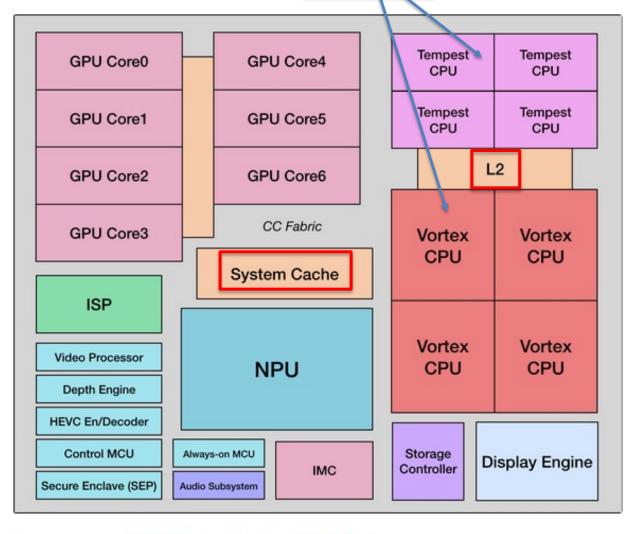


Image source: A12X Bionic - Apple - WikiChip



# Apple A11/12/13



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Name	Model no.	Image	Semiconductor technology	Die size	Transistor count	CPU ISA	СРИ	CPU cache	GPU
A13 Bionic	APL1W85	API 1986 839500988 12A2090996 1522	7 nm FinFET (TSMC N7P)	98.48 mm <sup>2[174]</sup>	8.5 billion	ARMv8.4-A <sup>[175]</sup>	2.65 GHz hexa-core (2× Lightning + 4× Thunder)	L1i: 128 KB L1d: 128 KB L2: 8 MB L3: none <sup>[176]</sup>	Custom design (quad- core)
A12Z Bionic	APL1083	PL1083	7 nm FinFET (TSMC N7)	≈135 mm <sup>2[172]</sup>	10 billion	ARMv8.3-A <sup>[168]</sup>	2.49 GHz octa- core (4× Vortex + 4× Tempest)	L1i: 128 KB L1d: 128 KB L2: 8 MB L3: none <sup>[173]</sup>	Custom design (octacore)
A12X Bionic									Custom design (heptacore)
A12 Bionic	APL1W81	* CONTROL OF STREET	7 nm FinFET (TSMC N7)	83.27 mm <sup>2[167]</sup>	6.9 billion	ARMv8.3-A <sup>[168]</sup>	2.49 GHz hexa-core (2× Vortex + 4× Tempest) <sup>[169]</sup>	L1i: 128 KB L1d: 128 KB L2: 8 MB L3: none <sup>[169]</sup>	Custom design (quad- core)
A11 Bionic	APL1W72	• intim rissis	10 nm FinFET (TSMC)	87.66 mm <sup>2[162]</sup>	4.3 billion	ARMv8.2-A <sup>[163]</sup>	2.39 GHz hexa-core (2x Monsoon + 4x Mistral)	L1i: 64 KB L1d: 64 KB L2: 8 MB L3: none <sup>[164]</sup>	Custom design (triple-core)



### Apple A12X



#### Apple A12X Bionic



#### General Info

Launched October 30, 2018

Discontinued March 18, 2020

Designed by Apple Inc.

Common TSMC<sup>[1]</sup>

manufacturer(s)

Product code APL1083<sup>[2]</sup>

Max. CPU clock to 2.49[3] GHz

rate

Cache

L1 cache 128 KB instruction, 128 KB

data

L2 cache 8 MB

Architecture and classification

Application Mobile

Min. feature size 7 nm<sup>[4]</sup>



### Apple A12X



#### Design [edit]

The A12X features an Apple-designed 64-bit ARMv8.3-A octa-core CPU, with four high-performance cores called **Vortex** and four energy-efficient cores called **Tempest**.<sup>[4][1]</sup> The Vortex cores are a 7-wide decode out-of-order superscalar design, while the Tempest cores are a 3-wide decode out-of-order superscalar design. Like the Mistral cores, the Tempest cores are based on Apple's Swift cores from the Apple A6, and are similar in performance to ARM Cortex-A73 CPU cores.<sup>[5][6]</sup> It is Apple's first SoC with an octa core CPU.<sup>[1]</sup>

The A12X integrates an Apple-designed septa core graphics processing unit (GPU) with twice the graphics performance of the A10X.<sup>[4]</sup> Embedded in the A12X is the M12 motion coprocessor.<sup>[7]</sup> The A12X includes dedicated neural network hardware that Apple calls a "Next-generation Neural Engine".<sup>[4]</sup> This neural network hardware, which is the same as found in the A12,<sup>[1]</sup> can perform up to 5 trillion operations per second.<sup>[4]</sup>

The A12X is manufactured by TSMC using a 7 nm FinFET process, and it contains 10 billion transistors<sup>[1][4]</sup> vs. the 6.9 billion on the A12.<sup>[8]</sup> The A12X is paired with 4 GB of LPDDR4X memory in the third-generation 12.9" iPad Pro and the 11" iPad Pro or 6 GB in the 1TB storage configurations.<sup>[9][2]</sup>

#### Products that include the Apple A12X [edit]

- iPad Pro 2018 11-inch (First-generation)
- iPad Pro 2018 12.9-inch (Third-generation)



### Apple ARM A13



Intel chips are **x86** ISA and multi-core CPU (only). Apple chips are **ARM** ISA with multi-core CPU's, GPU's, and NPU, MCU's. The latest Apple chip is the **A13**, succeeding the powerful **A12X** as the first "bionic" SoC.

**A13**: The A13 is the latest multi-core architecture designed by Apple with 8.5B transistors manufactured at TSMC (7nm EUV) -- extremely state-of-the-art. The A13 was released Sept. **2019** and is used in the iPhone **11**.

It contains a large number of **ARMv8** ISA cores: 6 CPU (2.65GHz) + 4 GPU + 8 NPU + 2 MCU. (Note that the A12X/Z has 8 CPU cores + 8 GPU's). All cores are Apple designed (ARM 64-bit v8 ISA is licensed). It includes a Neural engine (8x NPU) with machine learning (core ML 3 at 6x faster matrix multiply) -- which sets it apart from Intel chips without GPU's or an NPU. The GPU's can perform 1 trillion operations per second (1 Tflops=1000 Gflops), and the NPU may hit 5 Tflops. It has extreme power management as well (so good for portables and mobile).



# Apple ARM A12/13 SoC















#### 3 Answers



Matthew J. Stott, Senior Systems & Mac Engineer (1996-present)

Answered Sep 30



It's called a SoC - System on Chip. It means the CPU package includes a lot more than just the CPU cores. What's changed with the A13 is even more power management abilities to shut off unused parts of the A13 but also right down to individual transistors as well. It is the most advanced power management in use right now. It is responsible for the excellent battery life of the 11, 11 Pro, 11 Pro Max iPhones. Yes, they increased the battery capacity a bit at the same time but that is just improved battery engineering.

Add to Yowan's A12X the Image Processing Core, a couple of Machine Learning accelerator cores and a bit less on the GPU with the A13 Bionic SoC. It is expected there will be an A13X for upgrade iPad Pros coming soon.





Quora post

And I think iPhones are going to be more power-efficient than Snapdragon 855 powered Android Phones. If you are asking about CPU, then the A13 Bionic is based on 64-bit Fusion Architecture. It is a Hexa-Core CPU with 2 Performance cores and 4 Efficiency cores. And it consumes 40% less power than the A12 Bionic. Coming to 855 Snapdragon, both Snapdragon 855 and 855 Plus is an ARM 64-bit SoC with Kryo 485 Octa-Core CPU. And it has Three CPU Clusters: 1 Cortex-A76 Prime Core, 3 Cortex-A76 Performance Cores and 4 Cortex-A55 Efficiency Cores. From these it seems Snapdragon 855 will definitely be a strong competitor for the Apple A13 Bionic Chip.

Moreover, while talking about GPU, for Apple, it is an Apple-designed Quad Core GPU and Snapdragon 855 has Adreno 640 GPU. And I don't think the Snapdragon will beat the performance of Apple's A13 bionic chip.



# A Series: ARMv7/8



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	ISA		Cores			Cache		Speed
	ARMv7-A	Swift <sup>[73]</sup>	2 cores. ARM / Thumb / Thumb-2 / DS / NEON	P / SIMD / VFPv4 FPU	L1: 32 KB / 32 KB, L2: 1 MB			3.5 DMIPS/MHz per core
	ARMv8-A	Cyclone <sup>[74]</sup>	2 cores. ARM / Thumb / Thumb-2 / DS / NEON / TrustZone / AArch64. Out-o		L1: 64 KB / 64	3, L3: 4 MB	1.3 or 1.4 GHz	
	ARMv8-A	Typhoon <sup>[74][75]</sup>	2 or 3 cores. ARM / Thumb / Thumb-2 FPU / NEON / TrustZone		L1: 64 KB / 64 KB, L2: 1 MB or 2 MB, L3: 4 MB			1.4 or 1.5 GHz
	ARMv8-A	Twister <sup>[76]</sup>	2 cores. ARM / Thumb / Thumb-2 / DS / NEON / TrustZone / A		KB, L2: 2 MB, L3: 4 MB or 0 MB		1.85 or 2.26 GHz	
Ax	ARMv8.1-A	Hurricane and Zephyr <sup>[77]</sup>	Hurricane: 2 or 3 cores. AArch64, 6-de superscalar, out-of-o Zephyr: 2 or 3 cores. AA	rder	L1: 64 KB / 64 KB, L2: 3 MB or 8 MB, L3: 4 MB or 0 MB			2.34 or 2.38 GHz
(Apple)	ARMv8.2-A	Monsoon and Mistral <sup>[78]</sup>	Monsoon: 2 cores. AArch64, 7-decod superscalar, out-of-o Mistral: 4 cores. AArch64, out-of-orde on Swift.	rder	L1I: 128 KB, L1D: 64 KB, L2: 8 MB, L3: 4 MB			2.39 GHz
	ARMv8.3-A	Vortex and Tempest <sup>[79]</sup>	Vortex: 2 or 4 cores. AArch64, 7-deco superscalar, out-of-o Tempest: 4 cores. AArch64, 3-dec superscalar. Based on	order code, out-of-order,	L1: 128 KB / 128	3 KB, L2: 8 M	IB, L3: 8 MB	2.5 GHz
	ARMv8.4-A	Lightning and Thunder <sup>[80]</sup>	Lightning: 2 cores. AArch64, 7-decor superscalar, out-of-o Thunder: 4 cores. AArch64, out-of-	order	L1: 128 KB / 128 KB, L2: 8 MB, L3: 16 MB			2.66 GHz



# Apple T1/2 SoC



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MacBook Pro

#### T series list [edit]

				77							
Name	Model no.	Image	Semiconductor technology	Die size	CPU ISA	CPU	CPU cache	GPU	Memory technology	Introduced	Utilizing devices
T1	APL1023 <sup>[190]</sup>	# 5910884310 01634			ARMv7			TBD		October 2016	<ul> <li>MacBook Pro (13-inch, 2016, Four Thu</li> <li>MacBook Pro (15-inch, 2016)</li> <li>MacBook Pro (13-inch, 2017, Four Thu</li> <li>MacBook Pro (15-inch, 2017)</li> </ul>
T2	APL1027 <sup>[191]</sup>	LOTOSSOCC CEOL Ter PIN-JANANA BANANA			ARMv8-			TBD	LPDDR4	December 2017	<ul> <li>iMac Pro 2017</li> <li>MacBook Pro (13-inch, 2018, Four Thue)</li> <li>MacBook Pro (15-inch, 2018)</li> <li>Mac mini (2018)</li> <li>MacBook Air (2018)</li> <li>MacBook Pro (15-inch, 2019)</li> <li>MacBook Pro (13-inch, 2019)</li> <li>MacBook Air (2019)</li> <li>MacBook Pro (16-inch, 2019)</li> <li>Mac Pro (2019)</li> <li>MacBook Air (2020)</li> </ul>



# **Apple Special Processor**





The Apple M-series coprocessors are motion coprocessors used by Apple Inc. in their mobile devices. First released in 2013, their function is to collect sensor data from integrated accelerometers, gyroscopes and compasses and offload the collecting and processing of sensor data from the main



### Section



# Apple Chips

M1 (ARM v8)

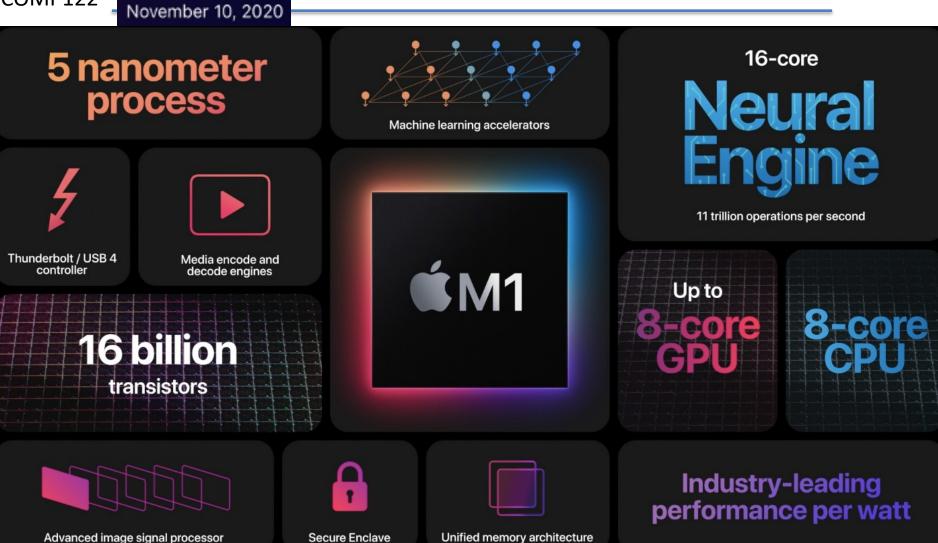


### Apple M1



**COMP122** 

Advanced image signal processor





# Apple M1



# 5-nanometer process

The first personal computer chip built with this cutting-edge technology.

# 16 billion transistors

The most we've ever put into a single chip.





# Apple M1 Module







## Apple M1



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November 10, 2020

# 11 trillion

11 Tera FLOPS

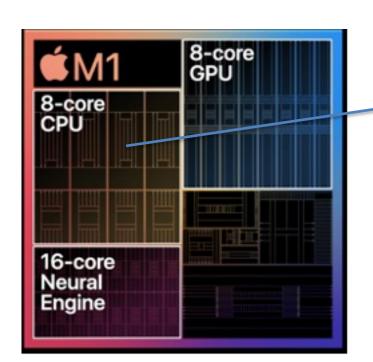
Operations per second

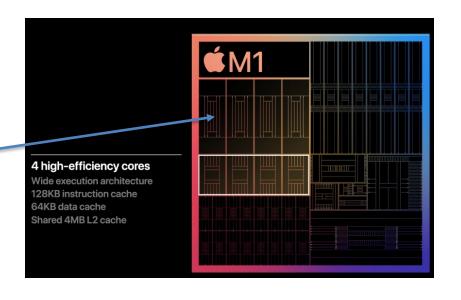
- **Cores** 
  - □ 8 CPU
  - 8 GPU
  - □ 16 NPU



- CPU cores
  - 4 Hi Perf (20W P)
  - 4 Hi Efficiency

(1.3W low power E)







### Apple M1 vs x86 CPUs



# Why is the Intel microchip inferior to the MacBook M1 microchip, in average-user, normal-computing terms?



Jeff Drobman, Lecturer at California State University, Northridge (2016-present)

Answered just now

core count. Intel *microchips* come in a broad array of core counts, both CPU and GPU. the Apple M1 has 8 CPU, 8GPU and 16 NPU cores. it would perform comparable to any other such chip — with same number of cores. high-end x86 chips from Intel (Xeon) and AMD (Epyc) will outperform the M1 by a lot, but low end ones will not.



### Apple M1 SoC



What's the architectural difference between the low-power and high-performance Apple M1 cores, and can both execute the same instruction sets?



**Jeff Drobman**, Lecturer at California State University, Northridge (2016-present)

Answered just now

the Apple M1 SoC has 8 CPU cores plus 8 GPU, 16 NPU cores. the CPU cores all run the ARMv8 64-bit ISA. while I don't know the specifics, a CPU core can lower its power consumption by lowering its frequency, and maybe by low powering (Sleep) some less often used functions like L2 or L3 cache. A CPU core can only increase its performance via parallelism. SMT with superscalar is the usual way, along with parallel data via SIMD extensions.



### Apple M1







#### Shresth Sonkar, Mac User since 2014

Answered December 20



- The M1 has a max TDP of 20W and a nominal TDP of 15W. This is way lesser than the previous intel chips used in previous generation — which had 28W nominal TDP. Thus, the heat generation itself is lower
- Since the heat generation is lower, the MacBook Air can handle it via passive cooling using a aluminium heat spreader which carries heat away from processor via conduction instead of convection cooling which uses a fan to blow cool air over the CPU.
- 3. The M1 has asymmetric cores 4 efficiency cores of the octa core design are working on barely 1.3W of power while the rest 4 performance cores are working at 13.8W. This means that the M1 generates less heat in day to day usage to require cooling. Only when the performance cores and GPU are being used, does the power spike up to the 20W figure.

All this makes the M1 a rather highly thermally efficient processor — which doesn't waste energy as heat. It is producing way less heat than intel processors in the same segment of laptops and thus doesn't need a fan.

For comparison, the A14 powering iPhone 12 lineup has 5W TDP, about a third of the Macs. So 5W is not much for a smart phone and 15 is definitely not much for a laptop which has way more surface area for dissipating heat than a smartphone.



### SoC's



# Why don't electronic chip manufacturers have most of the features of a whole computer on one chip similar to the Apple M1 SoC? Is it cost or problems manufacturing it?



Jeff Drobman, Lecturer at California State University, Northridge (2016-present)

Answered just now

manufacturers? even Apple does not manufacture chips. if you mean designers, like Apple, then many do have multi-core SoC's. Intel is the only desktop CPU supplier that also manufactures their own chips. Samsung is the only mobile CPU supplier that also manufactures their own chips.

the parts of a "whole computer" that might not fit onto an SoC are large DRAM (best left to separate chips) and I/O devices like sensors. mobile CPU's or SoC's are designed by Qualcomm

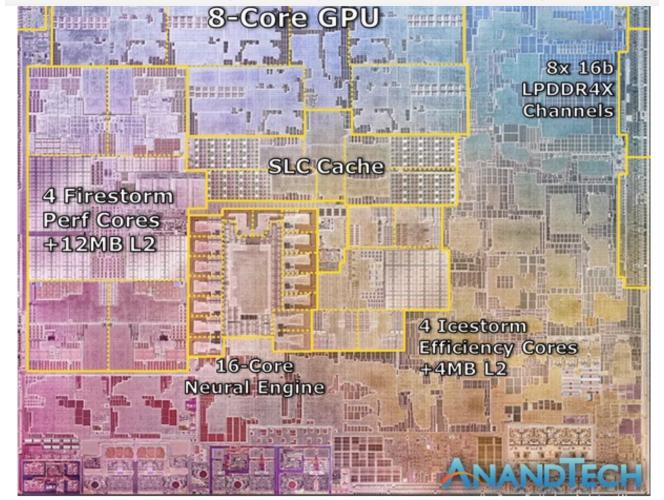


# Apple M1



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- I don't know how big SLC is.
  - It looks physically smaller than the 12MB L2 in the Firestorm cores, but it probably uses noticeably denser SRAM cells. L2 may be optimized for very low latency.
  - The memory latency numbers measured by AnandTech show drop-offs at 8MB and 32MB.
  - Drop off ar 8MB is probably L2 capacity. However, Firestorm supposedly has 12MB L2, so that suggests some partitioning. I wouldn't be surprised to learn that 4MB is instructiononly to help Rosetta.
  - Drop off ar 32MB is likely SLC capacity. 32MB sounds reasonable actually.





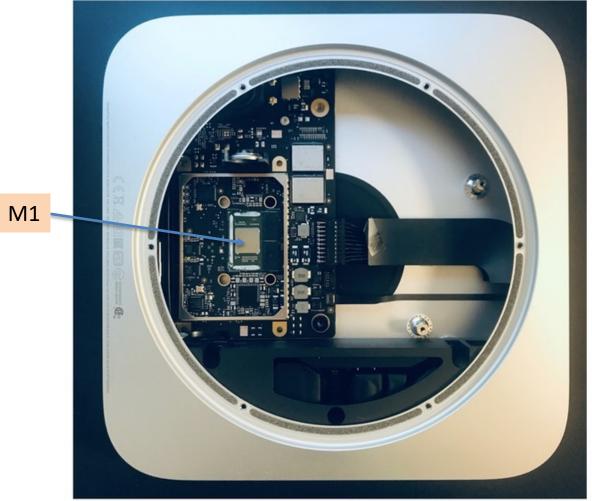
#### COMP122

# Apple M1



Joe Zbiciak replied to your comment on an answer to: "If putting two GPUs in a computer is normal, why isn't putting two CPUs?"

I found an actual picture (rather than illustration) of the M1 with its heat spreader removed. You can see it in the middle-left. It looks a lot like the illustration. Link.



M1 SoC exposed and ready to test (photo credit: Don Scansen)



# **Apple Event**



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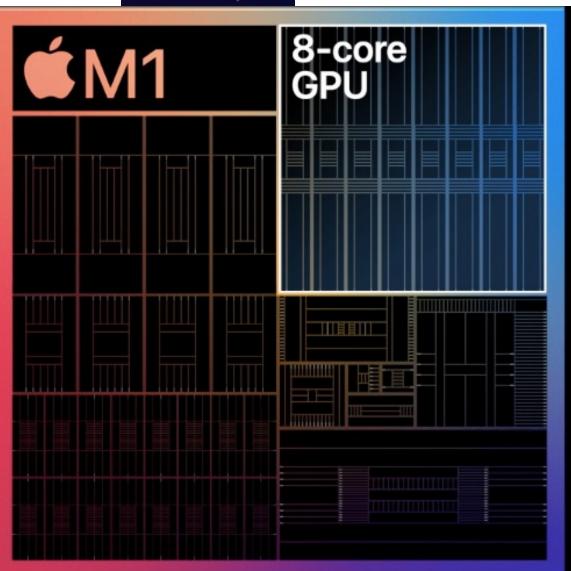
November 10, 2020							
Advanced power management	High-efficiency CPU cores	High-per CPU core	formance Secure s Enclave		Low-power vide playback		
10.1.1	Advanced display engine			High-performa	High-performance GPU		
High-bandwidth caches							HDR imaging
	HDR video processor	ćM1					
Cryptography acceleration							
					High-performa	nce	
High-performance unified memory	Always-on processor						
					Thunderbolt / U controller	ISB 4	controller
Machine learning accelerators	High-quality image signal processor	Low-power design	High-perfo		High-efficiency aud processor	lio	Advanced silicon packaging





COMP122

November 10, 2020



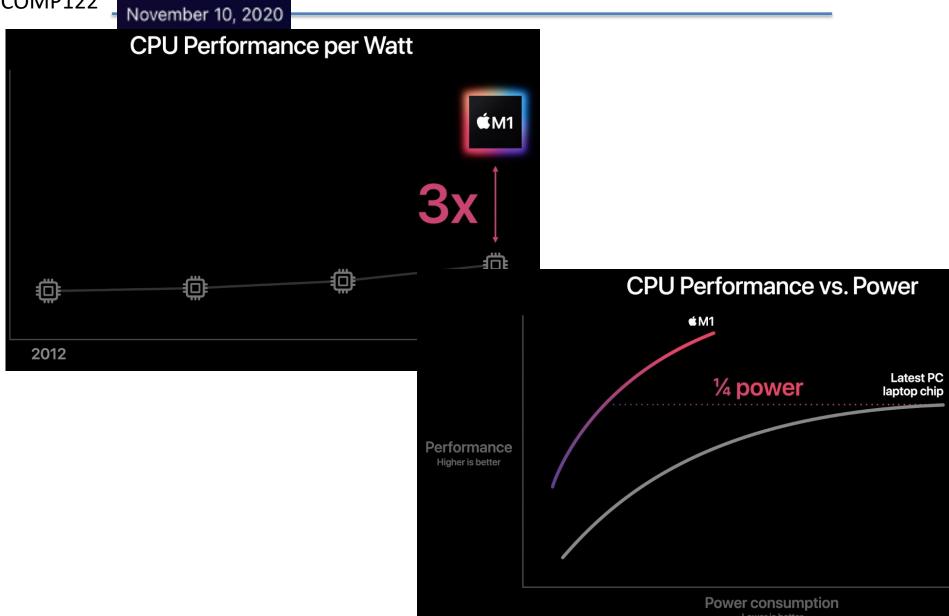
#### Up to 8 cores

128 execution units
Up to 24,576 concurrent threads
2.6 teraflops
82 gigatexels/second
41 gigapixels/second







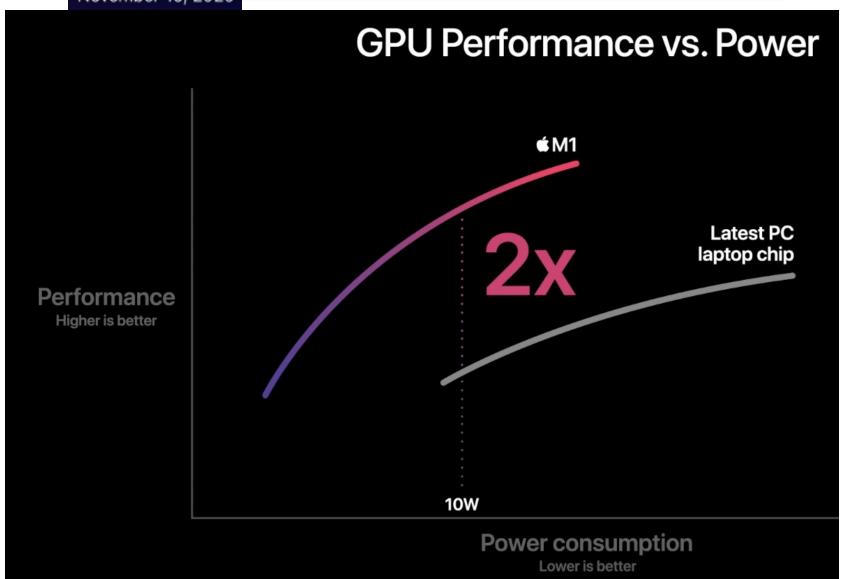






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November 10, 2020

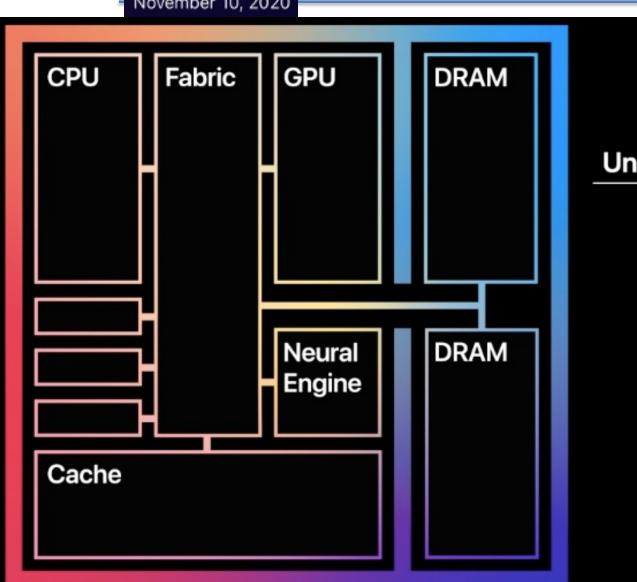






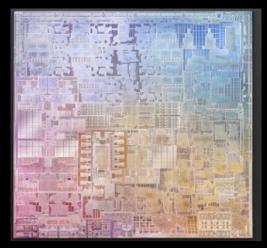
**COMP122** 

November 10, 2020



#### Unified memory architecture

High bandwidth, low latency Apple-designed package Accessible to entire SoC

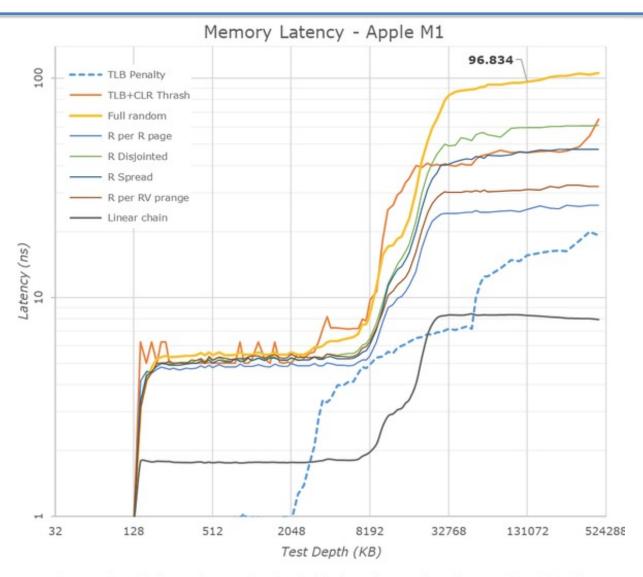




#### COMP122

#### M1 Memory





 There's a lot of unknown in AnandTech's die labeling. Also, we don't know Apple's SLC policy or interconnect architecture. Apple has demonstrated repeatedly that they're more than happy to ignore ARM's standard mechanism and methodologies.



#### M1 Benchmark



	Apple iPad pro 12.9 (M1)		Microsoft Surface Pro 7 (Intel Core i5-1035G4 10th Gen)
Single-Core	1714	1740	862
Multi-Core	7272	7694	3104
OpenCL Score	20887	18347	7801

Apple's M1-based iPad Pro's benchmarks are in line with other M1-based systems.





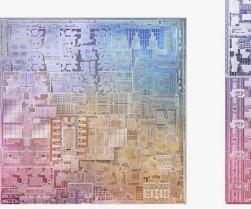




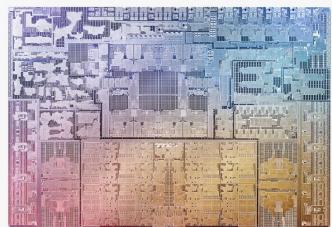
## Apple M1 Pro/Max



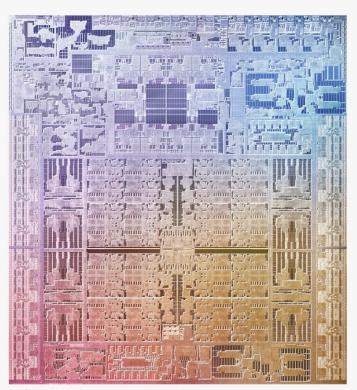








**≰**M1 Pro



**≰**M1 Max









#### 8 high-performance cores

Ultra-wide execution architecture

192KB instruction cache

128KB data cache

24MB L2 cache

#### 2 high-efficiency cores

Wide execution architecture

128KB instruction cache

64KB data cache

4MB L2 cache

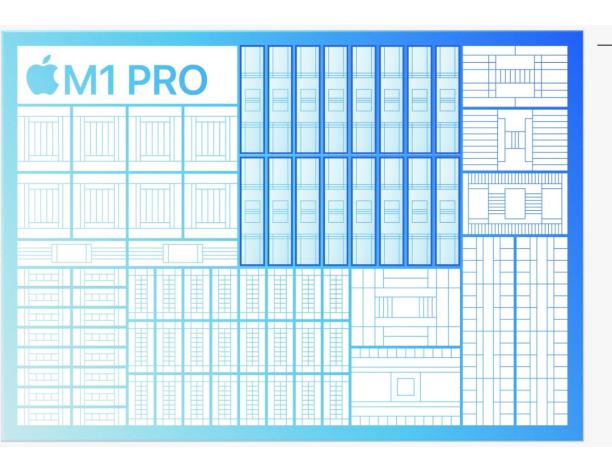


70%

Faster CPU performance than M1





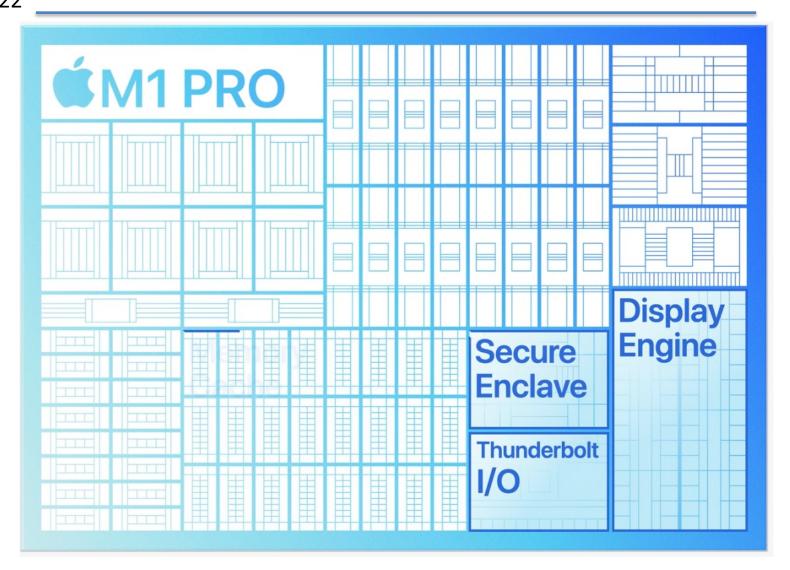


#### 16-core GPU

2048 execution units
Up to 49,512 concurrent threads
5.2 teraflops
164 gigatexels/second
82 gigapixels/second

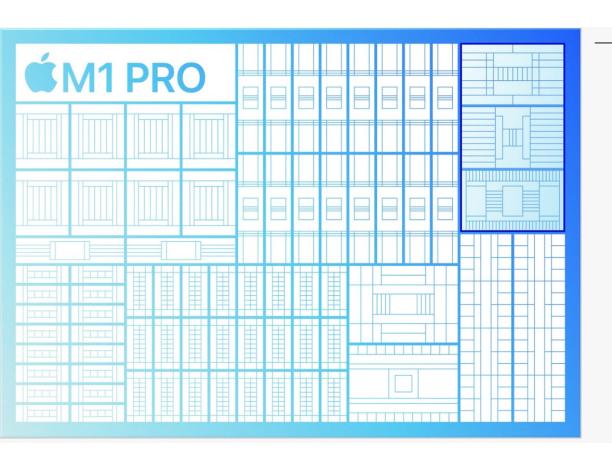










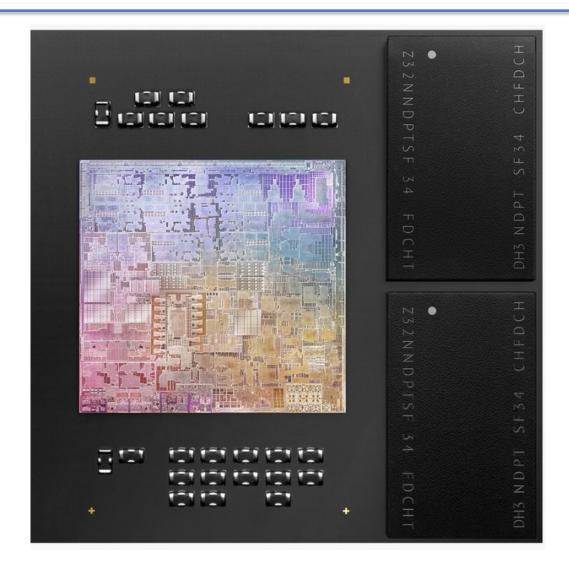


#### Media Engine

Hardware-accelerated H.264, HEVC,
ProRes, and ProRes RAW
Video decode engine
Video encode engine
ProRes encode/decode engine
Multiple streams of
4K and 8K ProRes video

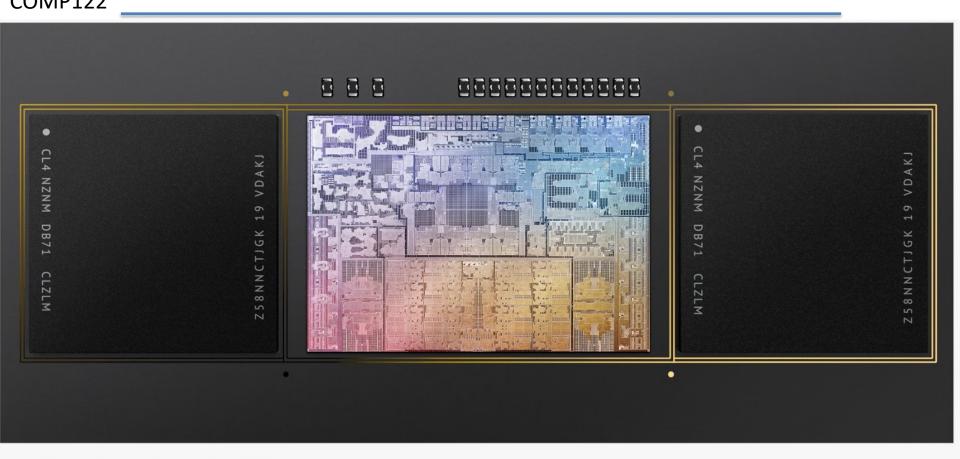












#### 32GB unified memory

High bandwidth, low latency
256-bit LPDDR5 interface
Apple-designed custom package

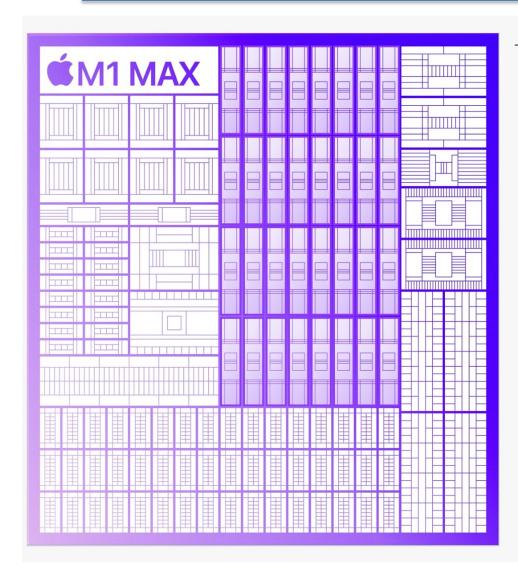






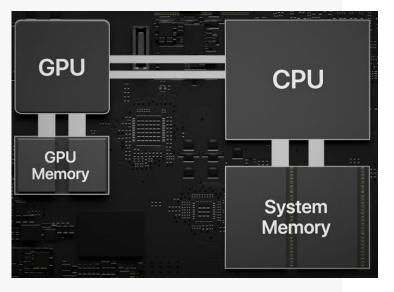






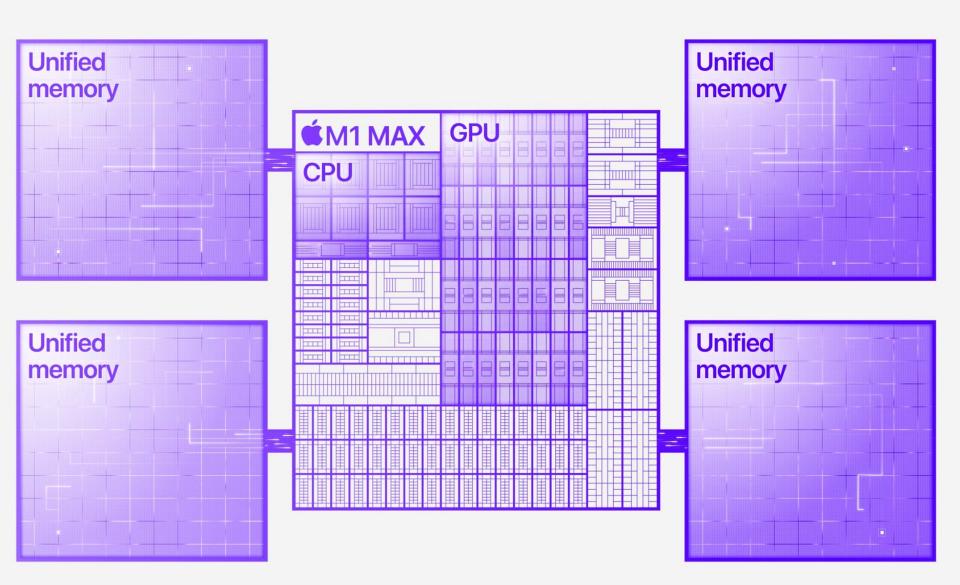
#### 32-core GPU

4096 execution units
Up to 98,304 concurrent threads
10.4 teraflops
327 gigatexels/second
164 gigapixels/second



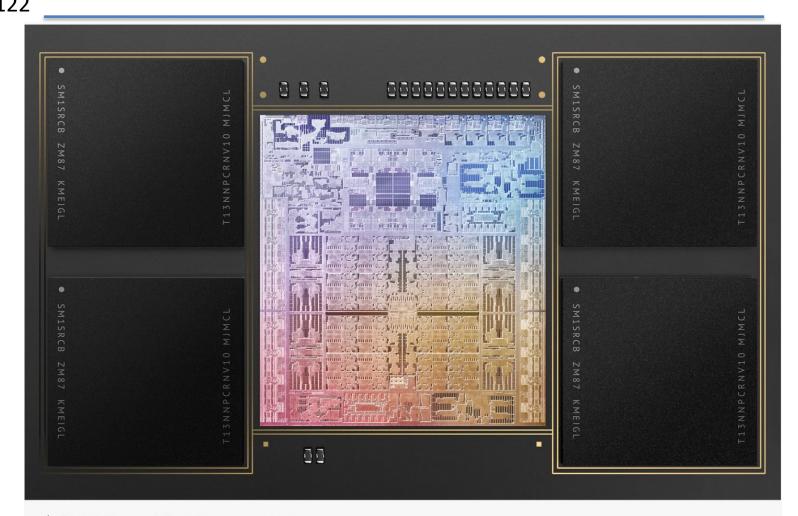












#### 64GB unified memory

High bandwidth, low latency 512-bit LPDDR5 interface Apple-designed custom package

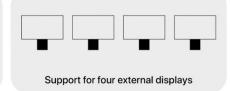
















16-core

#### Neural Engine

11 trillion operations per second

**SM1**MAX



10-core CPU



Industry-leading performance per watt

5 nm process

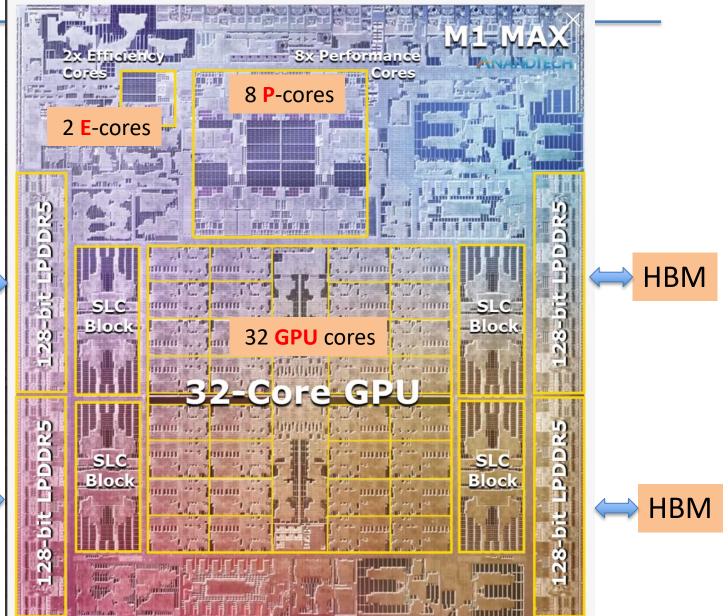
400GB/s
Memory bandwidth



#### Apple M1 Max Die







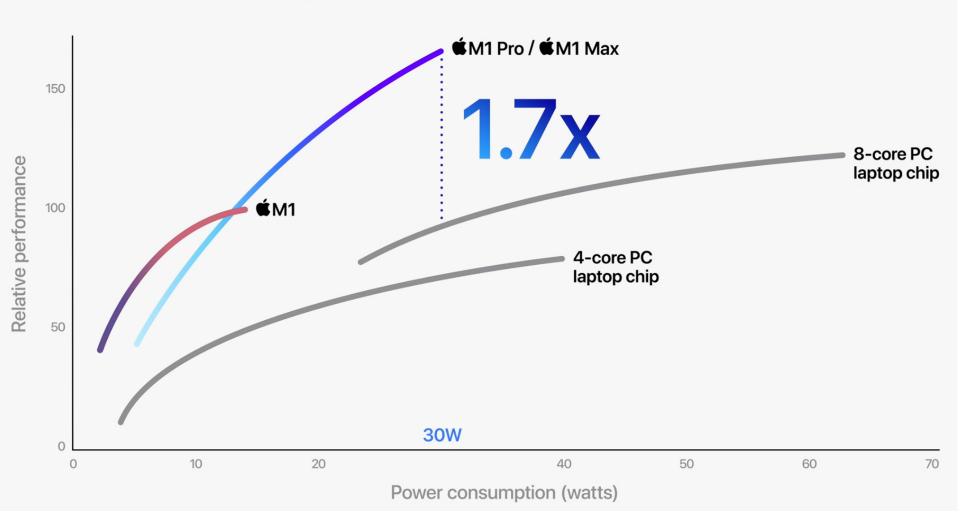
**HBM** 

**HBM** 





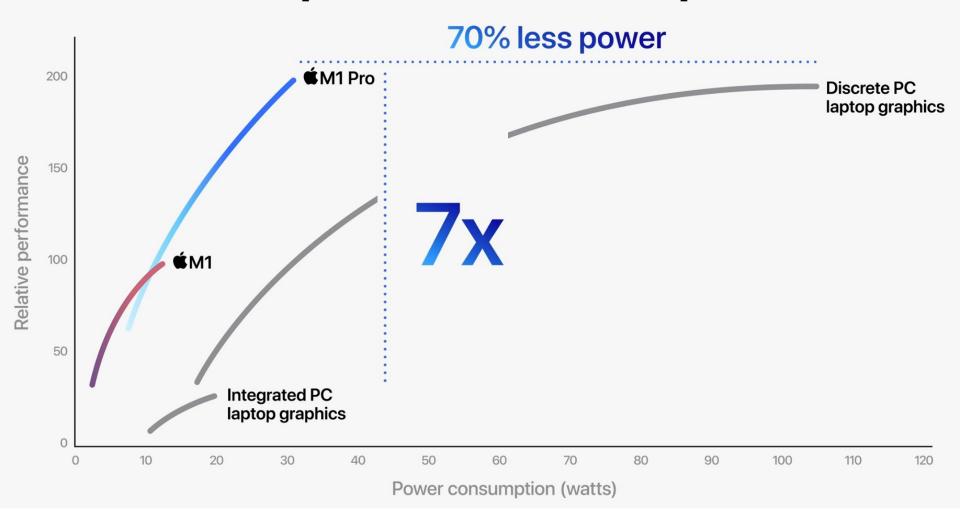
#### CPU performance vs. power







#### GPU performance vs. power







# Hardware-verified secure boot Runtime anti-exploitation Fast in-line encryption



# New Apple Event



COMP122



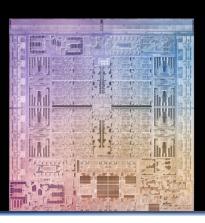


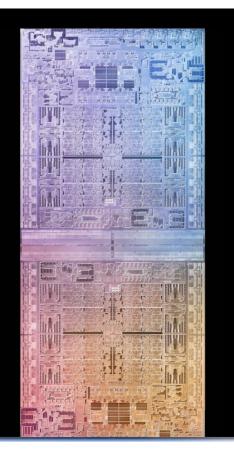


March 8, 2022



Interprocessor bandwidth











## Apple M1 Models

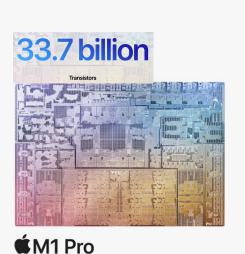


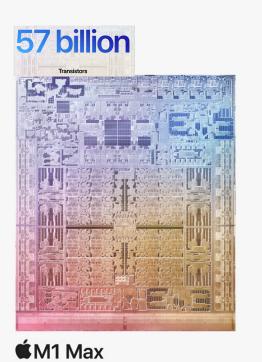
114 billion

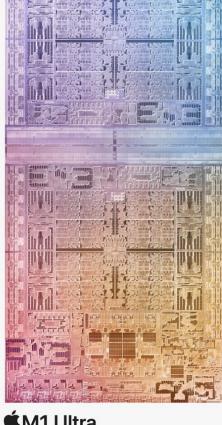
#### **Transistors**



**€**M1





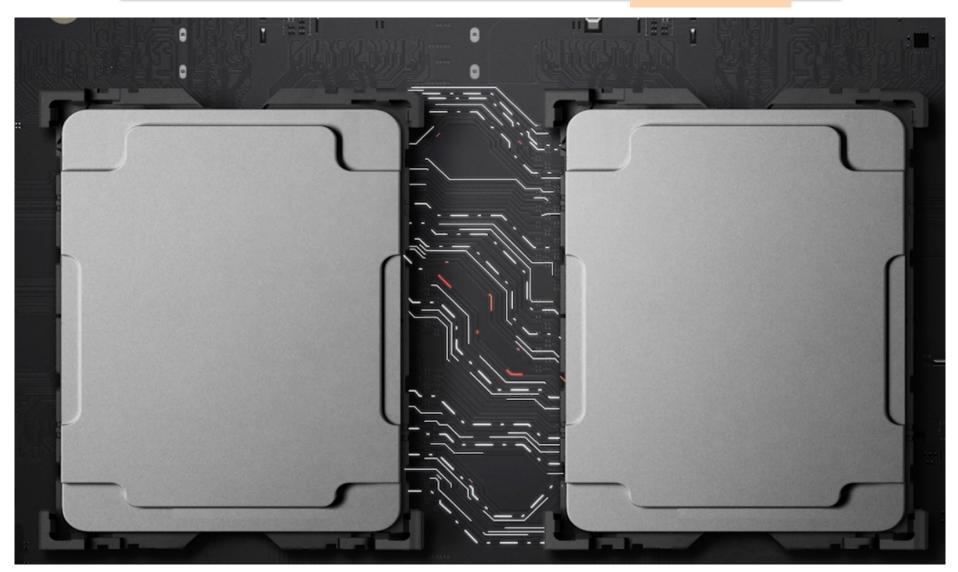


**₡**M1 Ultra





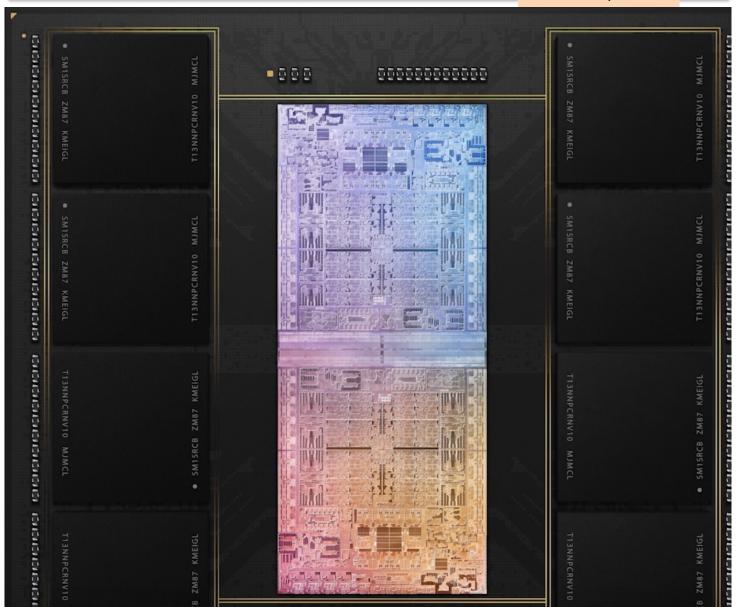
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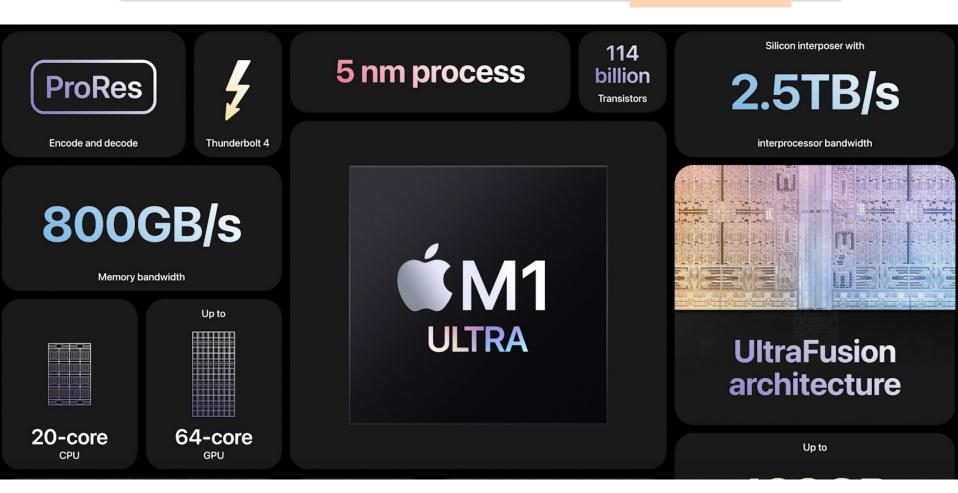


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March 8, 2022



#### 16 high-performance cores

Ultrawide execution architecture

192KB instruction cache

128KB data cache

48MB total L2 cache

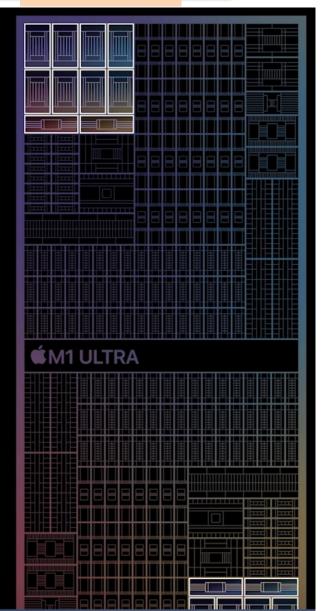
#### 4 high-efficiency cores

Wide execution architecture

128KB instruction cache

64KB data cache

8MB total L2 cache







March 8, 2022

#### 64-core GPU

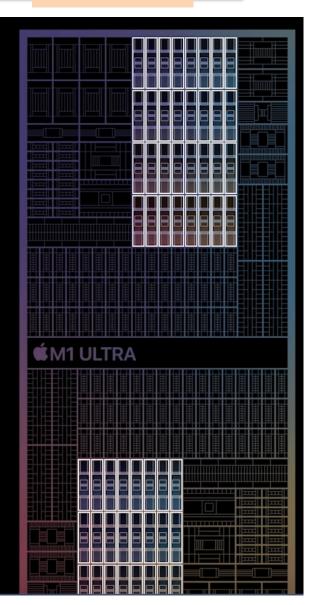
8192 execution units

Up to 196,608 concurrent threads

21 teraflops

660 gigatexels/second

330 gigapixels/second





#### M1 Ultra: CPU Performance



March 8, 2022



50% Faster

Mac Pro 28-core Xeon

#### **CPU** performance

Mac Studio M1 Ultra

90%

**Faster** 

Mac Pro 16-core Xeon



#### M1 Ultra: GPU Performance



March 8, 2022



#### **GPU** performance

Mac Studio M1 Ultra

**Faster** 



#### Section



June 6, 2022

# Apple Chips



Second-generation 5 nanometer



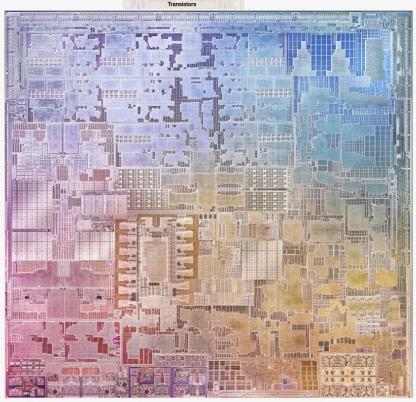
## Apple M2 Die



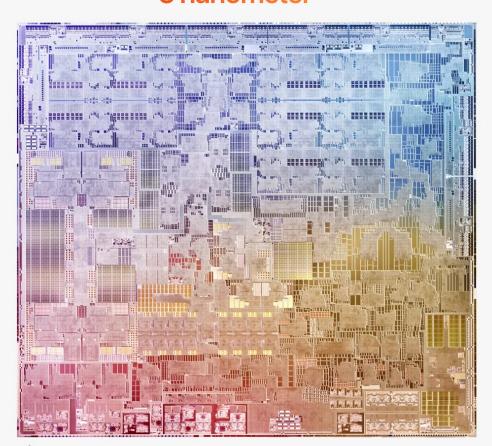
June 6, 2022

# Second-generation 5 nanometer













**Transistors** 





**COMP122** 

June 6, 2022



Up to

**24GB** 

LPDDR5 memory

#### **Second-generation** 5 nm technology



encode and decode



Over

20 billion

transistors

**High-performance** media engine

40%

**Faster Neural Engine** 



**Industry-leading** performance per watt

50% More memory bandwidth

Up to 15.8 trillion

16-core Neural Engine

operations per second



**CPU** 



18%

Faster CPU

35%

Faster GPU

100GB/s Memory bandwidth





COMP122 \_\_\_\_\_

June 6, 2022

#### 8-core CPU

P

#### 4 high-performance cores

Ultrawide microarchitecture

192KB instruction cache

128KB data cache

Shared 16MB cache

E

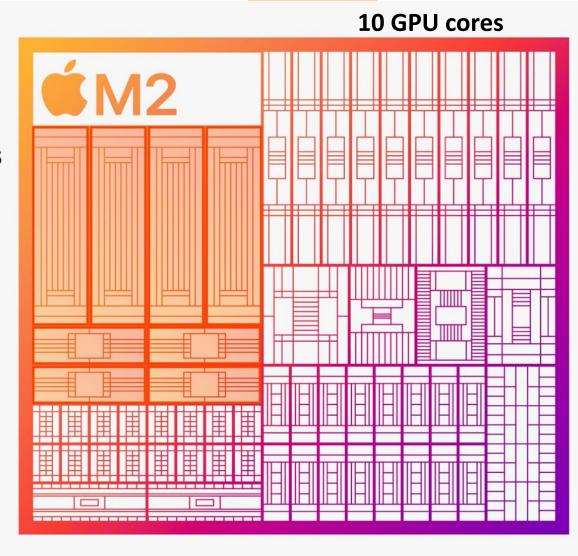
#### 4 high-efficiency cores

Wide microarchitecture

128KB instruction cache

64KB data cache

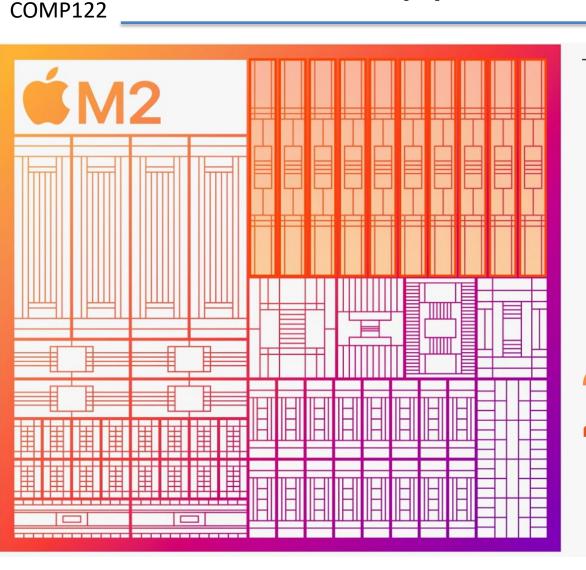
Shared 4MB cache







June 6, 2022



#### 10-core GPU

Larger L2 cache
3.6 teraflops
111 gigatexels per second

55 gigapixels per second

# 20 billon

**Transistors** 

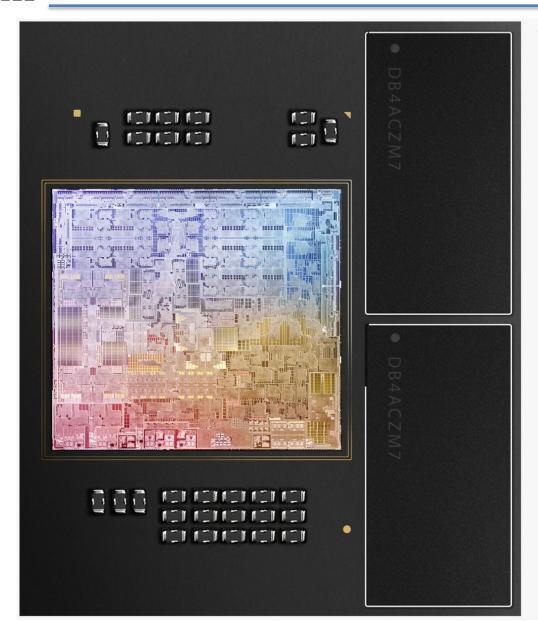


# Apple M2 Module



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June 6, 2022



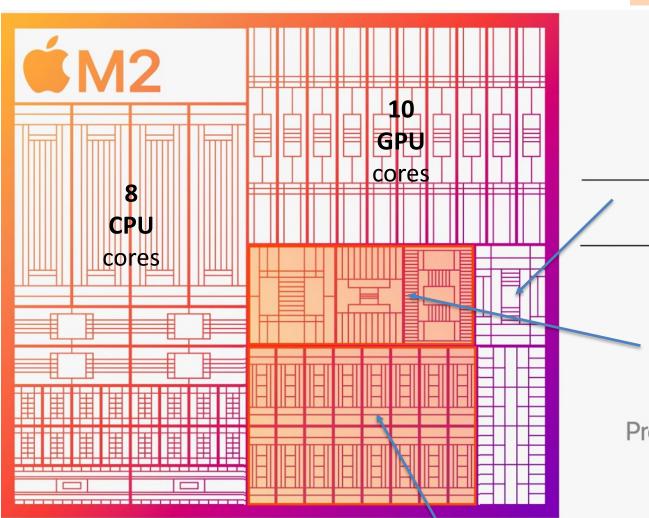
24GB unified memory





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June 6, 2022



#### **Secure Enclave**

#### Media engine

8K H.264, HEVC, ProRes
Video decode engine
Video encode engine
ProRes encode/decode engine

#### **Neural Engine**



## Apple M2 v Intel

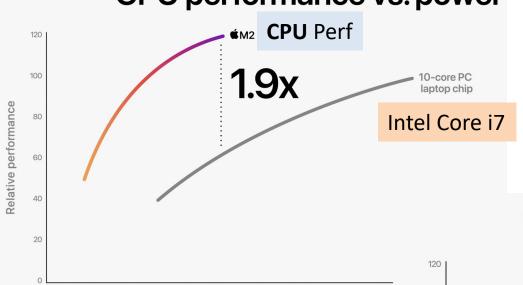


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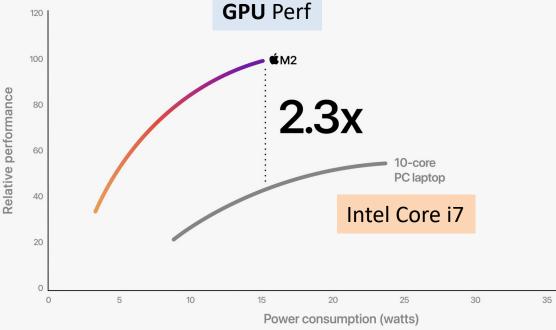
June 6, 2022



Power consumption (watts)



#### GPU performance vs. power

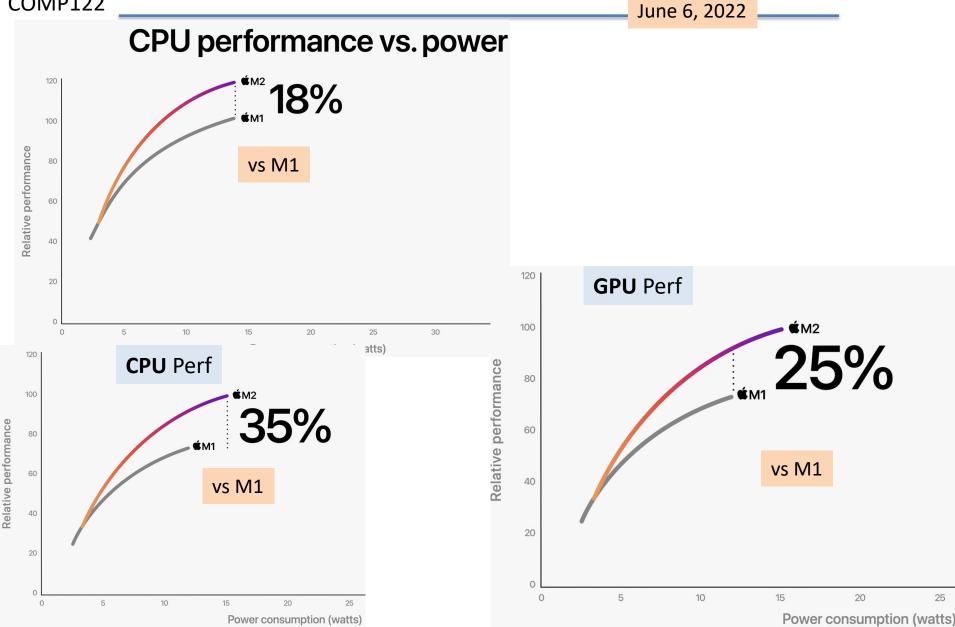




# Apple M2 v M1



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#### Section



# Apple Chip Fab/Mfg



#### TSMC 4nm

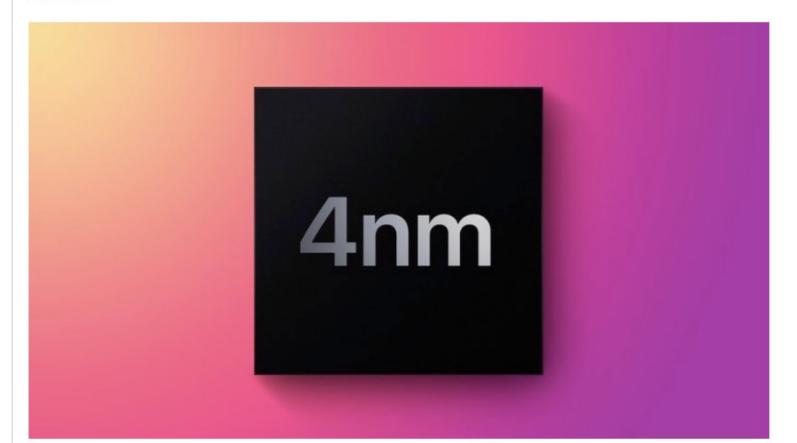


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#### **Apple Orders 4nm Chip Production for Next-Generation Macs**

Tuesday March 30, 2021 12:35 am PDT by Sami Fathi

Apple has booked the initial production capacity of 4nm chips with long-time supplier TSMC for its next-generation Apple silicon, according to industry sources cited in a new report today from *DigiTimes*.

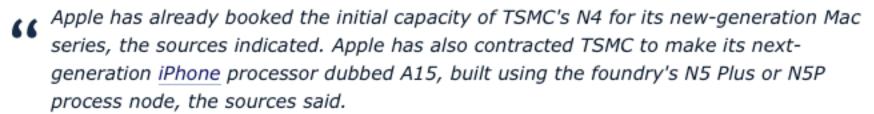




# Apple & TSMC



**COMP122** 



TSMC is expected to kick off production for Apple's A15 chip that will power the upcoming iPhone 13 series by the end of May, the sources noted.

The latest Apple silicon, the M1 chip, is the first of its kind in the industry based on the 5nm process. The A14 Bionic chip in the <u>iPad Air</u> and <u>iPhone 12</u> lineup is also based on the 5nm process. According to the report, Apple is already looking to the 4nm chip process for its next-generation Apple silicon.

A timeframe for when these new 4nm chips will debut isn't provided, but *DigiTimes* does report that TSMC will move to volume production of the new process in Q4 of 2021, ahead of the previously set 2022 timeframe. Additionally, Apple plans to use an enhanced version of the 5nm process for the A15 chip in the iPhone 13, with production set to get underway by the end of May.

The smaller process reduces the chips' actual footprint and provides better efficiency and performance. Apple's expected to launch <u>multiple new Macs</u> this year with more powerful Apple silicon chips; however, there's no indication that any will be based on the 4nm process.



# TSMC \$ Apple



**COMP122** 

# Taiwan Semiconductor asked for 2023 price increase from Apple, tech giant said no: report

Sep 28, 2022 11:23 AM ET | Taiwan Semiconductor Manufacturing Company Limited (TSM) | Chris Ciaccia, SA News Editor

Taiwan Semiconductor (NYSE:TSM) is slated to raise prices on its customers starting in 2023, but the company's largest customer, Apple (NASDAQ:AAPL), has reportedly told the global foundry no deal.

According to Chinese news outlet Economic Daily News, Taiwan Semiconductor (TSM) wanted to increase the price of the process for its 3 nm process by 3%, which may be used in the A17 chip in some of Apple's (AAPL) Mac computers and perhaps next year's iPhone. However, the tech giant refused and said no, the news outlet said, citing sources.

In May, it was reported that Taiwan Semiconductor Manufacturing (TSM) had started to tell some of its customers that it will raise its prices between 5% and 9%, starting next year, due to inflation concerns, rising costs and its expansion.

Cupertino, California-based Apple (AAPL) is Taiwan Semiconductor's (TSM) largest customer and some reports have suggested that it accounts for as much as 25% of the global foundry's annual revenue.

25%



### TSMC 3nm



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8-17-22

#### TSMC's Initial 3nm HVM Yield To Be Better Than Its 5nm

TSMC **N3e** is the HPC version for Intel, AMD, Nvidia, etc... The SoC companies Apple, Mediatek, will use **N3**. Please remember that TSMC sets expectations on the conservative so they don't disappoint. According to my sources N3 for Apple was frozen in December and the N3e process is now frozen with HVM starting in 1H 2023.

> Apple now in production (HVM) with 4nm



### Software



# Apple MacOS



### New Mac OS



COMP122

November 10, 2020





#### New Mac OS



COMP122

November 10, 2020

# Hardware-verified secure boot Automatic high-performance encryption macOS run-time protections





#### Software



# Apple Software ios 6-7-21



### WWDC 21



# iOS 15

