

Computer Organization (Architecture)

Lecture 1A: Intro

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Section



Numbers

Binary/Hex vs Decimal

Is there any point where using binary, hexadecimal or octal instead of decimal is better or worse from a computational standpoint?

...



Jeff Drobman

Lecturer at California State University, Northridge (2016–present) · Just now · 💰

Binary is the radix of choice due to digital logic being in 2 states. Decimal is usually binary encoded in BCD and has no benefit.

Binary is a base 2 number system. *Octal* is merely *representing* binary as 3-bit digits, and hex as 4-bit digits. Sort of like zooming in or out of same data.

Ordinals

COMP222

Powers of 2 <> 10: 10:3

Technical ordinals

$10^{(-24)}$	yacto
$10^{(-21)}$	zepto
$10^{(-18)}$	atto
$10^{(-15)}$	femto
$10^{(-12)}$	pico
$10^{(-9)}$	nano
$10^{(-6)}$	micro
$10^{(-3)}$	milli
$10^{(-2)}$	centi
$10^{(-1)}$	deci
$10^{(+1)}$	deka
$10^{(+2)}$	hecto
$10^{(+3)}/2^{(10)}$	kilo
$10^{(+6)}/2^{(20)}$	mega
$10^{(+9)}/2^{(30)}$	giga
$10^{(+12)}/2^{(40)}$	tera
$10^{(+15)}/2^{(50)}$	peta
$10^{(+18)}/2^{(60)}$	exa
$10^{(+21)}/2^{(70)}$	zetta
$10^{(+24)}/2^{(80)}$	yotta

Gazillions

$10^{(+6)}$	million
$10^{(+9)}$	billion
$10^{(+12)}$	trillion
$10^{(+15)}$	quadrillion
$10^{(+18)}$	quintillion
$10^{(+21)}$	sexillion
$10^{(+24)}$	septillion
$10^{(+27)}$	octillion
$10^{(+30)}$	nonillion
$10^{(+33)}$	decillion
$10^{(+36)}$	undecillion
$10^{(+39)}$	duodecillion
$10^{(+42)}$	tredecillion
$10^{(+45)}$	quattuordecillion
$10^{(+48)}$	quindecillion
$10^{(+51)}$	sexdecillion
$10^{(+54)}$	septendecillion
$10^{(+57)}$	octodecillion
$10^{(+60)}$	novemdecillion
$10^{(+63)}$	vigintillion
$10^{(+100)}$	googol
$10^{(+303)}$	centillion
$10^{(10^{(+100)})}$	googolplex

Ordinal	Power of 2	Power of 10	Actual
1K	2^{10}	10^3	1024
1M	2^{20}	10^6	1,048,576
1G	2^{30}	10^9	1.074×10^9
1T	2^{40}	10^{12}	1.0995×10^{12}

Name	2^n	M/G	Actual
byte	2^8	--	256
short	2^{16}	64K	65,536
integer	2^{32}	4B	4.3×10^9
long	2^{64}	16 Q	1.84×10^{19}
IPv6	2^{128}	340 uD	3.4×10^{38}

GiB/TiB ($2^{30}/2^{40}$)

Decimal	Abbreviation	Value	Binary term	Abbreviation	Value	% Larger
kilobyte	KB	10^3	kibibyte	KiB	2^{10}	2%
megabyte	MB	10^6	mebibyte	MiB	2^{20}	5%
gigabyte	GB	10^9	gibibyte	GiB	2^{30}	7%
terabyte	TB	10^{12}	tebibyte	TiB	2^{40}	10%
petabyte	PB	10^{15}	pebibyte	PiB	2^{50}	13%
exabyte	EB	10^{18}	exbibyte	EiB	2^{60}	15%
zettabyte	ZB	10^{21}	zebibyte	ZiB	2^{70}	18%
yottabyte	YB	10^{24}	yobibyte	YiB	2^{80}	

Actual
1024
1,048,576
1.074×10^9
1.0995×10^{12}

Ordinal	Power of 2	Power of 10	Actual
1K	2^{10}	10^3	1024
1M	2^{20}	10^6	1,048,576
1G	2^{30}	10^9	1.074×10^9
1T	2^{40}	10^{12}	1.0995×10^{12}

Signed Numbers

Binary	Unsigned	Sign		Two's Complement
		Magnitude	Excess-127	
00000000	0	0	-127	0
00000001	1	1	-126	1
⋮	⋮	⋮	⋮	⋮
01111110	126	126	-1	126
01111111	127	127	0	127
10000000	128	-0	1	-128
10000001	129	-1	2	-127
⋮	⋮	⋮	⋮	⋮
11111110	254	-126	127	-2
11111111	255	-127	128	-1

ASCII Codes

Binary, hexadecimal, and decimal equivalents for each character in "Hello World"

Character	Binary	Hexadecimal	Decimal
H	01001000	48	72
e	01100101	65	101
l	01101100	6C	108
l	01101100	6C	108
o	01101111	6F	111
	00100000	20	32
W	01010111	57	87
o	01101111	6F	111
r	01110010	62	98
l	01101100	6C	108
d	01100100	64	100
NUL	00000000	00	0

Section



Logic

Computer Architecture

4-Layer Stack Model

PCB Board

Chipsets, Chiplets and Sockets

Macro-arch

System arch – Cores, caches

ISA

Instructions (Primitives)
Software Interface

Computer Org

Execution Units
❖ ALU, ICU, Reg

122

Micro-architecture

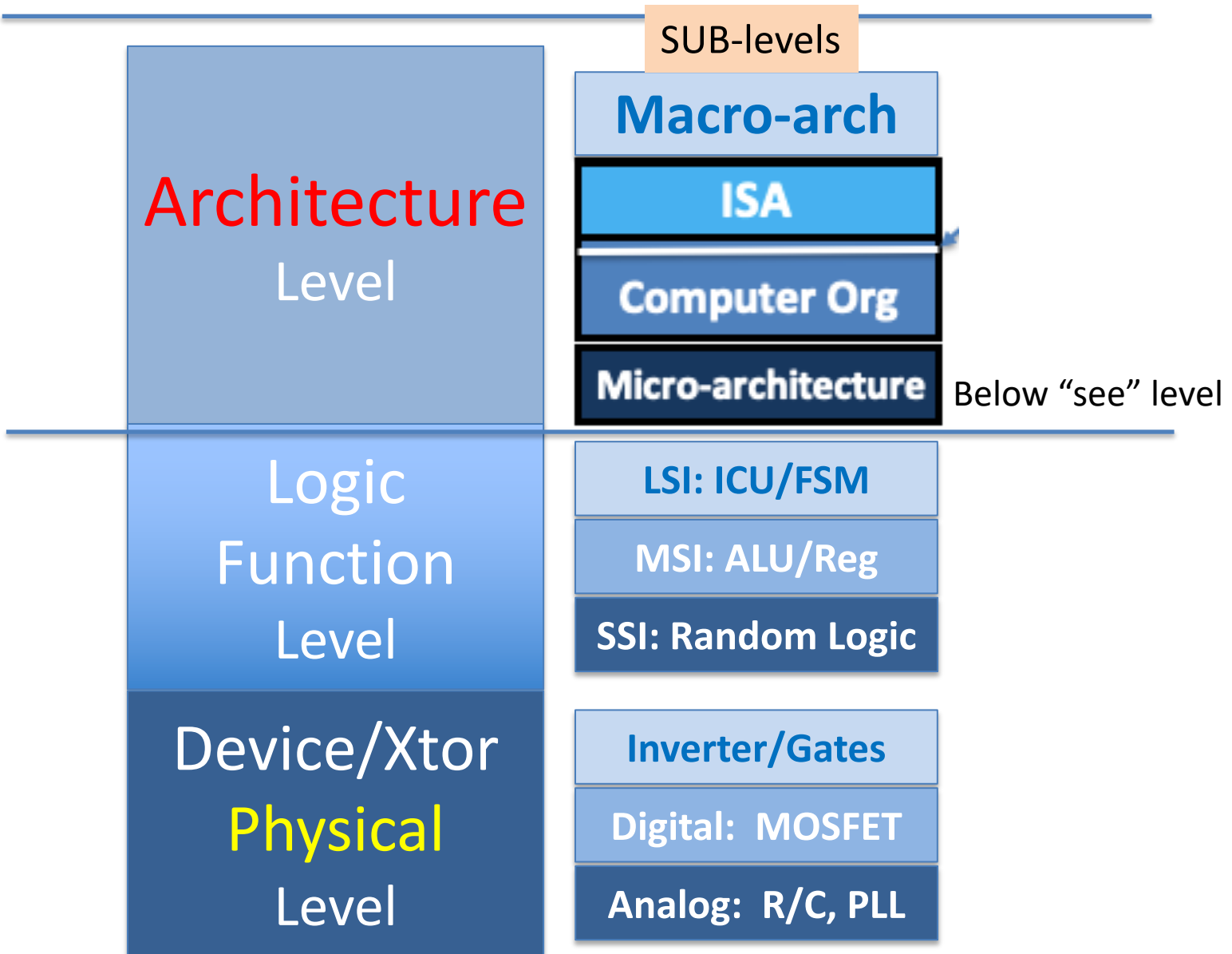
Low-level execution
❖ Pipelines, threads
❖ scheduling
❖ branch prediction

Below “see” level

222

Architecture
Level

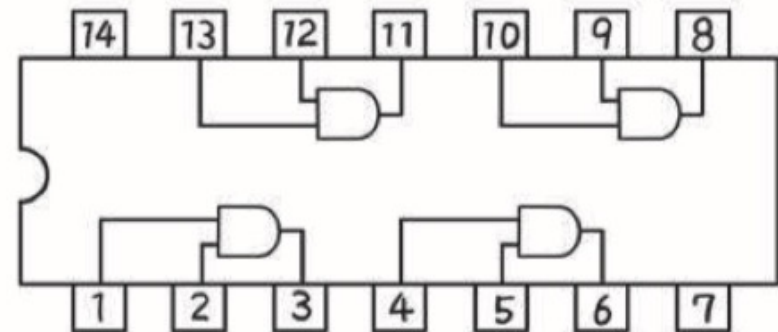
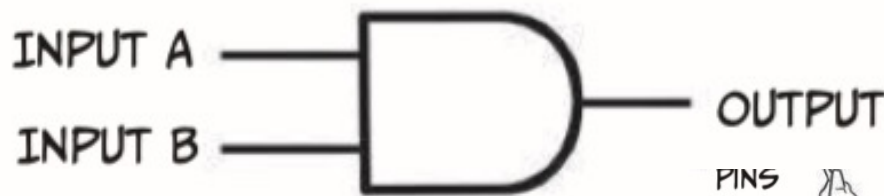
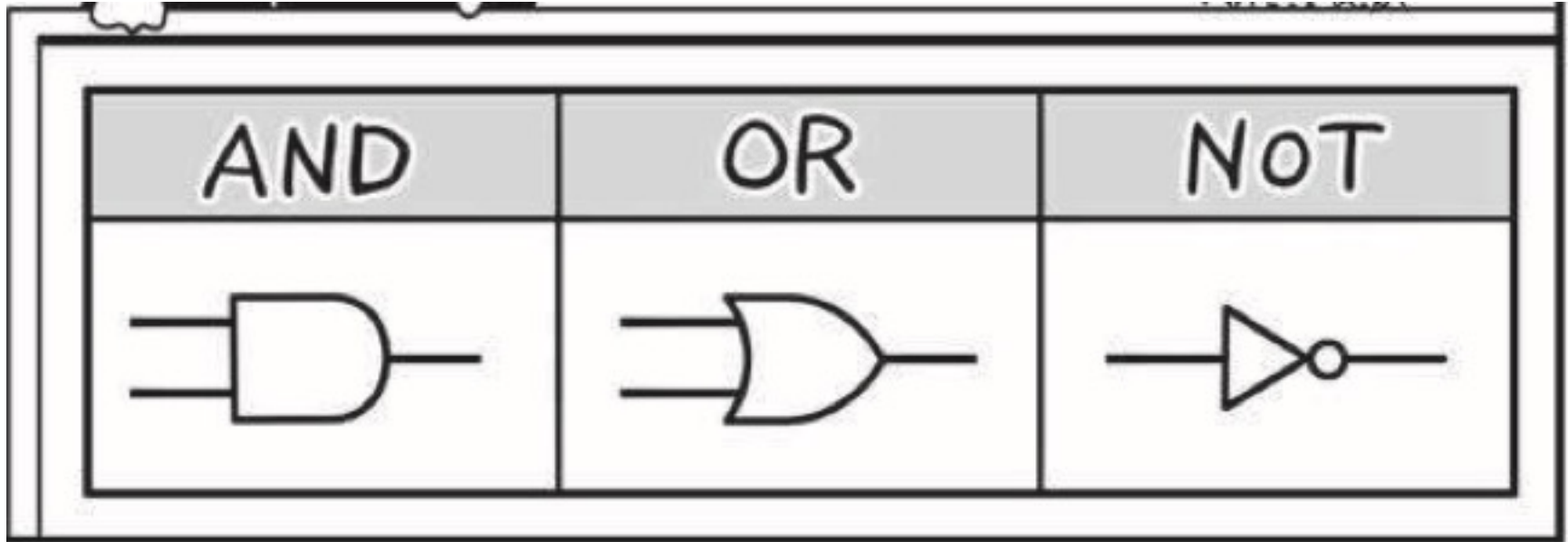
Transistors to Chips: Levels



Logic Universal Set

Manga Guide

https://nostarch.com/download/MangaGuidetoMicroprocessors_sample_Chapter2.pdf



THIS IS A LABELED DIAGRAM
OF THE INSIDE OF THIS CHIP.

PINS



Logic Gates: Polarity

DeMorgan's Law

Manga Guide



That's it! It also means that we can use De Morgan's laws to show our circuits in different ways. Using this technique, it's easy to simplify schematics when necessary.



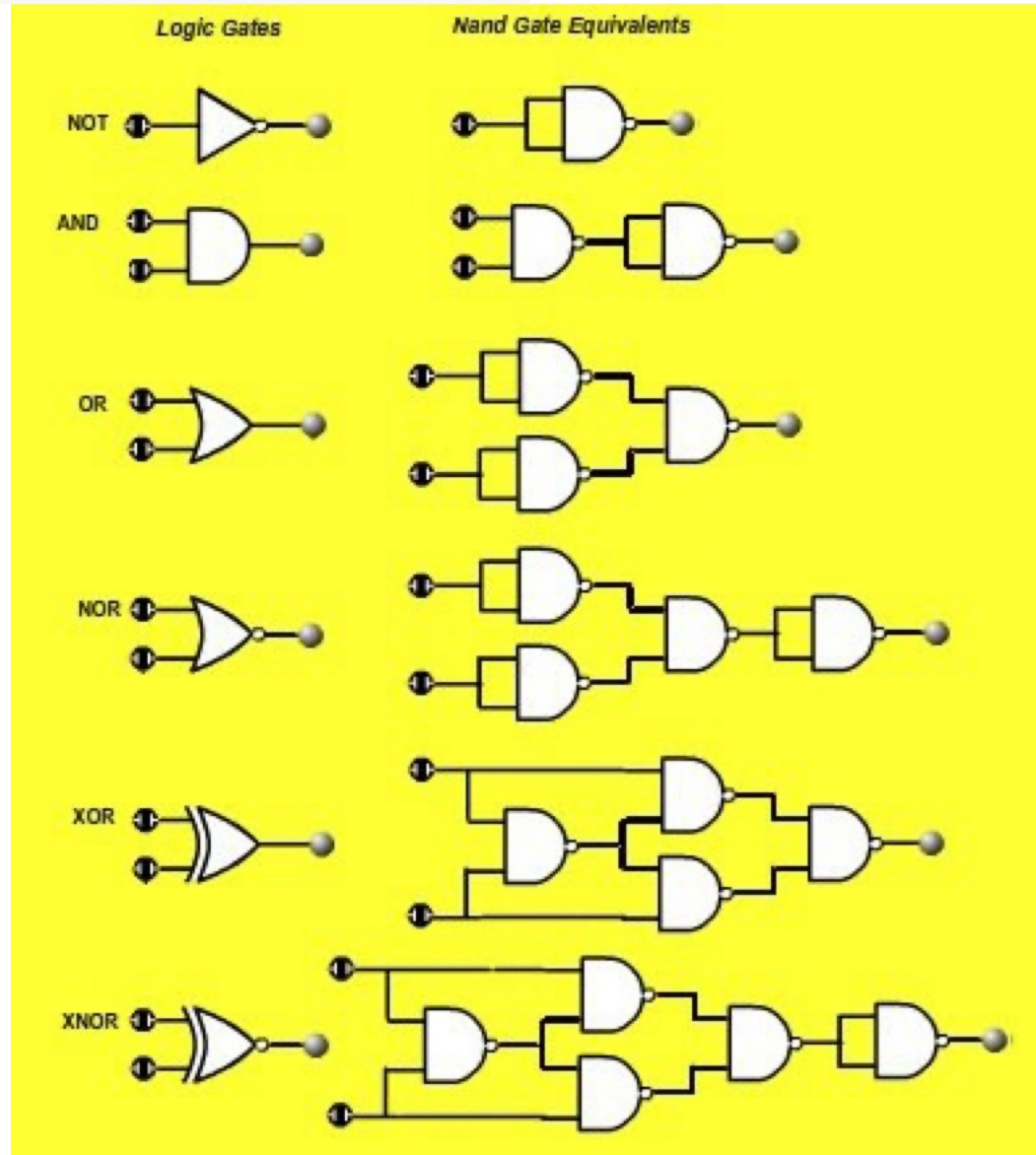
BOTH OF THESE ARE NAND GATES!



BOTH OF THESE ARE NOR GATES!

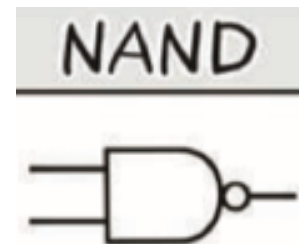
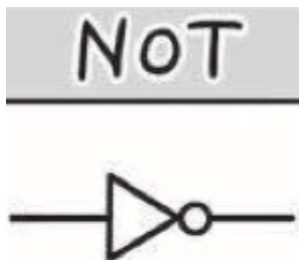
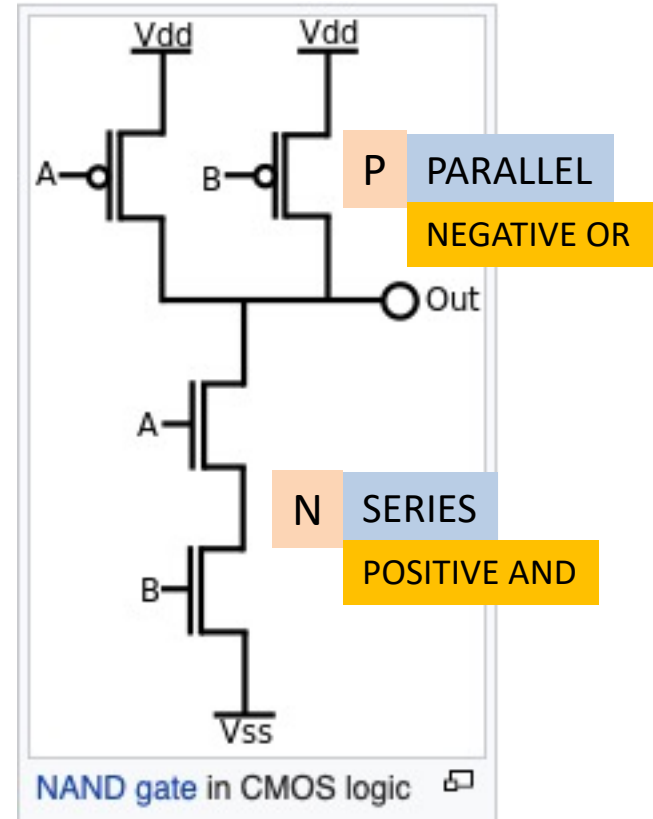
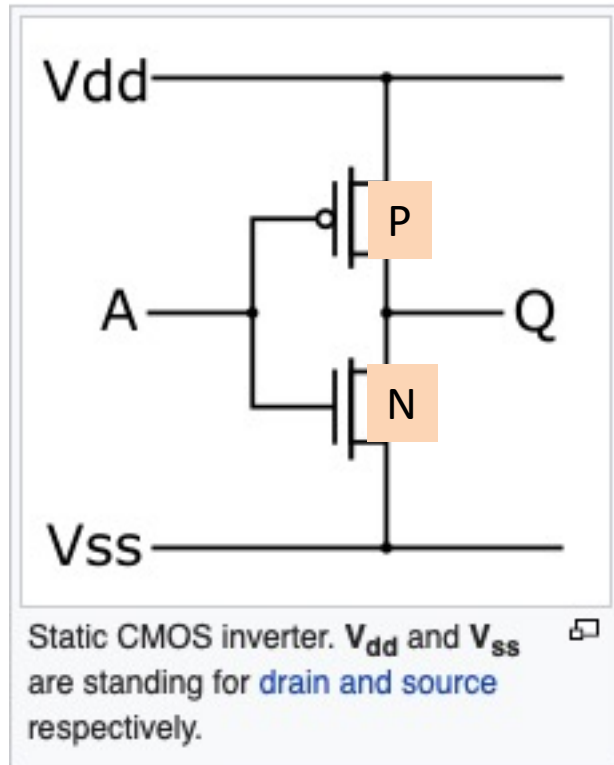


NAND Gates

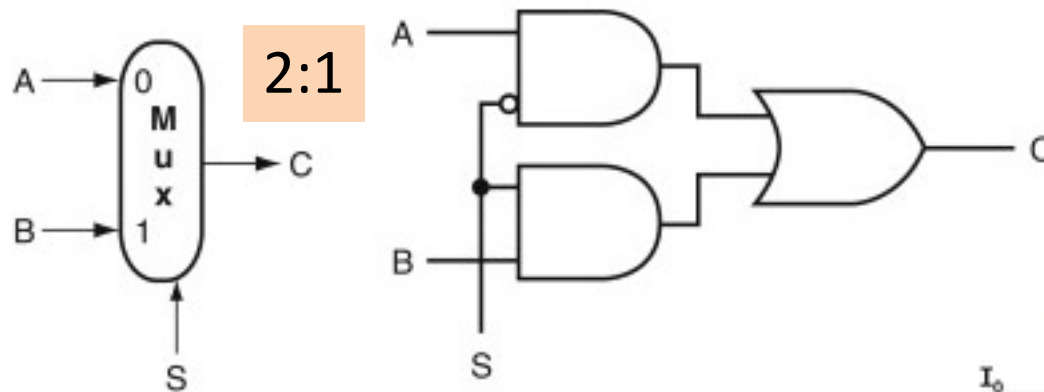


CMOS Gates

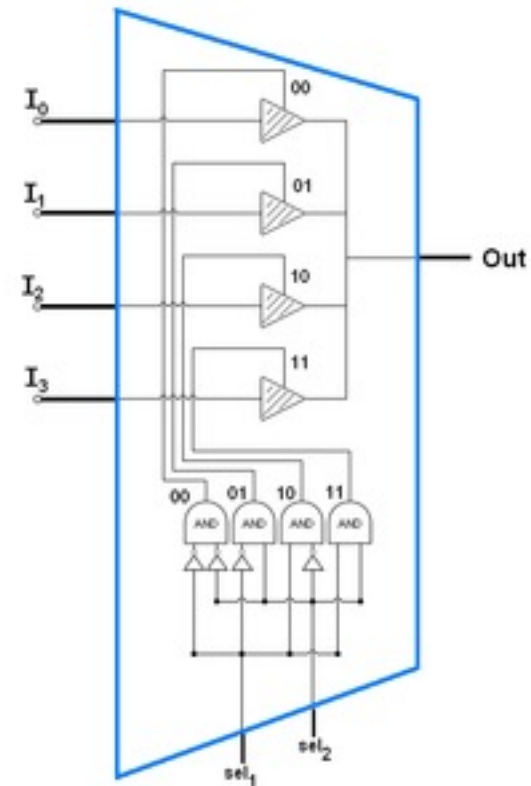
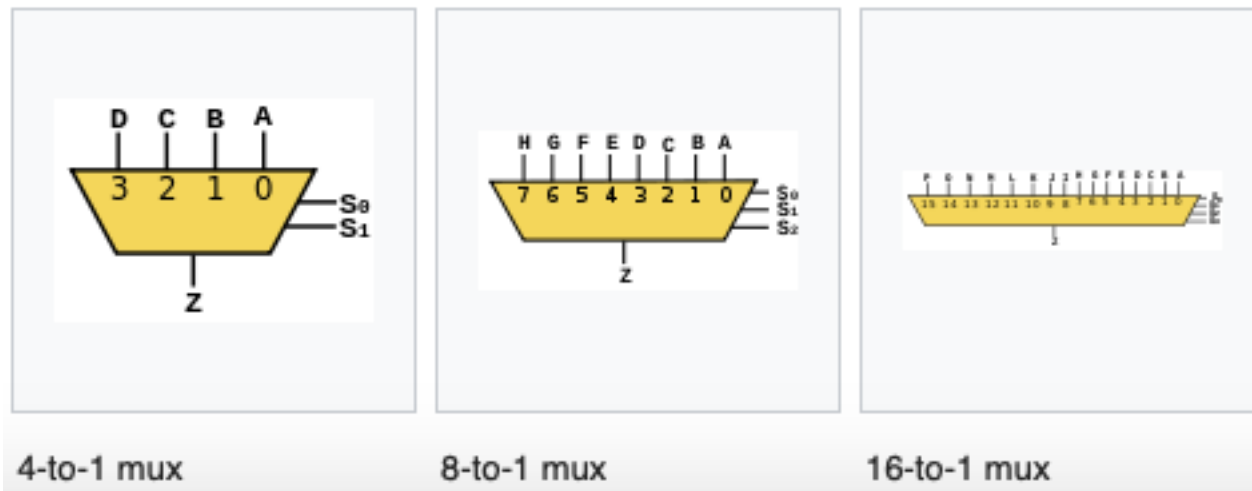
MOSFET



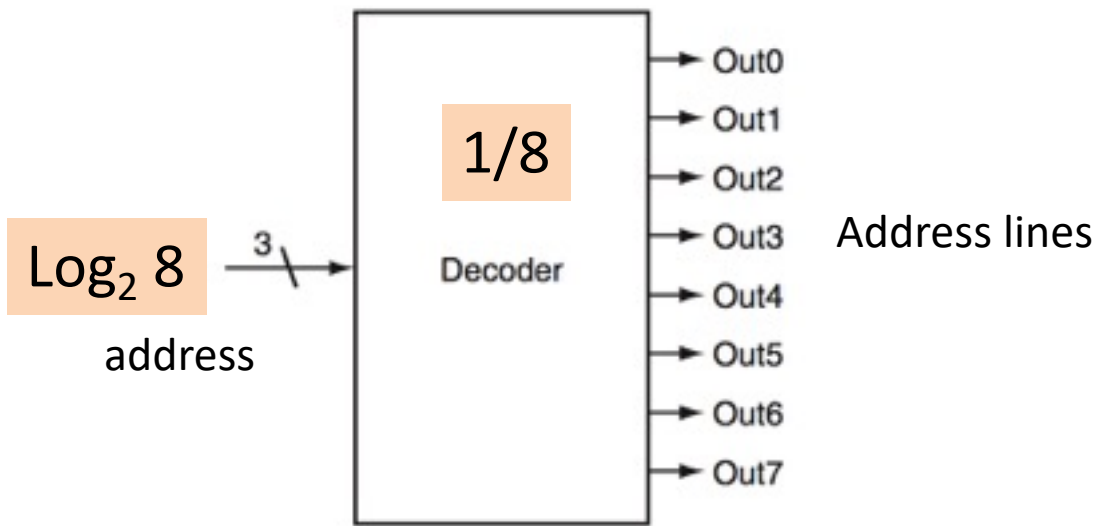
MUX



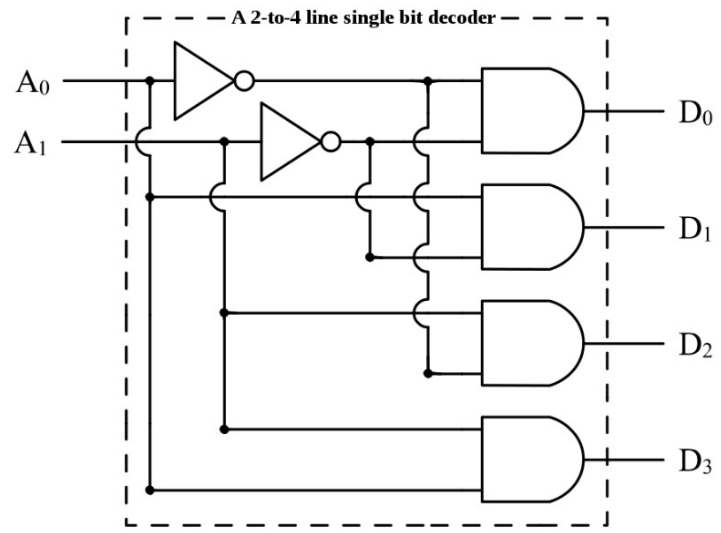
The following 4-to-1 multiplexer is constructed from 3-state buffers and AND gates



Decoder



a. A 3-bit decoder



Truth Table

A_1	A_0	D_3	D_2	D_1	D_0
0	0	0	0	0	1
0	1	0	0	1	0
1	0	0	1	0	0
1	1	1	0	0	0

Minterm Equations

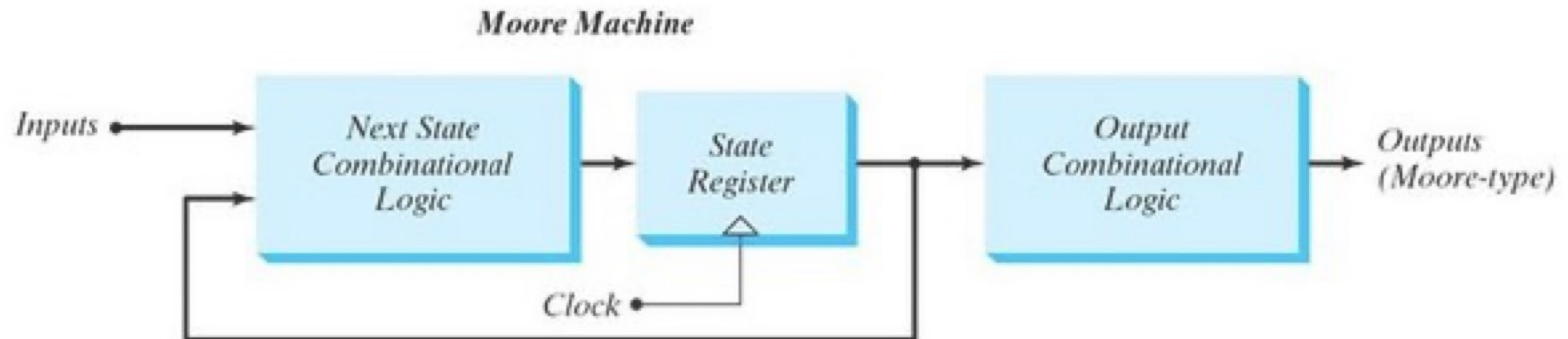
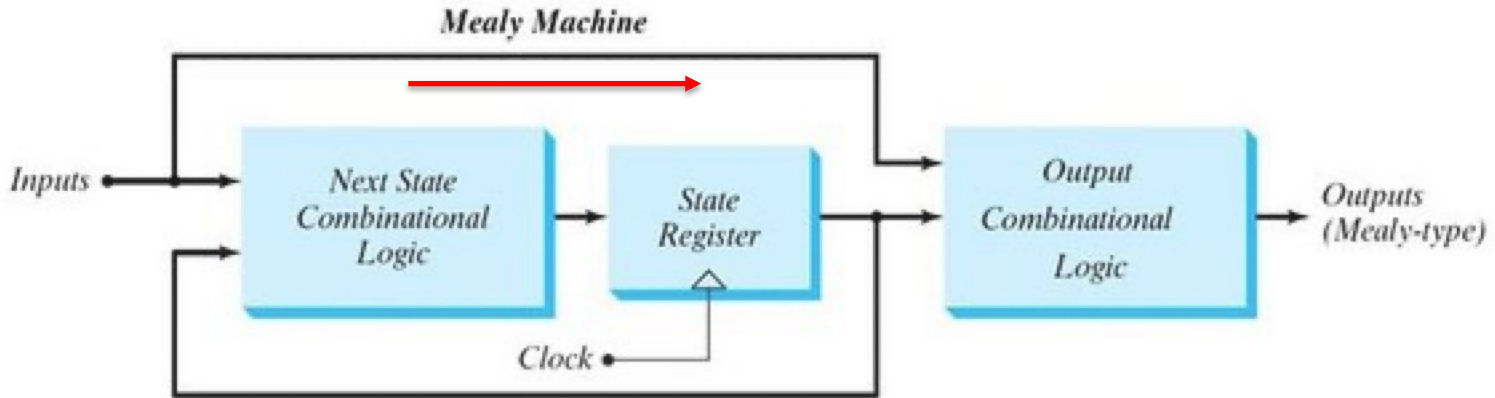
$$D_0 = \overline{A_1} \cdot \overline{A_0}$$

$$D_1 = \overline{A_1} \cdot A_0$$

$$D_2 = A_1 \cdot \overline{A_0}$$

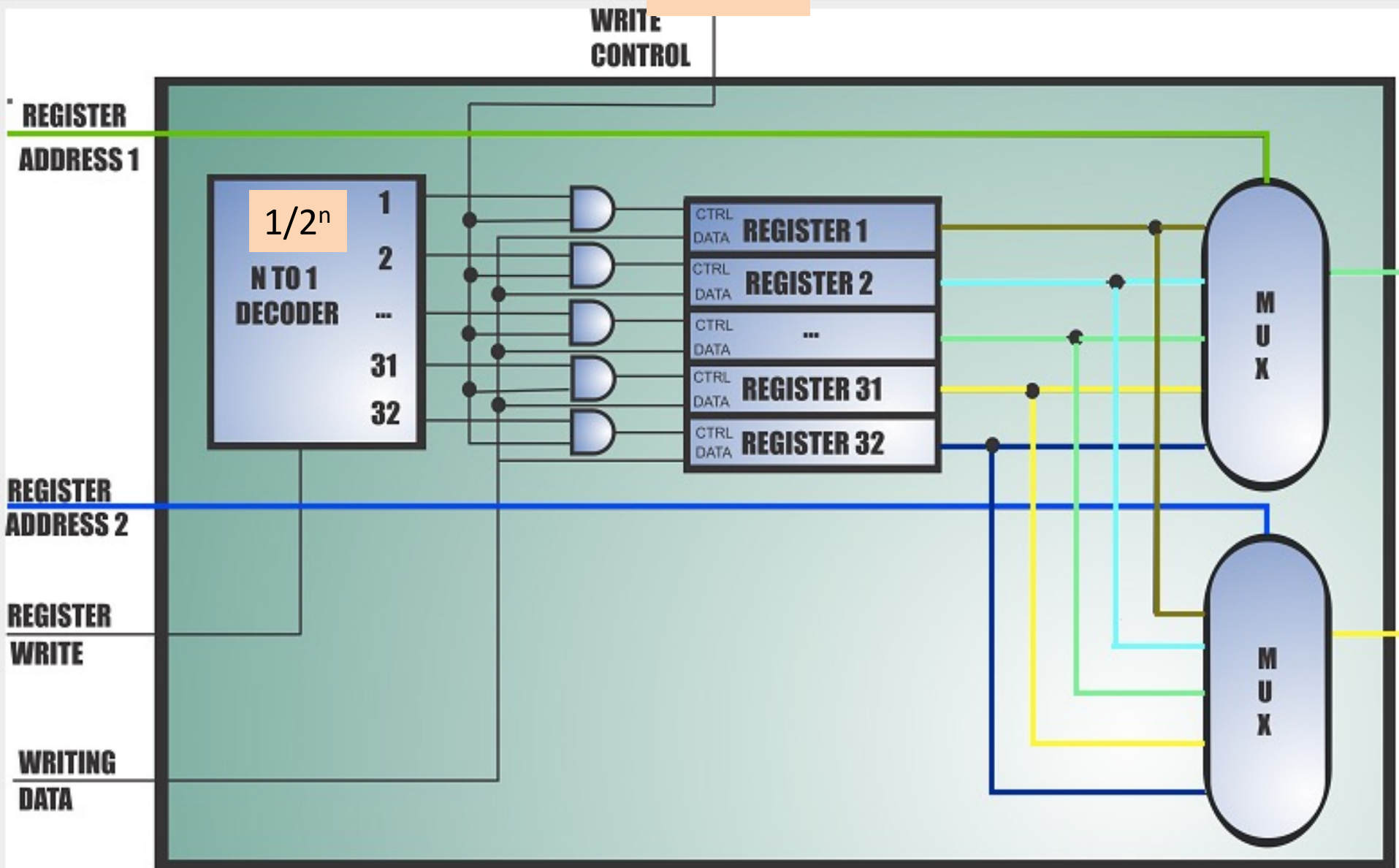
$$D_3 = A_1 \cdot A_0$$

Mealy-Moore FSM



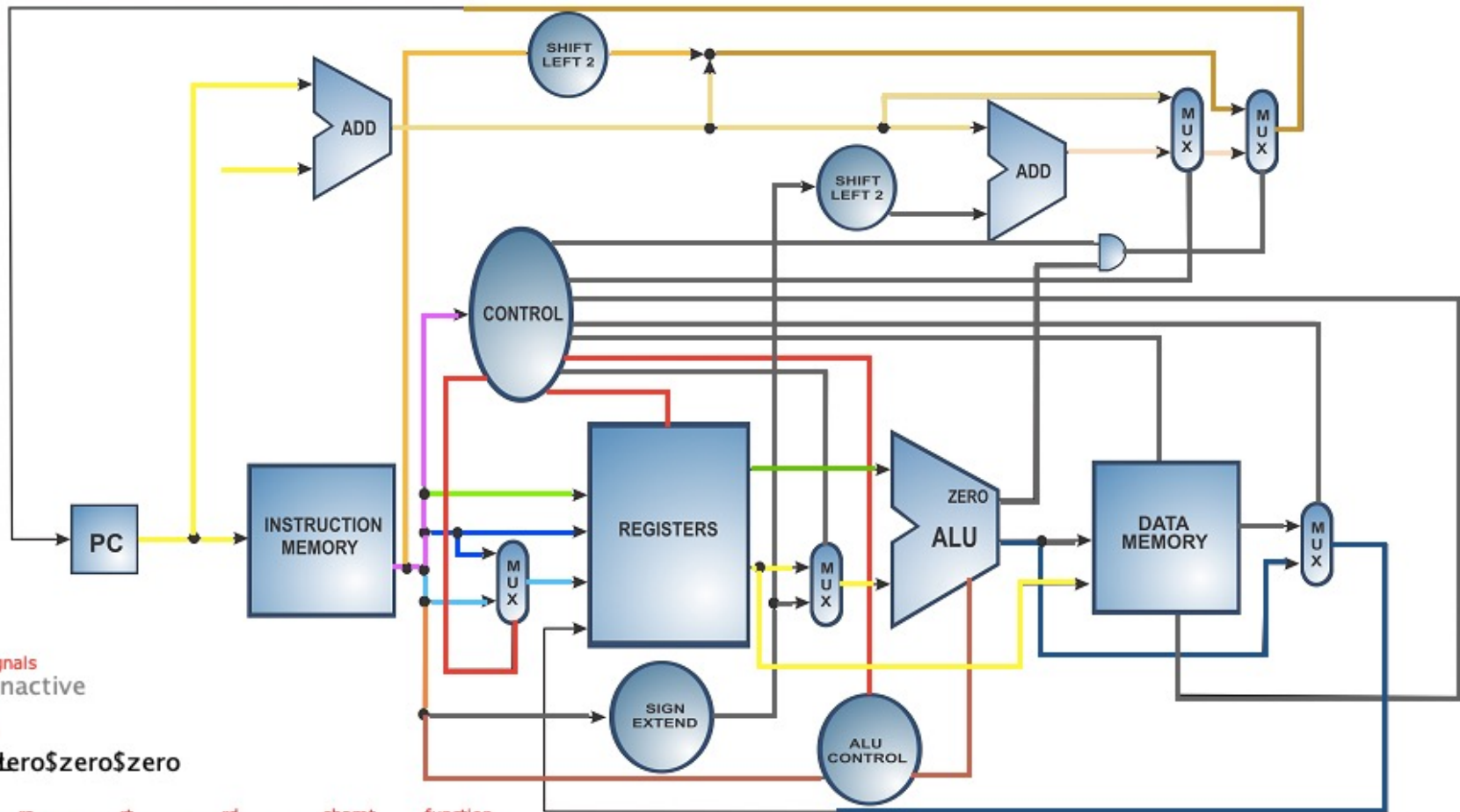
Register File on MARS

Decoders



MIPS on MARS

REGISTER TYPE INSTRUCTION



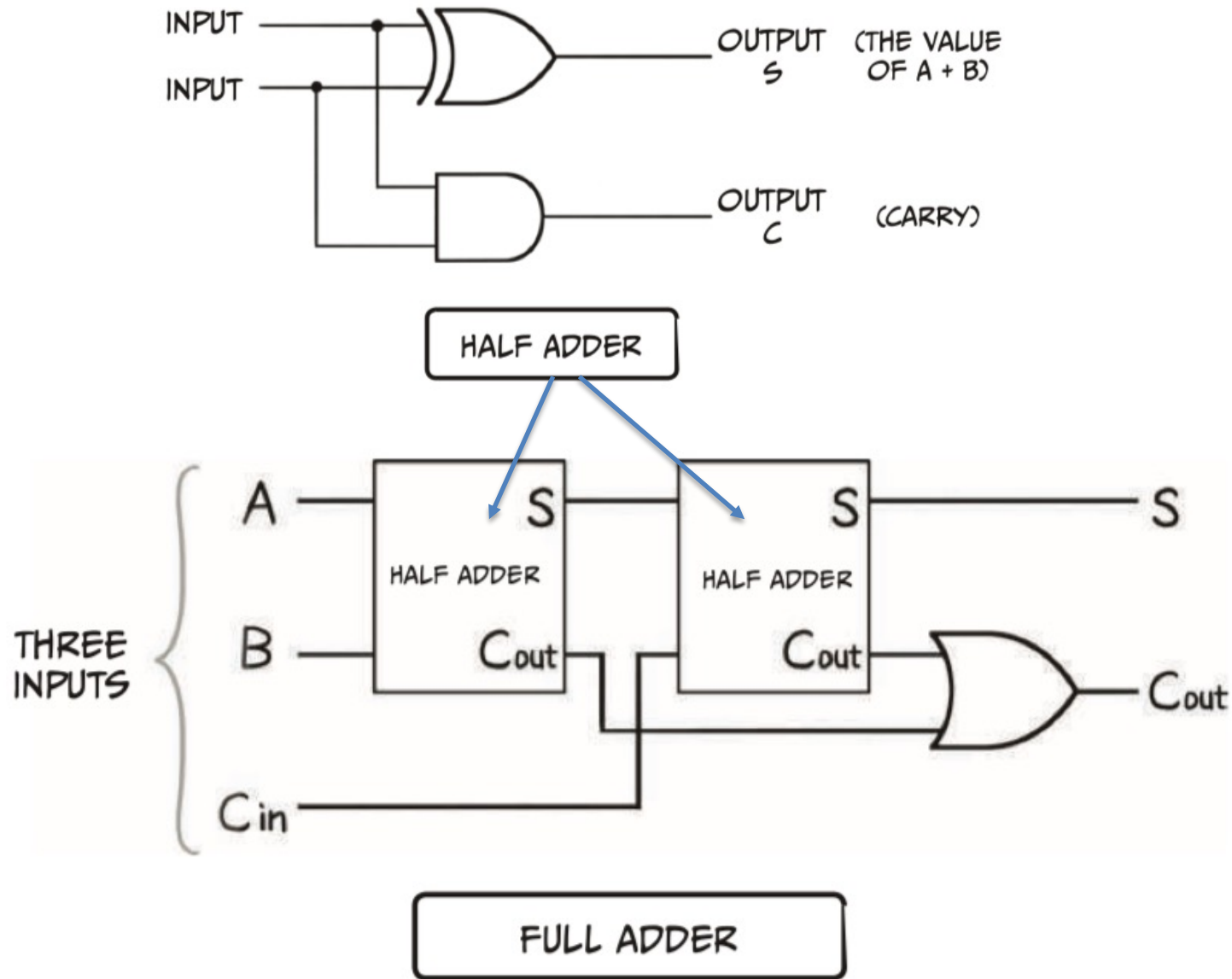
Control Signals
Active Inactive

Instruction
SYSCALL zero\$zero\$zero

opcode	rs	rt	rd	shamt	function
000000	00000	00000	00000	00000	001100

To see details of control units and register bank click inside the functional block

Adders



Multiplication



Jeff Drobman · Just now

multiplication is usually done completely in hardware, via a 2D array of " $XY(i) + C$ " multiplier modules, whereby each row generates a partial product of the next signed digit of the multiplier times the multiplicand. shifting occurs in the hardware placement of each row. this array can also be pipelined, so multiple operations can be performed in sequential concurrency.

(See the 1971 **Am2505** 2x4-bit multiplier slice, and my personal MS thesis.)

Am2505 Multiplier

COMP222

Drobman MS Thesis

Bit-slice

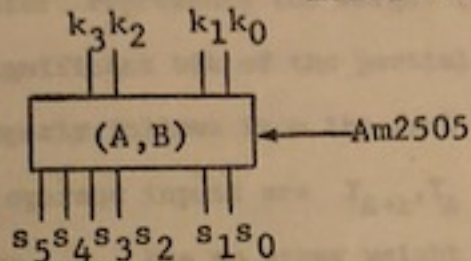
1971-80

Notation: (from [1], [15], [16])

multiplier pair = Y_{A+1}, Y_A

multiplicand group = $X_{B+3}, X_{B+2}, X_{B+1}, X_B$

"module designator" = (A,B)



2x4-bit slices



8-bit x 8-bit multiply

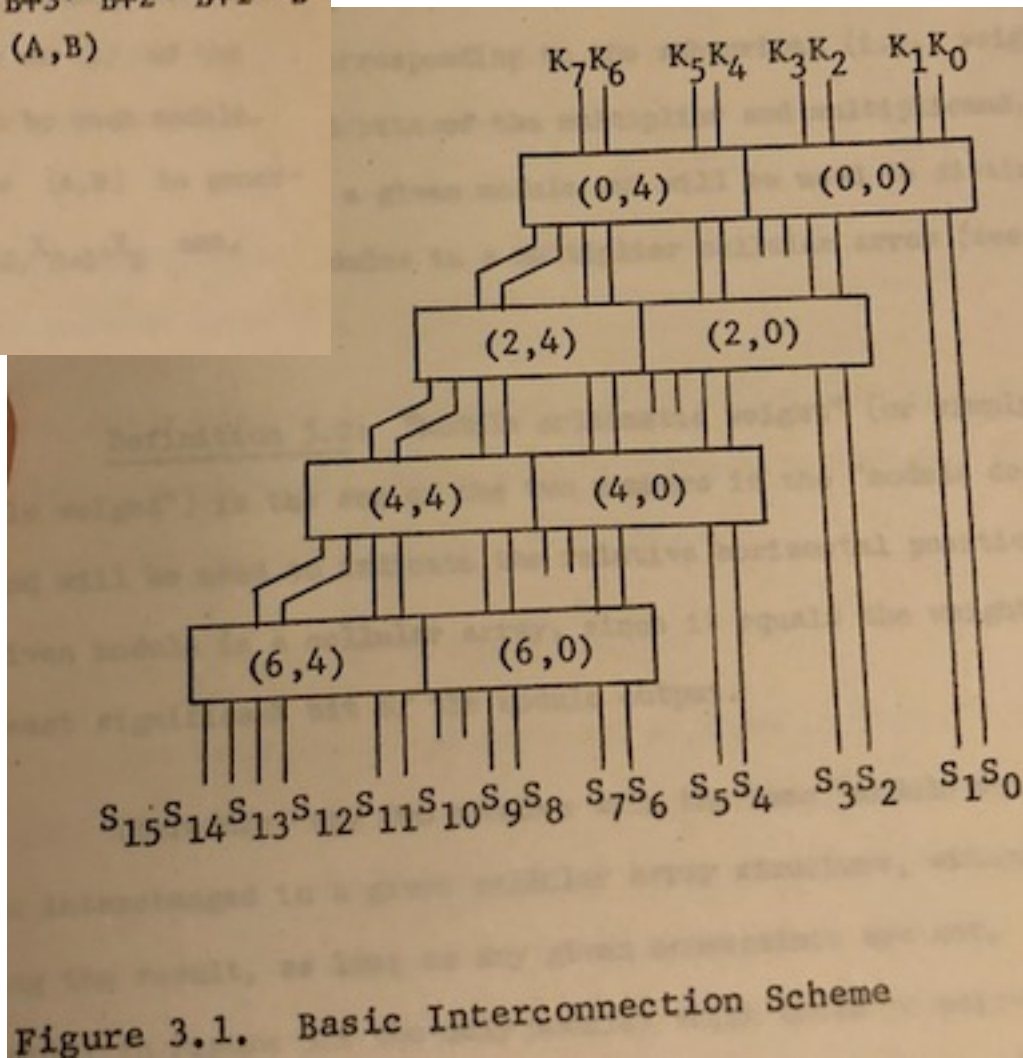


Figure 3.1. Basic Interconnection Scheme

Division

Non-Restoring Div

How do calculators calculate binary division?



Jeff Drobman, Lecturer at California State University, Northridge (2016-present)

Answered just now

the most common division algorithm used in the past was "non-restoring". but there are others, as listed in Wikipedia:

"Division algorithms fall into two main categories: slow division and fast division. Slow division algorithms produce one digit of the final quotient per iteration. Examples of slow division include [restoring](#) [↗](#), non-performing restoring, [non-restoring](#) [↗](#), and [SRT](#) [↗](#) division. Fast division methods start with a close approximation to the final quotient and produce twice as many digits of the final quotient on each iteration. [Newton-Raphson](#) [↗](#) and [Goldschmidt](#) [↗](#) algorithms fall into this category."

Section

VLSI vs ASIC vs FPGA

VLSI vs ASIC vs FPGA

➤ 3 options for chips

❖ VLSI

❑ **Fully** Custom

- *Building blocks:* Designer IP (all levels)
- *Tools:* Licensed from EDA vendors

❖ ASIC

❑ **Semi** Custom

- *Building blocks:* Manufacturer IP
- *Tools:* Provided by Mfr (ASIC vendor)

❖ FPGA

❑ **Programmable** Custom (SRAM)

- *Building blocks:* logic gates (NAND, NOR)
- *Tools:* Lab Programmers, software

FPGA vs PLD

❖ FPGA

- ❑ **Field Programmable** (SRAM based)
 - *Building blocks:* logic gates (NAND, NOR)
 - *Tools:* Lab Programmers, software

❖ PLD

- ❑ **PLA**
 - AMD *Mach* family (merged with PAL)
- ❑ **PAL**
 - MMI invented, bought by AMD
 - AMD spun off as Vantis (bought by Lattice)
- ❑ **CPLD**
 - *Complex* PLD

Programmable Logic – FPGA

From Wikipedia, the free encyclopedia

FPGAs

FPGA

A **field-programmable gate array (FPGA)** is an integrated circuit designed to be configured by a customer or a designer after manufacturing – hence the term *field-programmable*. The FPGA configuration is generally specified using a hardware description language (HDL), similar to that

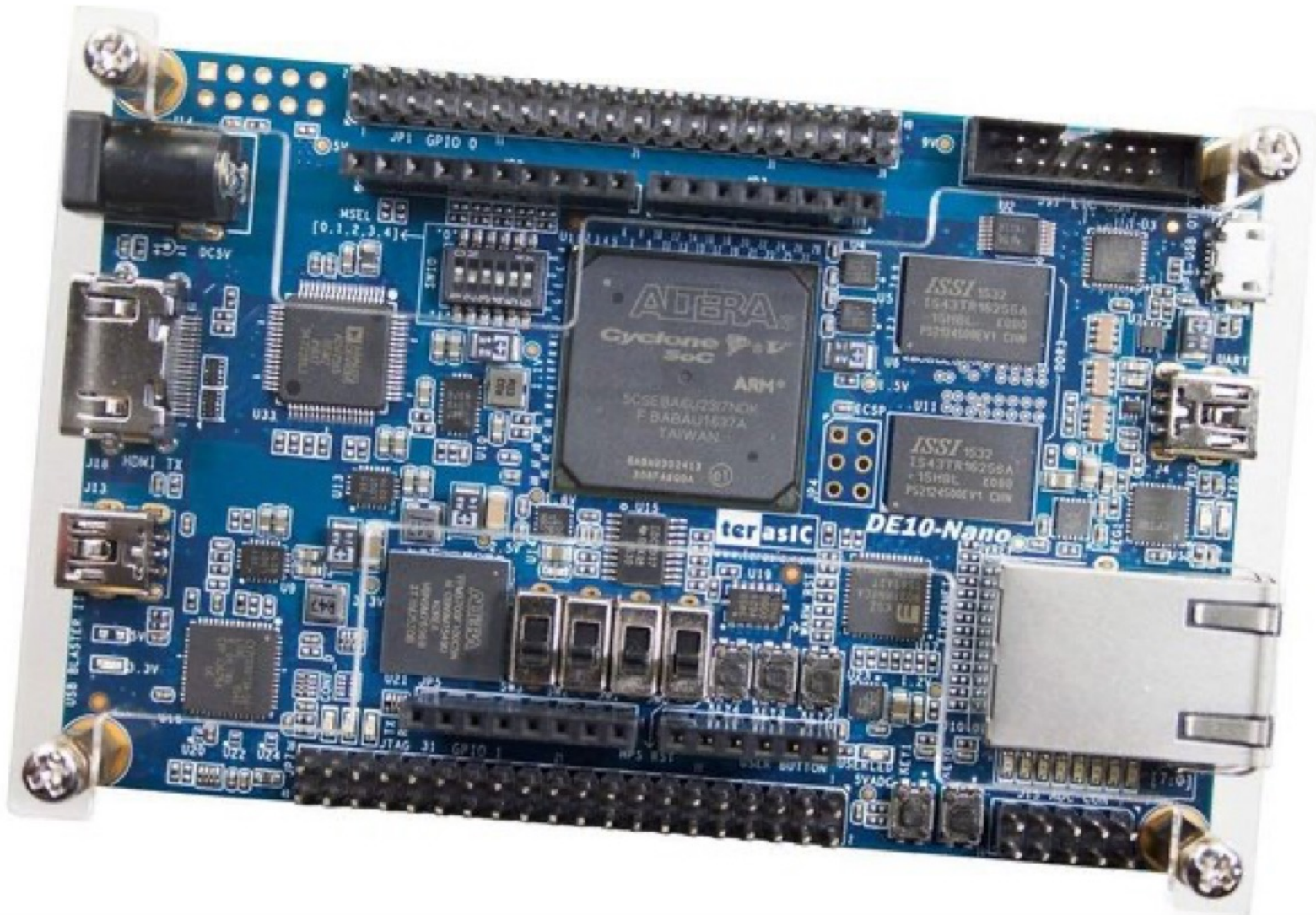
HDL



Intel



For example this is generic gaming console built using single FPGA:



CPU/GPU vs ASIC

Quora

What is the difference between ASICs and GPUs/CPU's?



Jeff Drobman

Lecturer at California State University, Northridge (2016–present) · Just now

in general, ASICs use smaller functional building blocks than “cores”, which are much larger, complete units. ASIC’s are “application specific” — to a single application, and are not *programmable*.

Whereas CPU and GPU cores are software *programmable* — so *general* purpose (not application specific).

Section

Chip Design Transistors

Making Transistors

Doping **P** & **N**
+ -

How does impurity mix with a material to form positive and negative semiconductor material? ...



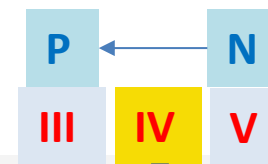
Jeff Drobman

Lecturer at California State University, Northridge (2016–present) · Just now · 💰

P and N dopants (III and V valence) are chemically *diffused* as gases into the silicon substrate in ovens. sometimes *ion implantation* is used instead.

Silicon Semi

Holes Donor

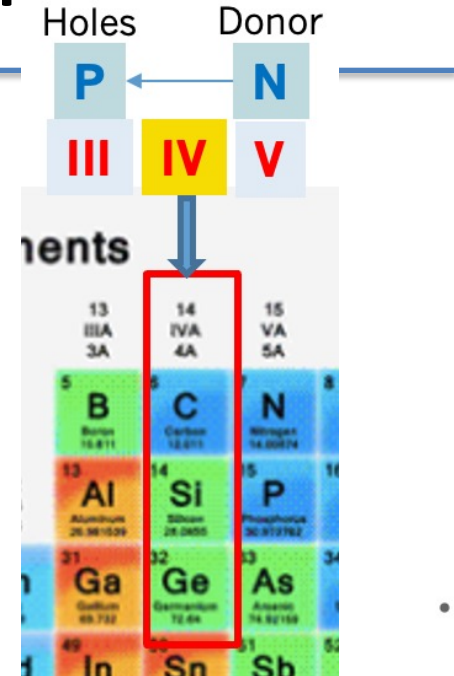
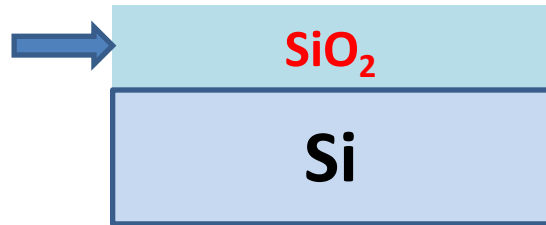


Periodic Table of the Elements

The image shows a standard periodic table of elements. A red rectangular box highlights the element Germanium (Ge), which is located in the 4th period and 14th group. A blue arrow points downwards from the top of the page towards the highlighted element. The table includes element symbols, names, atomic numbers, and atomic weights. It also features color-coded blocks for different groups of elements and labels for the Lanthanide and Actinide series at the bottom.

1 1A 11A																	18 VIII 8A														
1 H Hydrogen 1.0079	2 He Helium 4.0026																	13 III A 3A	14 IV A 4A	15 V A 5A	16 VI A 6A	17 VII A 7A	18 VIII 8A								
3 Li Lithium 6.941	4 Be Beryllium 9.0122																	5 B Boron 10.811	6 C Carbon 12.011	7 N Nitrogen 14.0031	8 O Oxygen 15.999	9 F Fluorine 18.9984	10 Ne Neon 20.1797								
11 Na Sodium 22.98976	12 Mg Magnesium 24.305	3 III B 3B	4 IV B 4B	5 V B 5B	6 VI B 6B	7 VII B 7B	8 VIII 8			9 VIII 9	10 VIII 10	11 IB 1B	12 IIB 2B	13 Al Aluminum 26.9815	14 Si Silicon 28.0855	15 P Phosphorus 30.9738	16 S Sulfur 32.06	17 Cl Chlorine 35.453	18 Ar Argon 39.948												
19 K Potassium 39.0983	20 Ca Calcium 40.078	21 Sc Scandium 44.9559	22 Ti Titanium 47.88	23 V Vanadium 50.9415	24 Cr Chromium 51.9961	25 Mn Manganese 54.938	26 Fe Iron 55.847	27 Co Cobalt 58.9332	28 Ni Nickel 58.6934	29 Cu Copper 63.546	30 Zn Zinc 65.38	31 Ga Gallium 69.723	32 Ge Germanium 72.64	33 As Arsenic 74.9216	34 Se Selenium 78.96	35 Br Bromine 79.904	36 Kr Krypton 83.80														
37 Rb Rubidium 85.4678	38 Sr Strontium 87.62	39 Y Yttrium 88.90585	40 Zr Zirconium 91.224	41 Nb Niobium 92.90638	42 Mo Molybdenum 95.94	43 Tc Technetium 98.9062	44 Ru Ruthenium 101.07	45 Rh Rhodium 102.9055	46 Pd Palladium 106.42	47 Ag Silver 107.8682	48 Cd Cadmium 112.411	49 In Indium 114.818	50 Sn Tin 118.71	51 Sb Antimony 121.76	52 Te Tellurium 127.6	53 I Iodine 126.90447	54 Xe Xenon 131.29														
55 Cs Cesium 132.90545	56 Ba Barium 137.327	57-71 Lanthanide Series		72 Hf Hafnium 178.49	73 Ta Tantalum 180.9479	74 W Tungsten 183.85	75 Re Rhenium 186.207	76 Os Osmium 190.23	77 Ir Iridium 192.22	78 Pt Platinum 195.08	79 Au Gold 196.9665	80 Hg Mercury 200.59	81 Tl Thallium 204.3833	82 Pb Lead 207.2	83 Bi Bismuth 208.98039	84 Po Polonium [209]	85 At Astatine [210]	86 Rn Radon [222]													
87 Fr Francium 223.017	88 Ra Radium 226.0254	89-103 Actinide Series		104 Rf Rutherfordium [261]	105 Db Dubnium [262]	106 Sg Seaborgium [266]	107 Bh Bohrium [264]	108 Hs Hassium [277]	109 Mt Meitnerium [268]	110 Ds Darmstadtium [271]	111 Rg Roentgenium [272]	112 Cn Copernicium [285]	113 Uut Ununtrium [284]	114 Uuq Ununquadium [289]	115 Uup Ununpentium [288]	116 Uuh Ununhexium [286]	117 Uus Ununseptium [286]	118 Uuo Ununoctium [294]													
Lanthanide Series		57 La Lanthanum 138.9055	58 Ce Cerium 140.116	59 Pr Praseodymium 140.90768	60 Nd Neodymium 144.24	61 Pm Promethium 144.9127	62 Sm Samarium 150.36	63 Eu Europium 151.964	64 Gd Gadolinium 157.25	65 Tb Terbium 158.92534	66 Dy Dysprosium 162.50	67 Ho Holmium 164.93032	68 Er Erbium 167.26	69 Tm Thulium 168.93421	70 Yb Ytterbium 173.04	71 Lu Lutetium 174.967															
Actinide Series		89 Ac Actinium 227.0278	90 Th Thorium 232.0377	91 Pa Protactinium 231.03688	92 U Uranium 238.02891	93 Np Neptunium 237.04817	94 Pu Plutonium 244.0642	95 Am Americium 243.0614	96 Cm Curium 247.0713	97 Bk Berkelium 247.0713	98 Cf Californium 251.0788	99 Es Einsteinium [252]	100 Fm Fermium [257]	101 Md Mendelevium [258]	102 No Nobelium [259]	103 Lr Lawrencium [260]															
		Alkali Metal			Alkaline Earth			Transition Metal			Basic Metal			Semimetal			Nonmetal			Halogen			Noble Gas			Lanthanides			Actinides		

Silicon Semi



Quora



Chris Bevis · Follow

Lives in Silicon Valley (1997–present) · Updated Sep 9

Related Why is silicon mostly used in tech companies than germanium?

The earliest semiconductor devices were made of germanium. This started to change when the first planar IC's were developed. It is easy to grow a stable, insulating oxide film on silicon but not on germanium, so silicon was the material of choice. One of the key breakthroughs in silicon processing was made by Andy Grove and a colleague: the Grove-Deal model of SiO₂ growth kinetics.

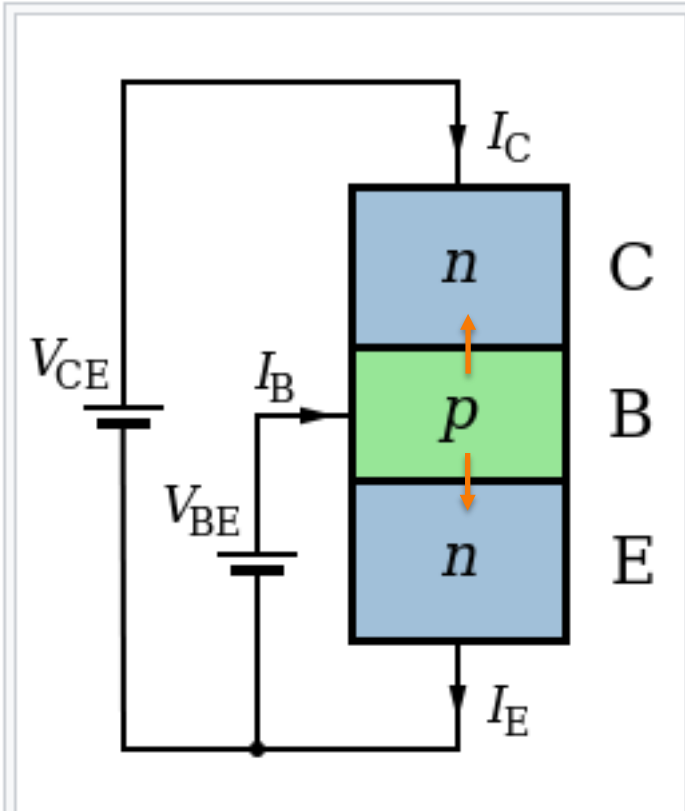
These days, most advanced devices have channels made of an alloy of Si and Ge doped with boron (SiGeB). The percentage of Si and Ge is carefully controlled and varied over the height of the channel to produce strain which enhances the mobility of electrons or holes.

Bipolar Transistors

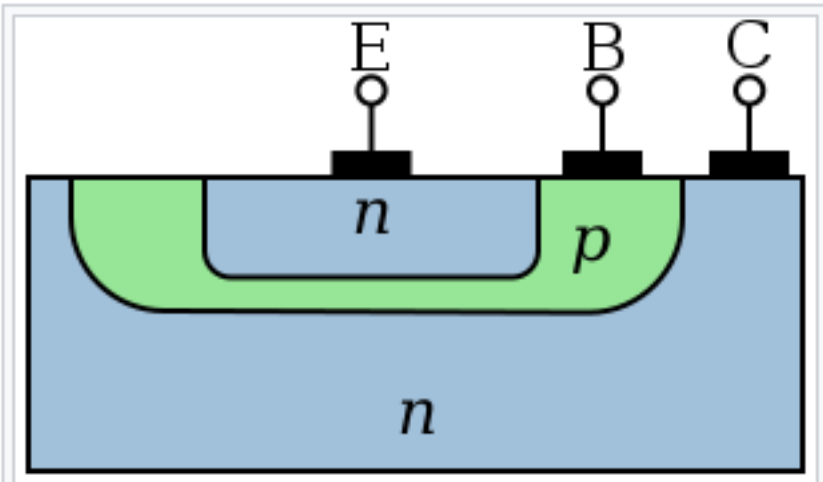
BJT

PLANAR

Structure [\[edit\]](#)



Structure and use of NPN transistor. Arrow according to schematic.



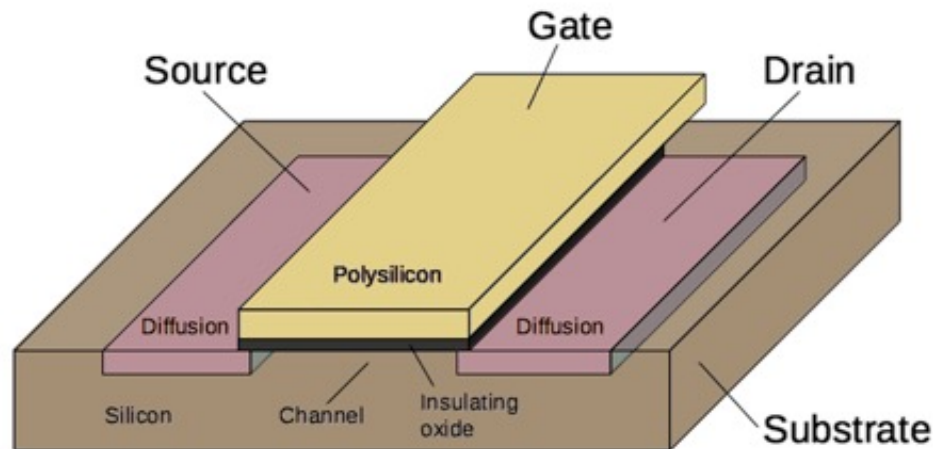
Simplified cross section of a planar *NPN* bipolar junction transistor

Physical Level: MOSFET

Device/Xtor
Physical
Level

Inverter/Gates

Digital: MOSFET

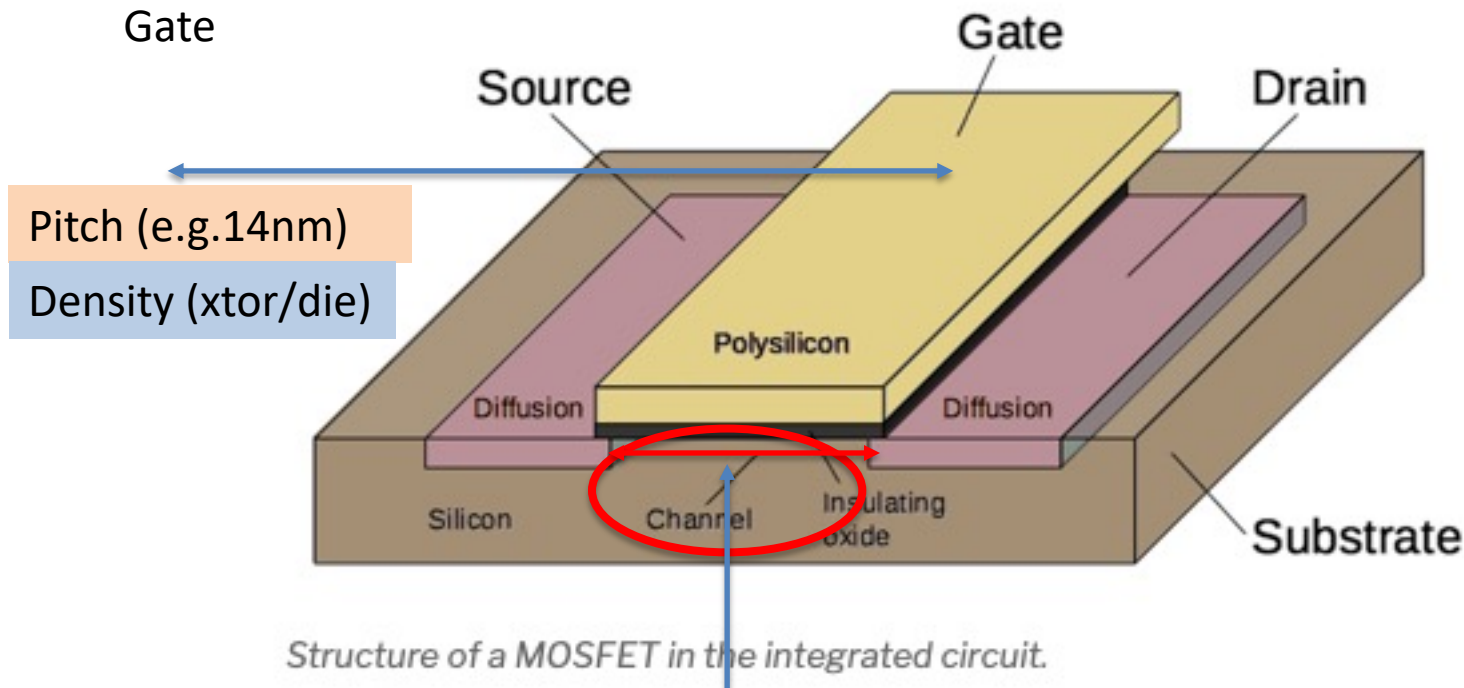


Structure of a MOSFET in the integrated circuit.

(see separate slide set **Transistors**)

MOS Transistor

$$V_g = 5 \rightarrow 3.3 \rightarrow 1.8 \text{ V}$$

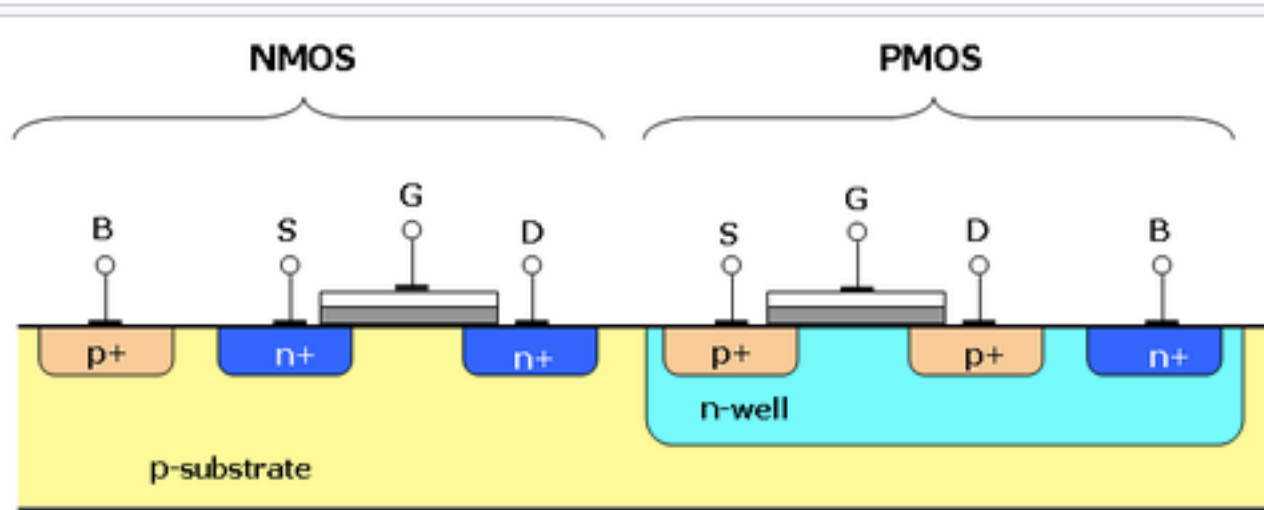


Smallest feature size (e.g. 5nm)

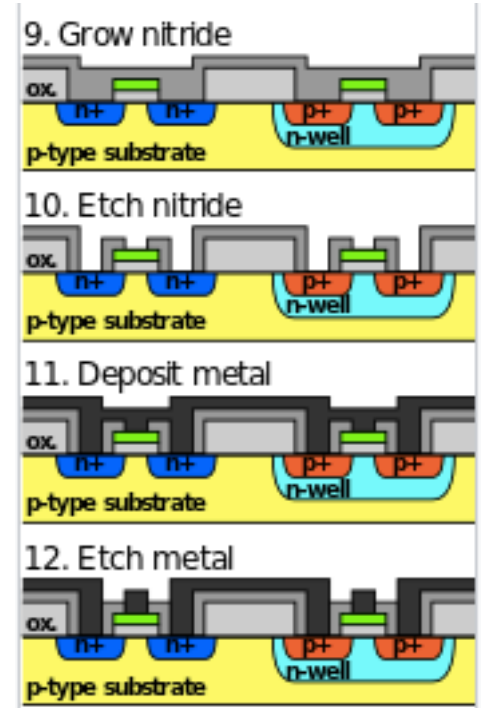
Performance (F_t)

CMOS Transistors

MOSFET



Cross section of two transistors in a CMOS gate, in an N-well CMOS process



Last 4 steps

IC Process & Interface

COMP122

TTL compatible

5V → 3V

❖ Bipolar

➤ RTL → DTL → TTL → Schottky TTL → LS TTL



5V

❖ MOS

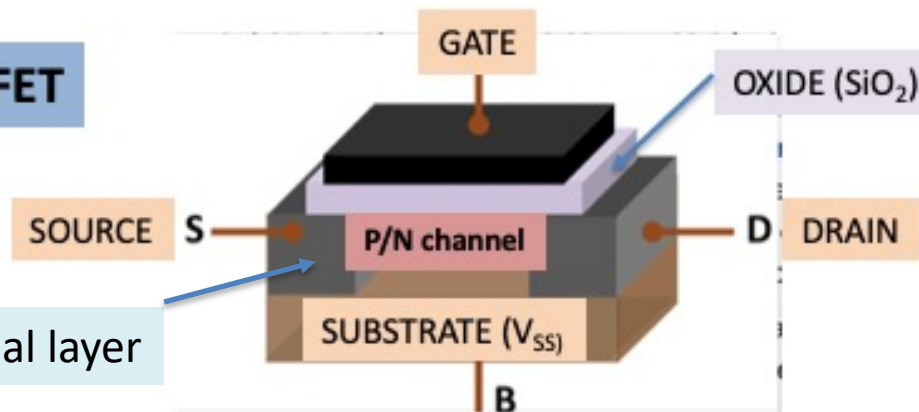
➤ PMOS → NMOS → CMOS → CMOS (TTL I/O) → 3.3V

5V → 3V

BiCMOS

MOSFET

Epitaxial layer



The metal–oxide–semiconductor field-effect transistor, also known as the metal–oxide–silicon transistor, is a type of field-effect transistor that is fabricated by the controlled oxidation of a semiconductor, typically silicon. It has an insulated gate, whose voltage determines the conductivity.

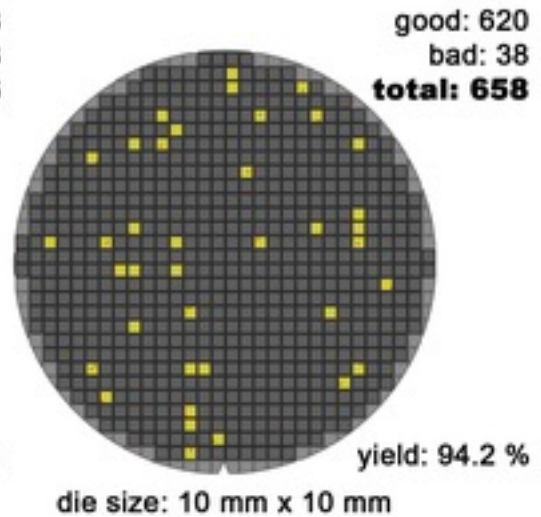
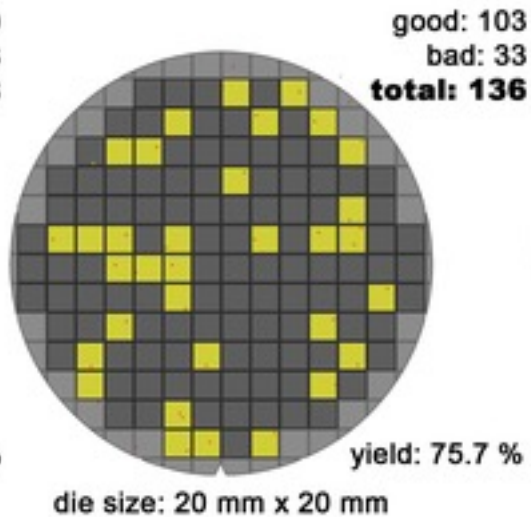
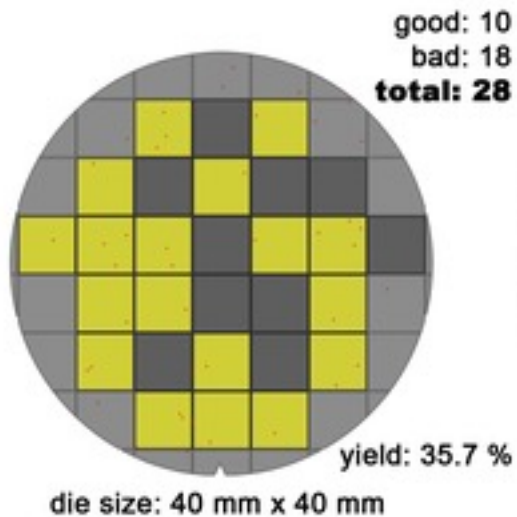
Section

Chip Design Fab

Chip Specs

- ❖ Architectural
- ❖ Functional
- ❖ Mechanical
- ❖ Electrical (DC)
- ❖ Timing (AC)
- ❖ Thermal (θ_{JA} , θ_{JC} , θ_{CA})

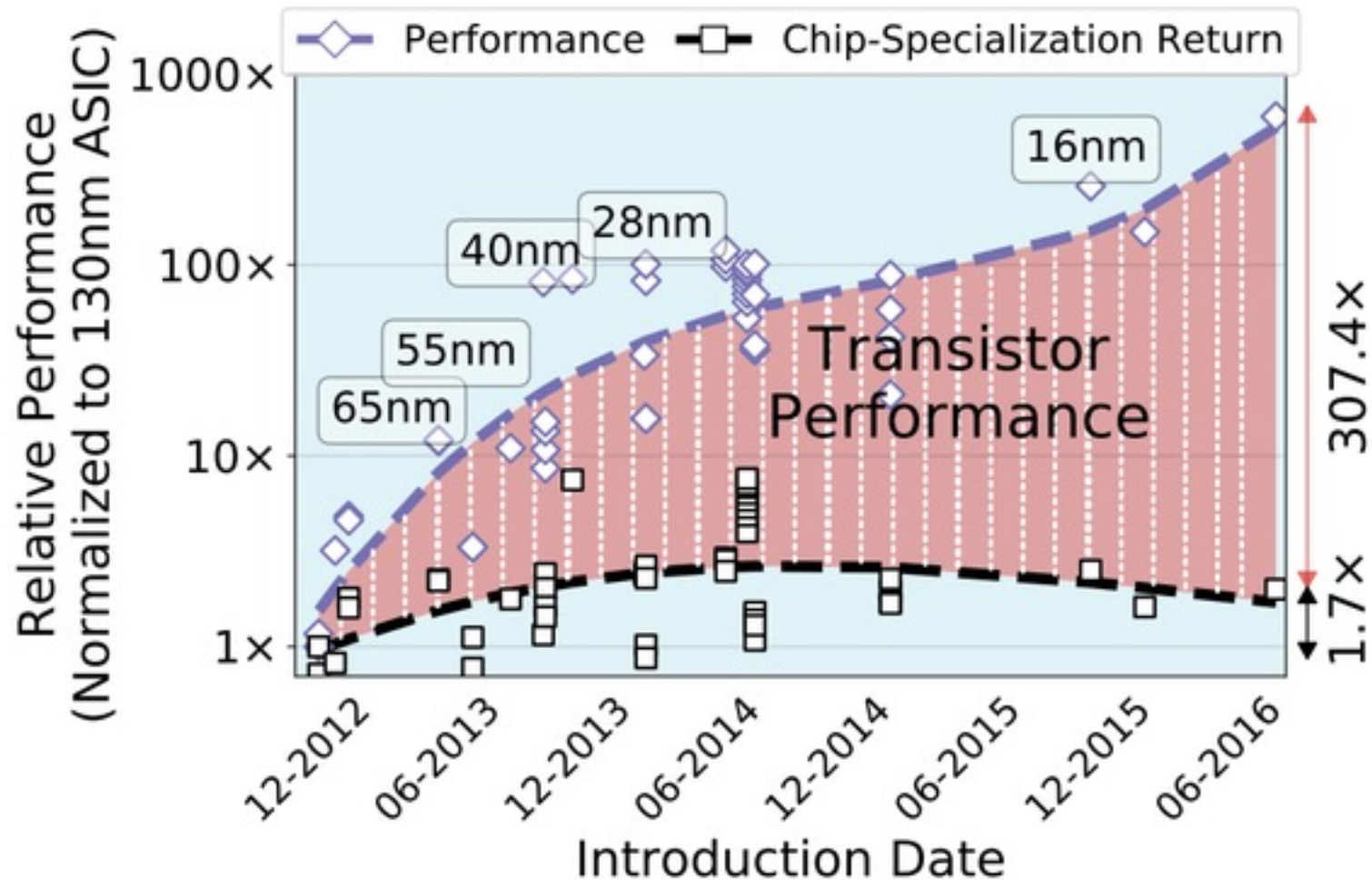
Wafers: Yield



yellow shows bad dice

(a function of defect density)

Chip Specializations



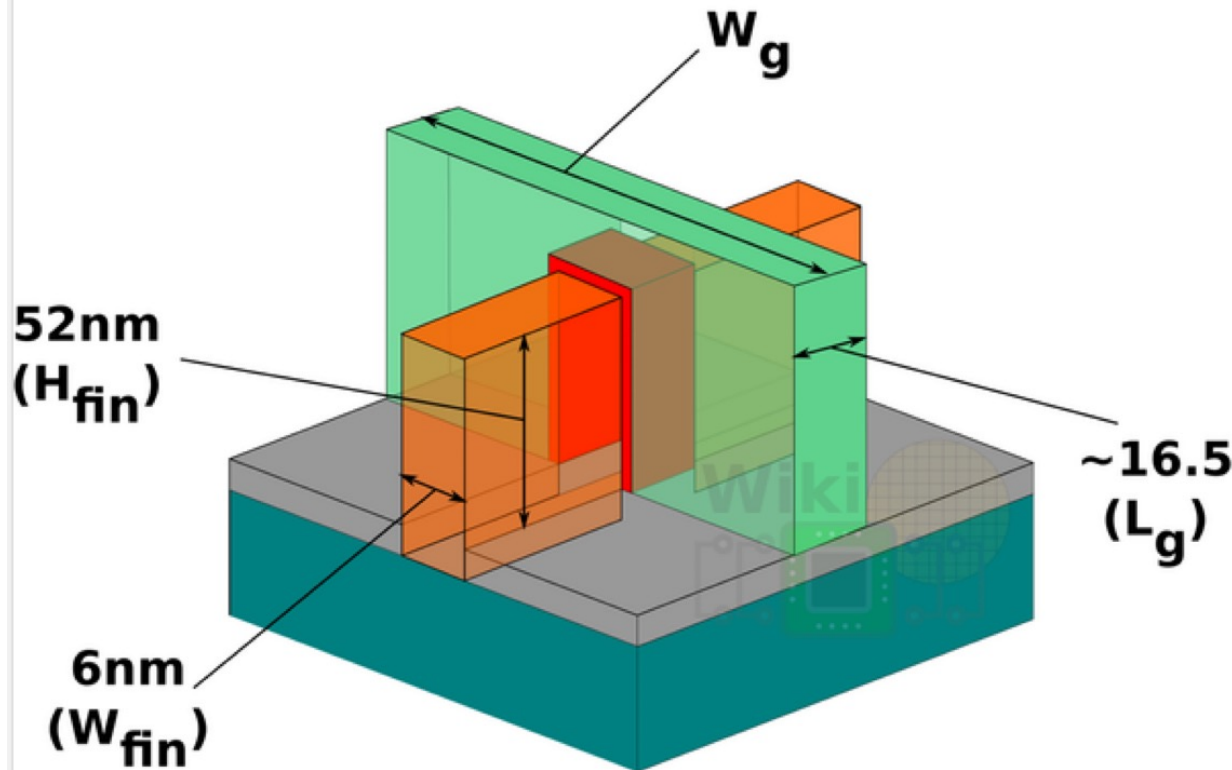
On-chip specialization or microarchitctural changes merely account for a fraction of the performance gains.

Chip Fab

7 nm TSMC

What's a 5nm FinFET transistor look like?

Well... I didn't find a good pic for 5nm, but I found a pic for 7nm [here](#): 

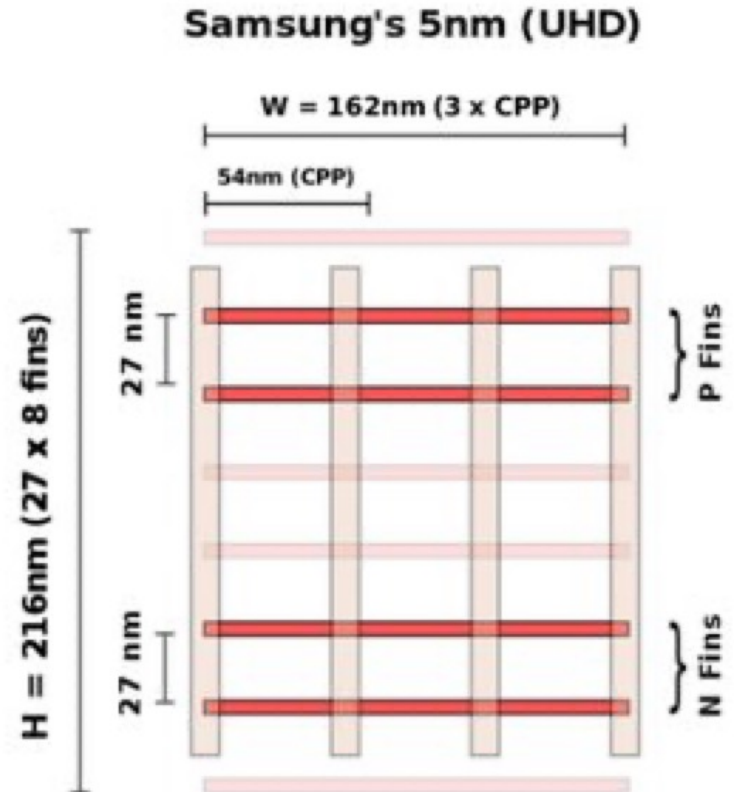
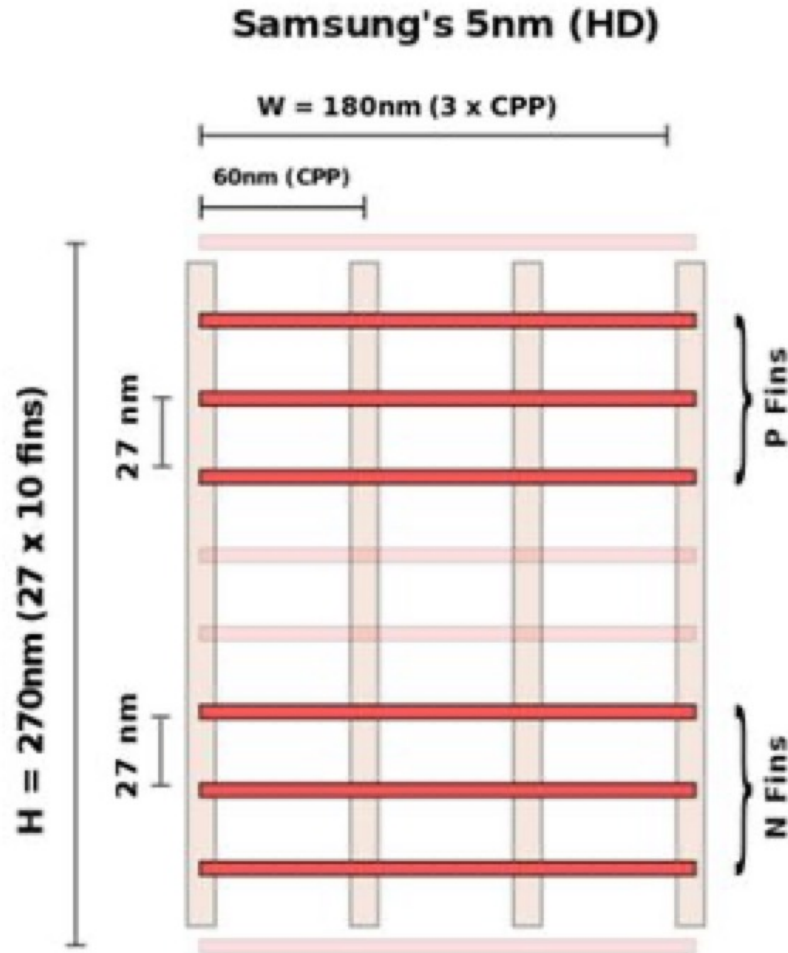


We can assume 5nm is slightly smaller on all axes.

The first thing to note is that the gate length (L_g) is 16.5nm. The width of the gate will vary, but I am going to go out on a limb and guess it is no smaller than $3W_{\text{fin}}$, or 18nm. And the overall structure is tall: 52nm plus another few nm

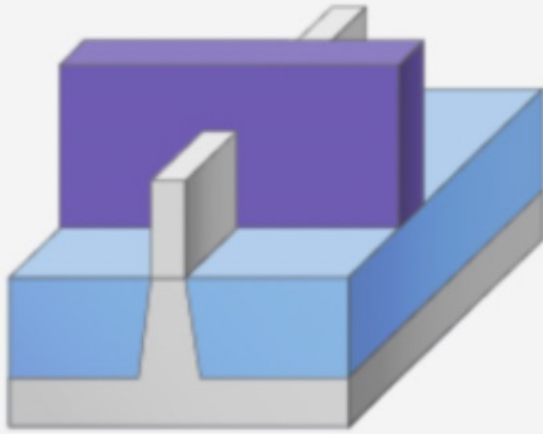
Making FinFET Transistors

CMOS = P & N

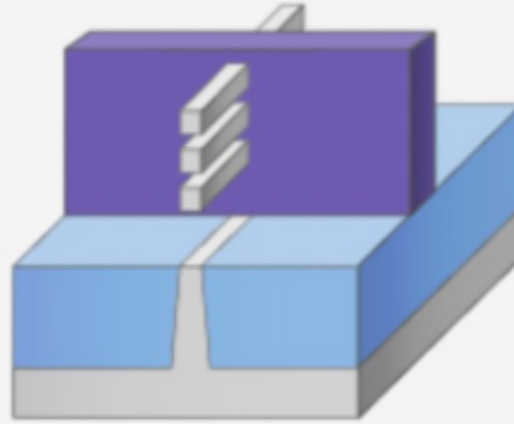


Above are CMOS gates having N and P transistors, roughly 5nm node has transistor size of 130 x 90 nm. Far, far, far away from 5nm name.

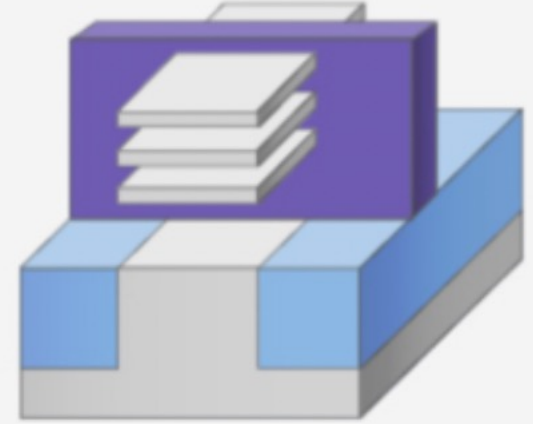
New Processes



FinFET



GAAFET
(Nanowire)



MBCFET™
(Nanosheet)

➤ It is all about the **Gate**

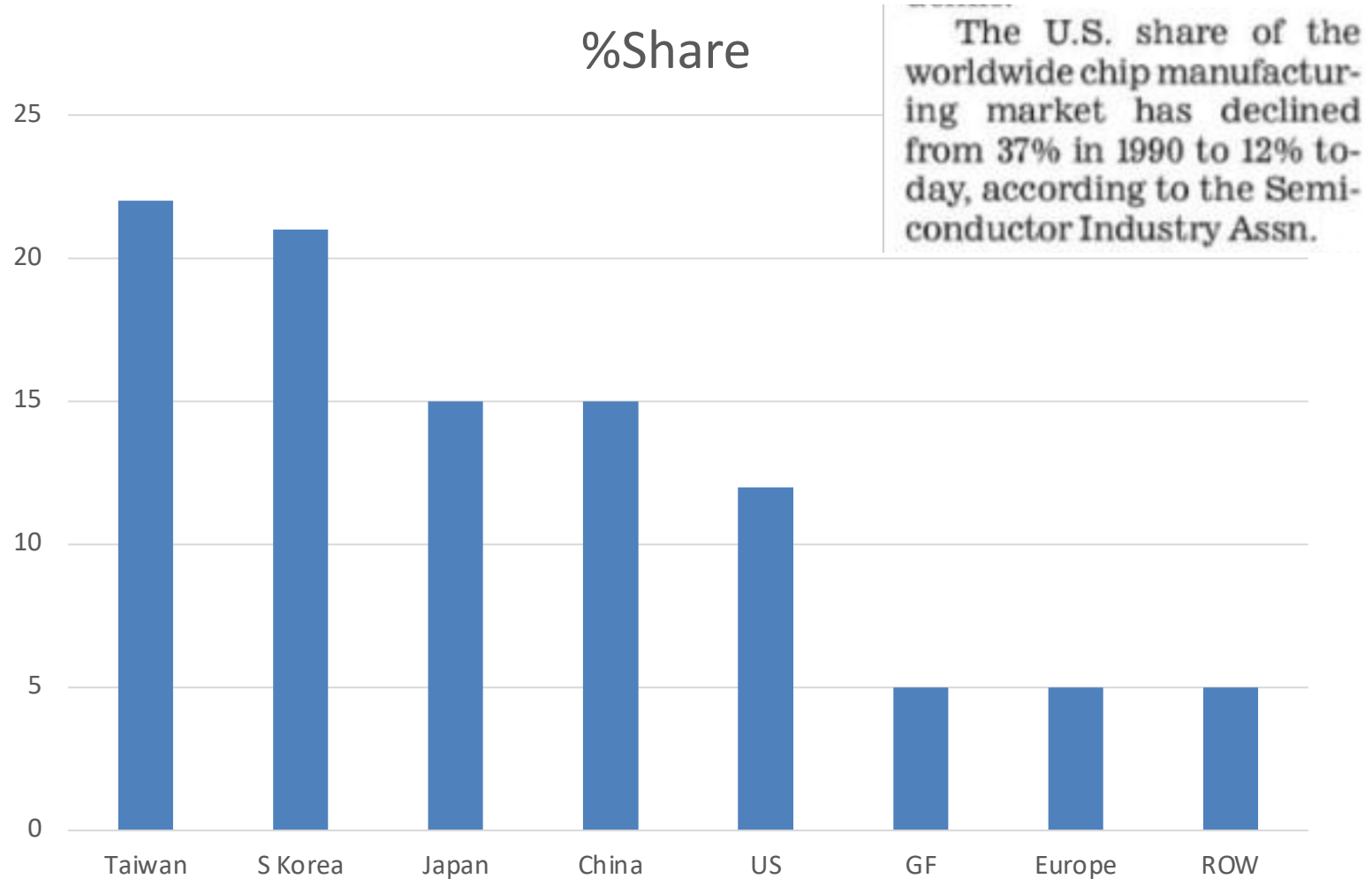
Wafer Fabs Today

- 1968 ❖ Intel
- 1978 ❖ Micron**
- 1980 ❖ Samsung
- 1987 ❖ TSMC* (1st foundry)
- 2009 ❖ AMD, IBM → Global Foundries*
- 2010 ❖ Chartered → Global Foundries*
❖ SMIC (China)

*Pure Foundry

**Internal use only

WW Fab Shares

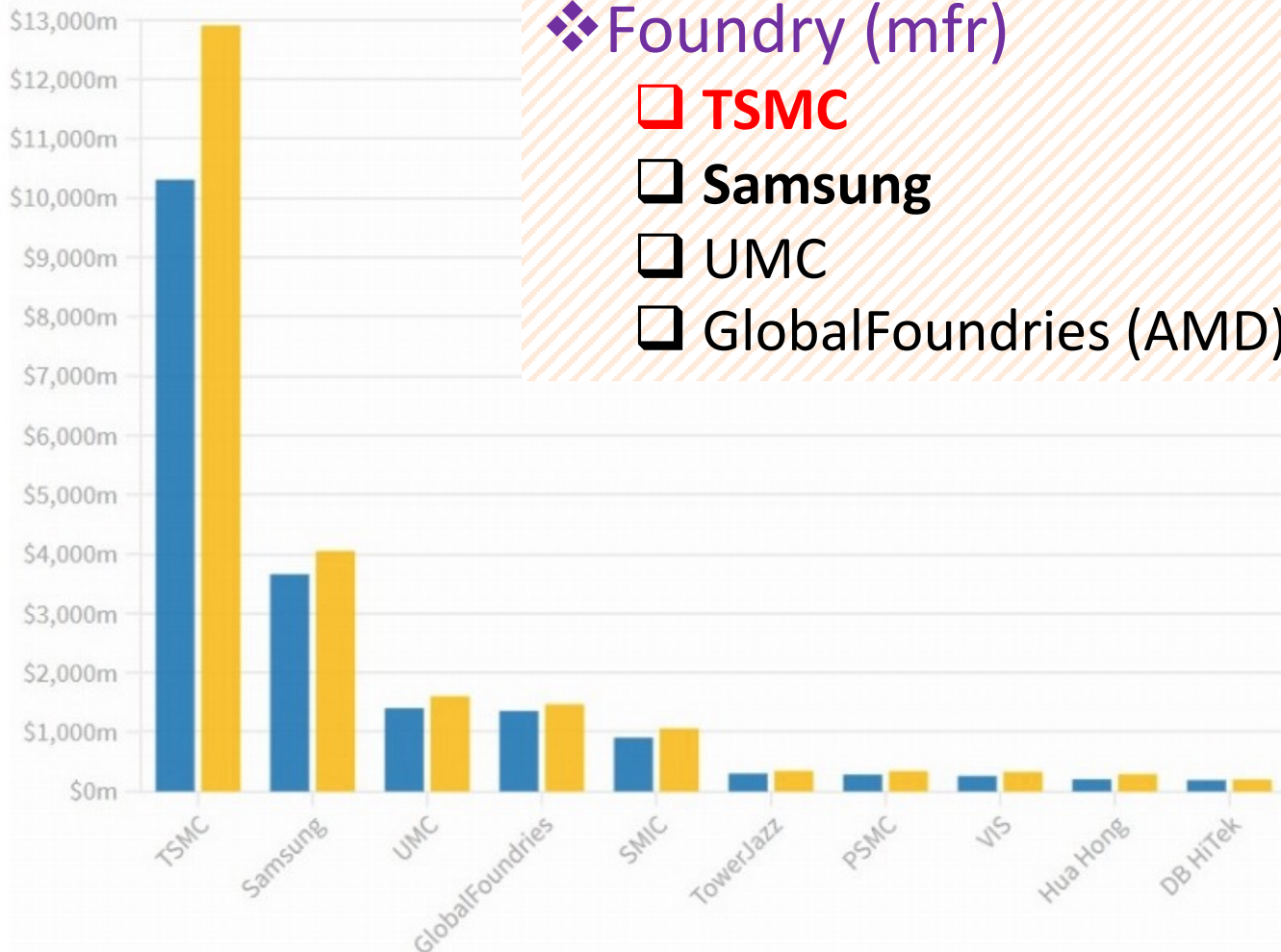


Source: LA Times/SIA 1/22/22

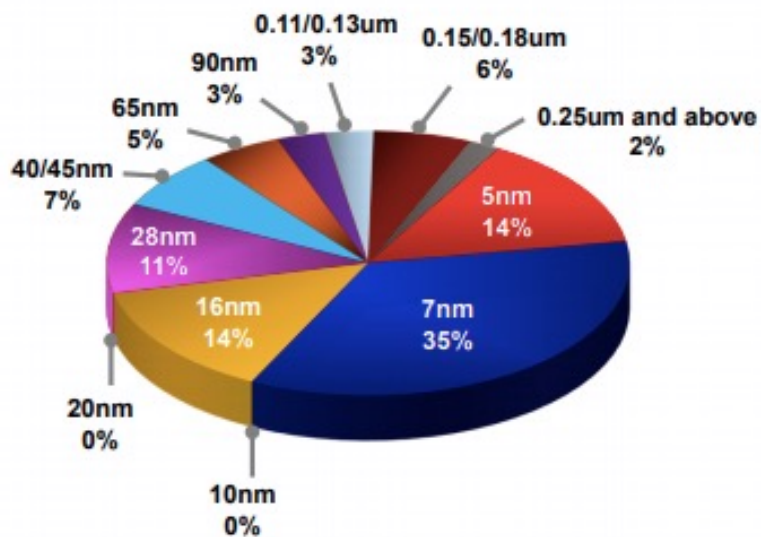
Foundry Sizes 2020-1

Top semiconductor foundries by revenue

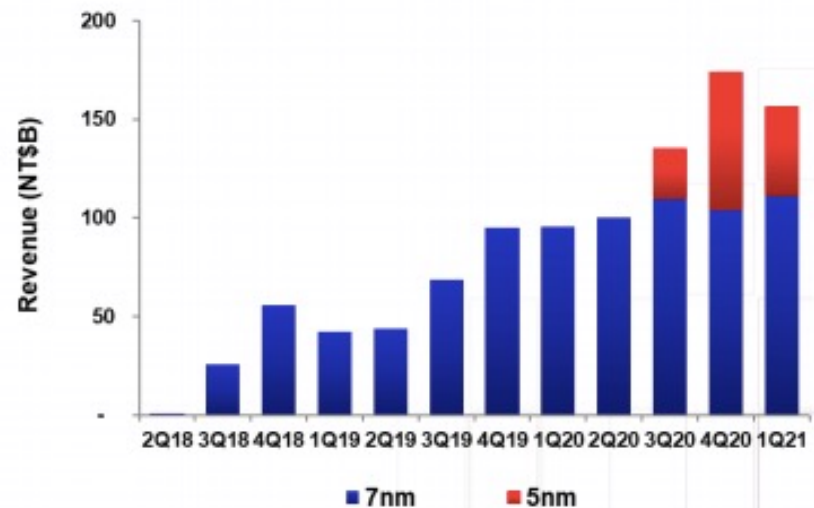
■ Q1 2020 ■ Q1 2021 (Projected)



1Q21 Revenue by Technology



7nm and Below Revenue



TSMC Customers

Table 4 – TSMC Customer Share of Revenues 2019-2021

	2019	2020	2021
Apple	24.0%	24.2%	25.4%
Hi-Silicon	15.0%	12.8%	0.0%
Qualcomm	6.1%	9.8%	7.6%
NVIDIA	7.6%	7.7%	5.8%
Broadcom	7.7%	7.6%	8.1%
AMD	4.0%	7.3%	9.2%
Intel	5.2%	6.0%	7.2%
Mediatek	4.3%	5.9%	8.2%

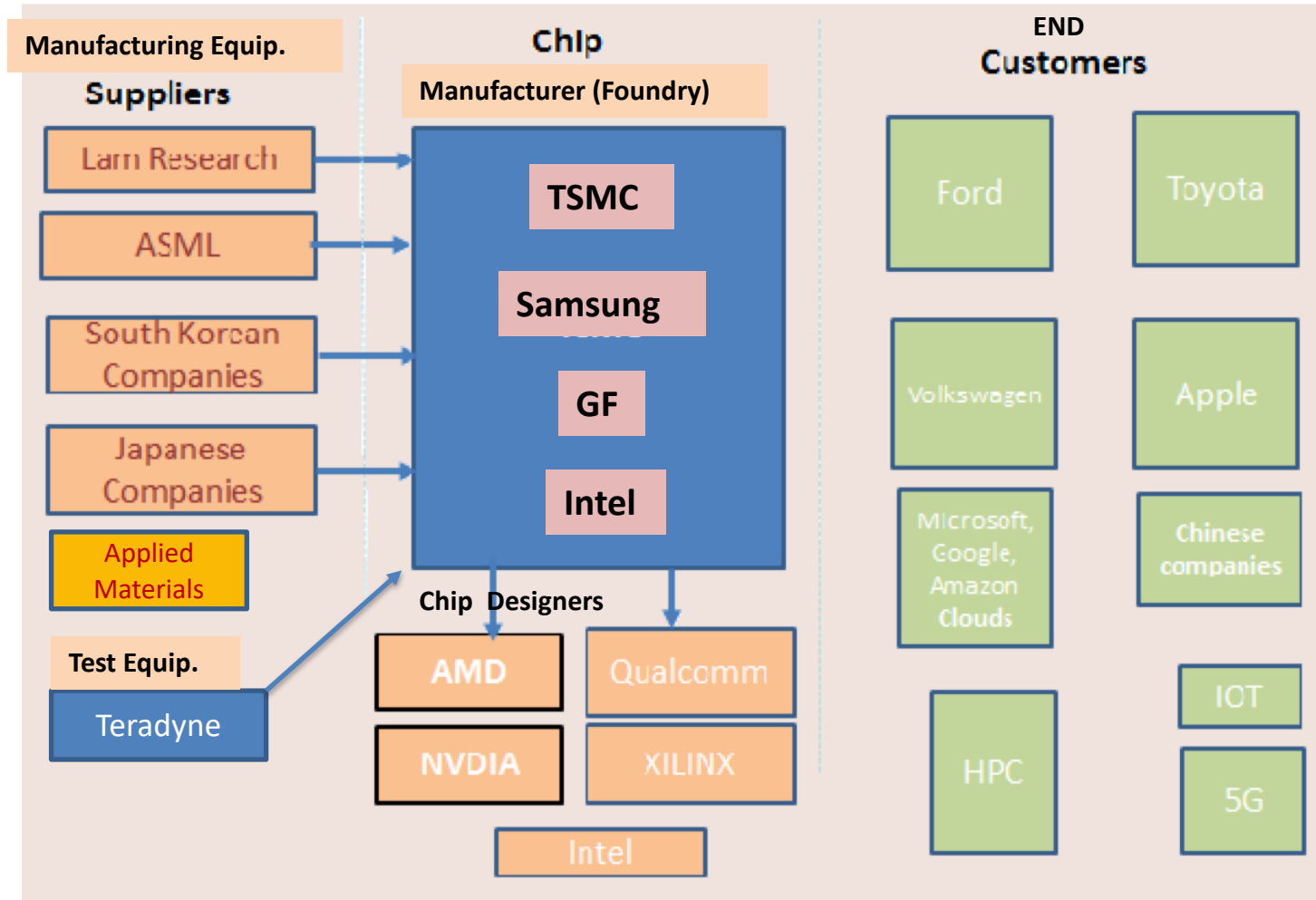
Source: The Information Network (www.theinformationnet.com)



Harvey King

born in Taiwan, grew up in US, family rooted in mainland China for centuries.

Foundry Supply Chain



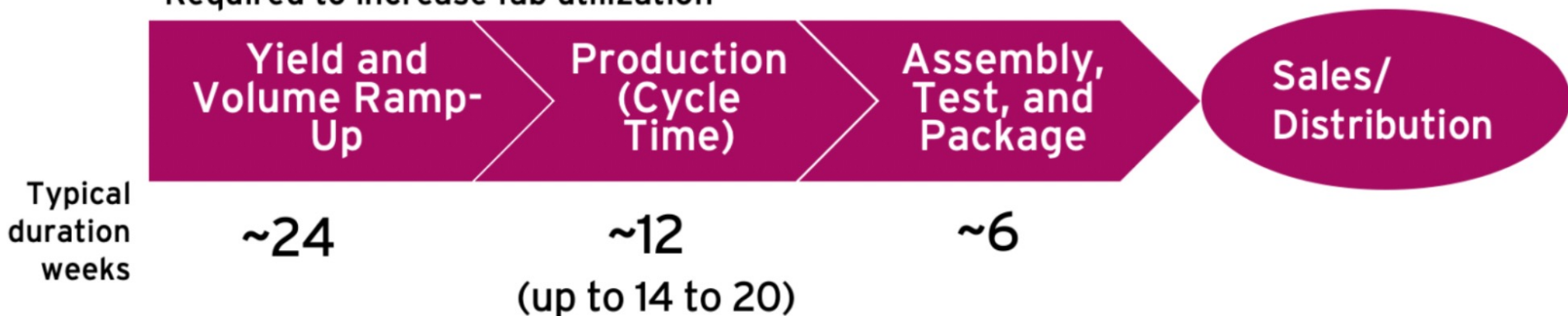
Fab Timescales

COMP222

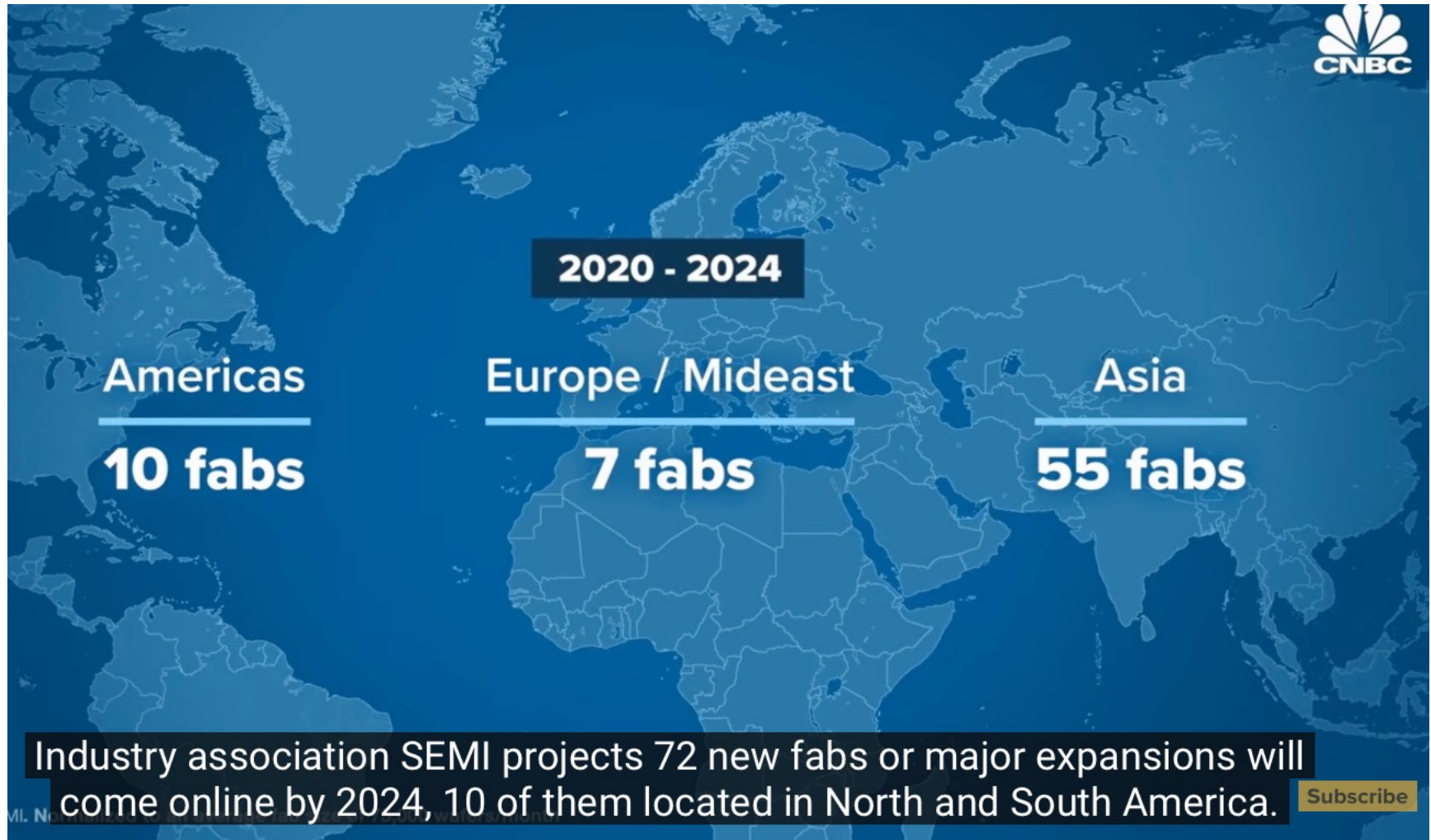


Semiconductor Fab Production Timescales

Required to increase fab utilization



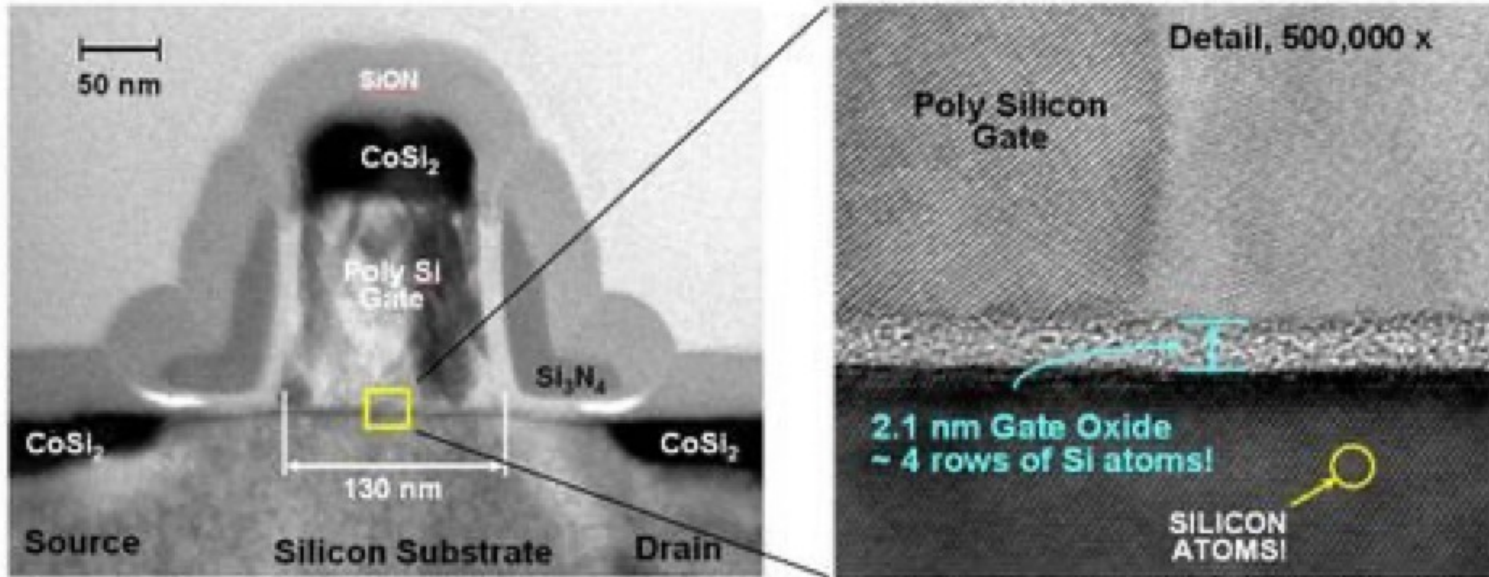
Global 72 New Fabs



Metal Interconnect

Aluminum → Copper → Cobalt

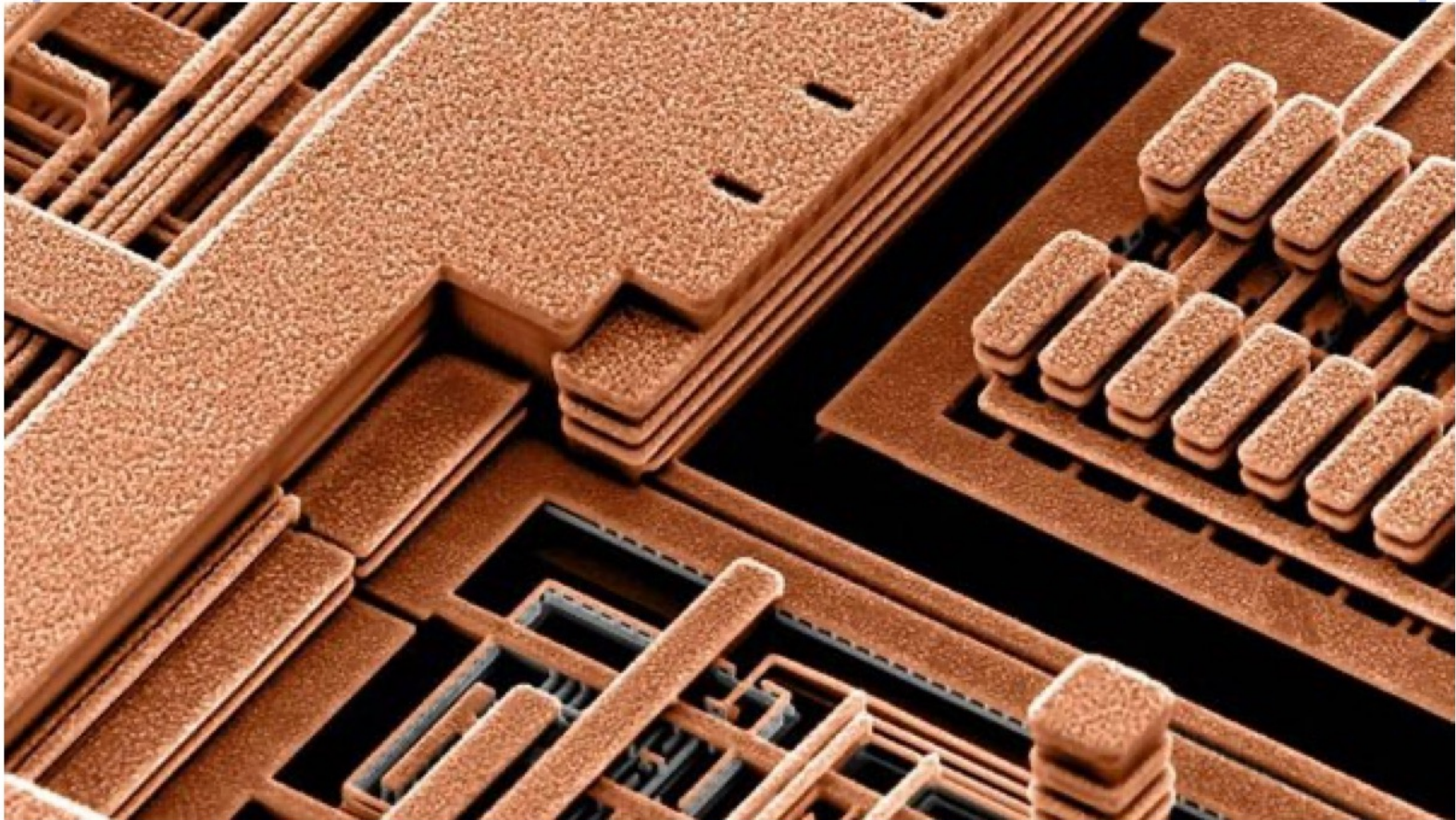
Figure 1 - Electron Micrograph of CMOS FET Cross Section



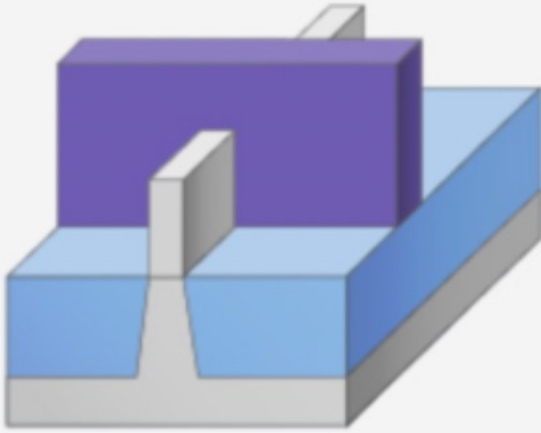
Metal Interconnect

Aluminum → Copper → Cobalt

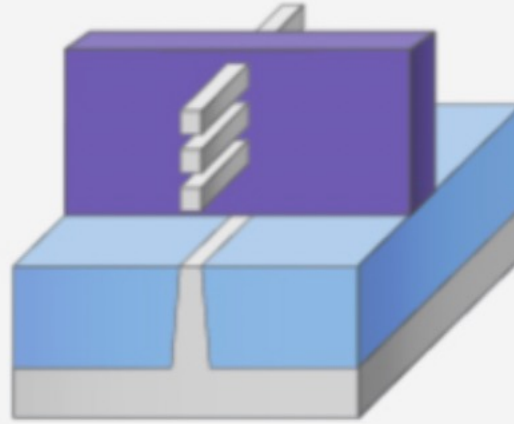
The transistors connect to each other using metal wires called interconnects. There are several layers of them (more than 8). Usually the space between them is filled with an insulator to provide structural rigidity, and expel air which can expand when heated and damage the chip, but IBM very kindly took the insulator out of one of their chips to show what the interconnect looks like:



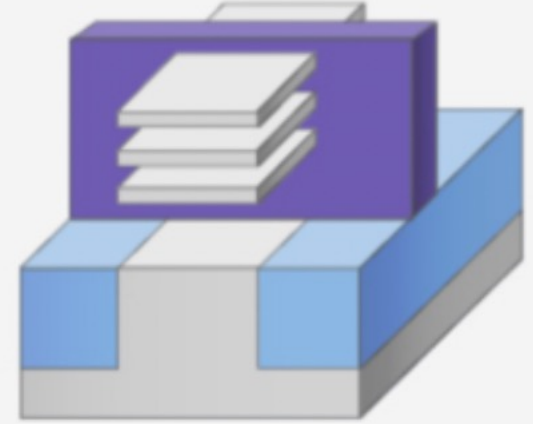
New Processes



FinFET



GAAFET
(Nanowire)



MBCFET™
(Nanosheet)

Chip Packaging



Package Technology Evolution

1960 – 1985
CDIP, PDIP+
> 50 pkg types



1986 – 1995
SOIC, PLCC, QFP+
> 250



1996 – 2000
BGA, QFN, SiP+
> 1000



2001 – 2005
Modules, Cards, Stack
> 1500

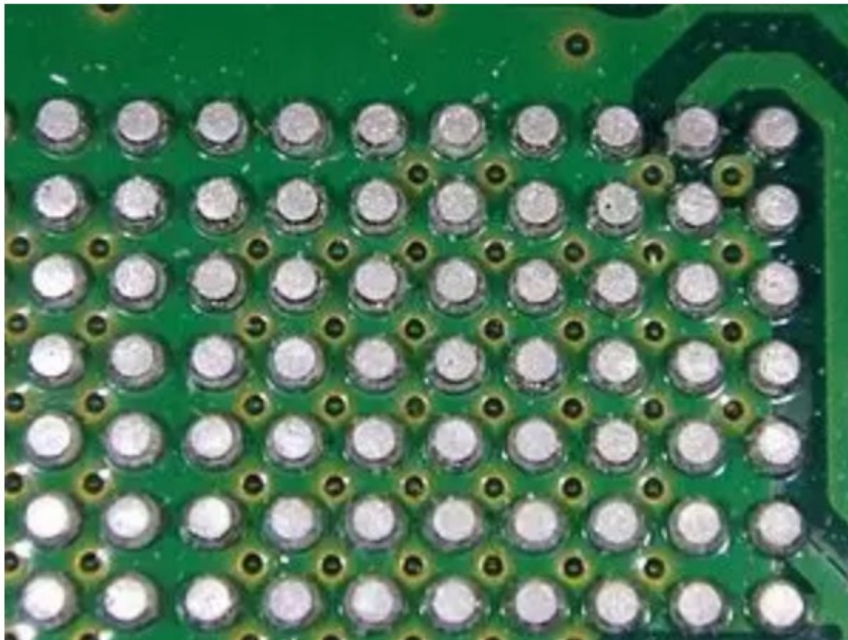


Source: Amkor

Chip Packaging

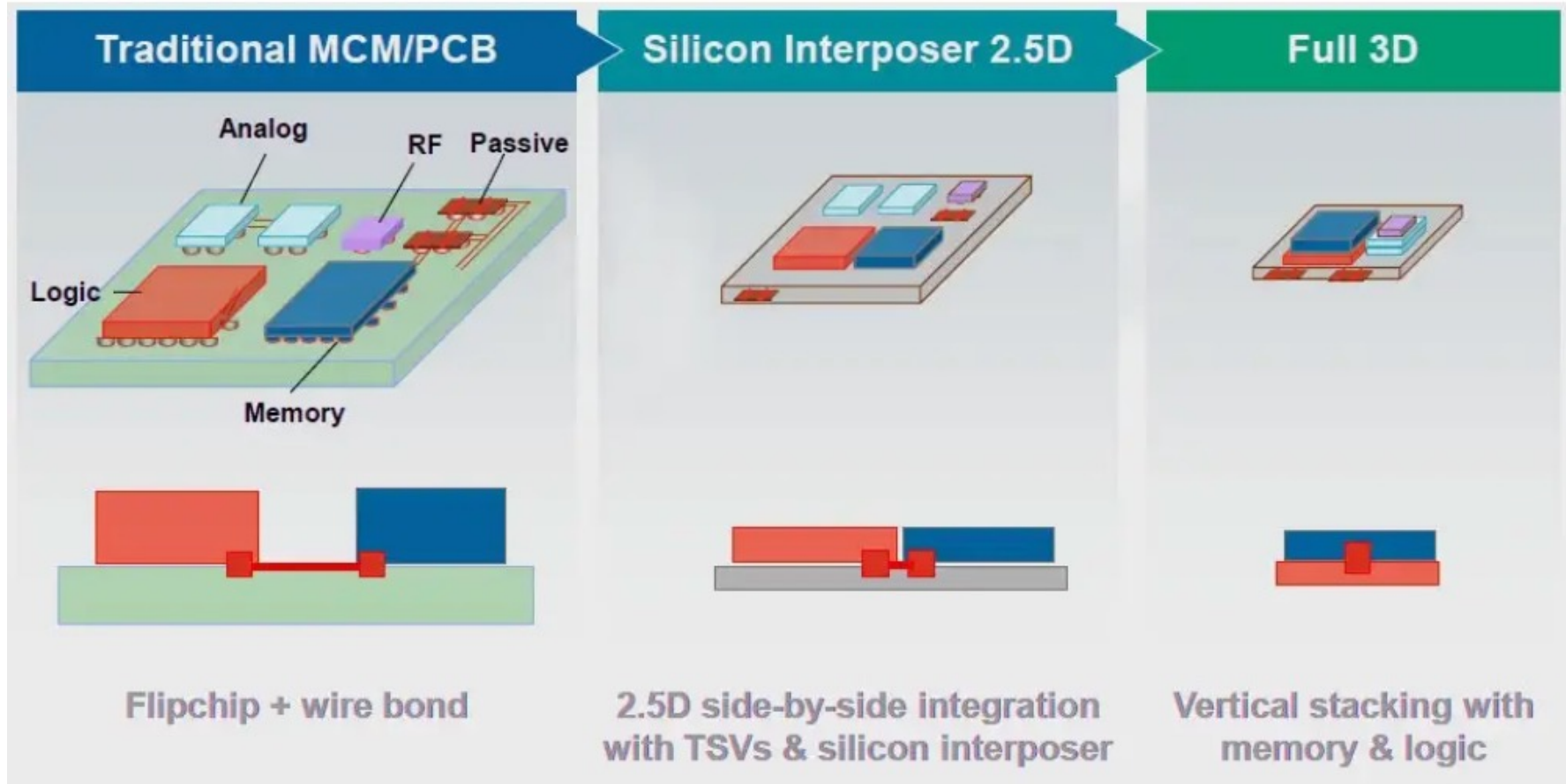
Ball Grid Packaging and Chip Scale Packaging (1990s – 2000s)

As the demands of semiconductor speed continue to pick up, so does the need for better packaging. While QFN (quad-flat no-leads) and other Surface Mounted technologies clearly continue to proliferate, I want to introduce you to the beginning of a package design that we will have to know about in the future. This is the beginning of the solder balls – or broadly Ball Grid Array (BGA) packaging.



Those balls or bumps are called solder bumps/balls

Chip Packaging (MCM)



Section

CPU Cores

CPU Function

What is the most purely mathematical description you could give of the workings of a CPU?



Jeff Drobman

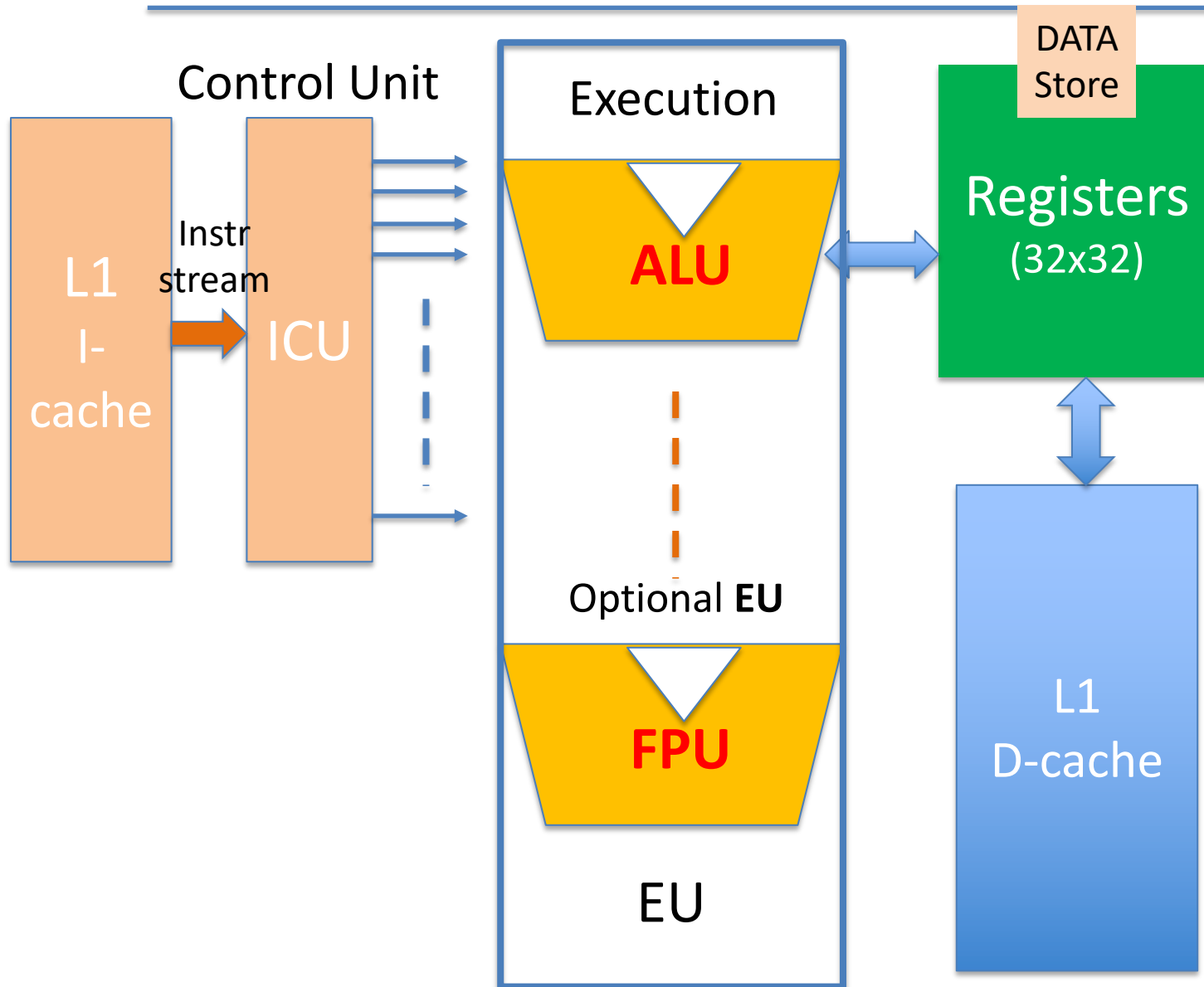
Lecturer at California State University, Northridge (2016–present) · Just now

`CPU_state = function(instruction, last_state)`

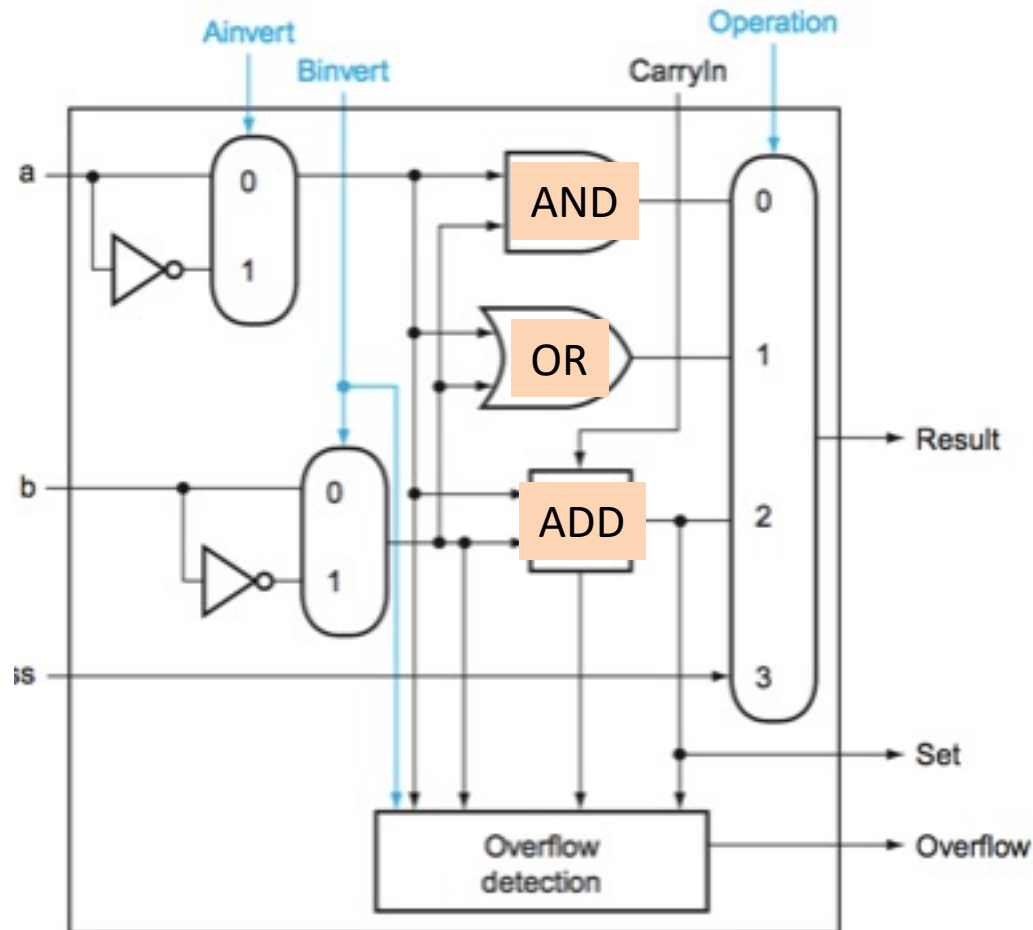
FSM definition

`CPU_state = Function(instruction, last_state)`

CPU = Data + Control



MIPS/MARS ALU



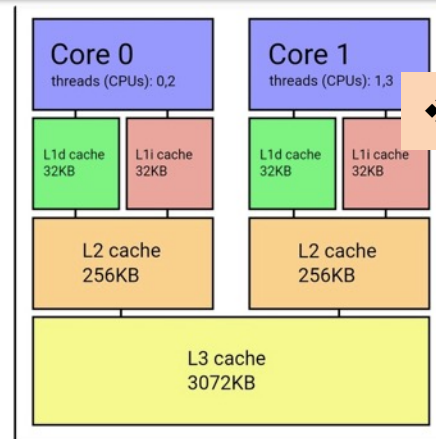
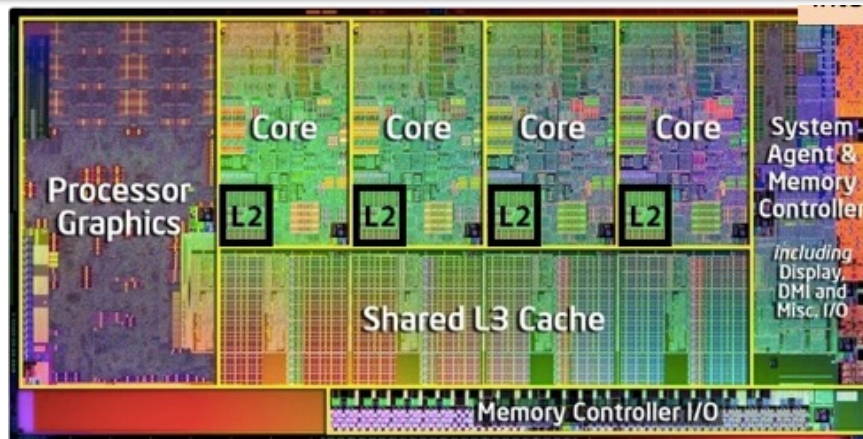
4 Levels of CPU Architecture

COMP222

COMP122/222

❖ Macro

System=
Multi-core
SoC

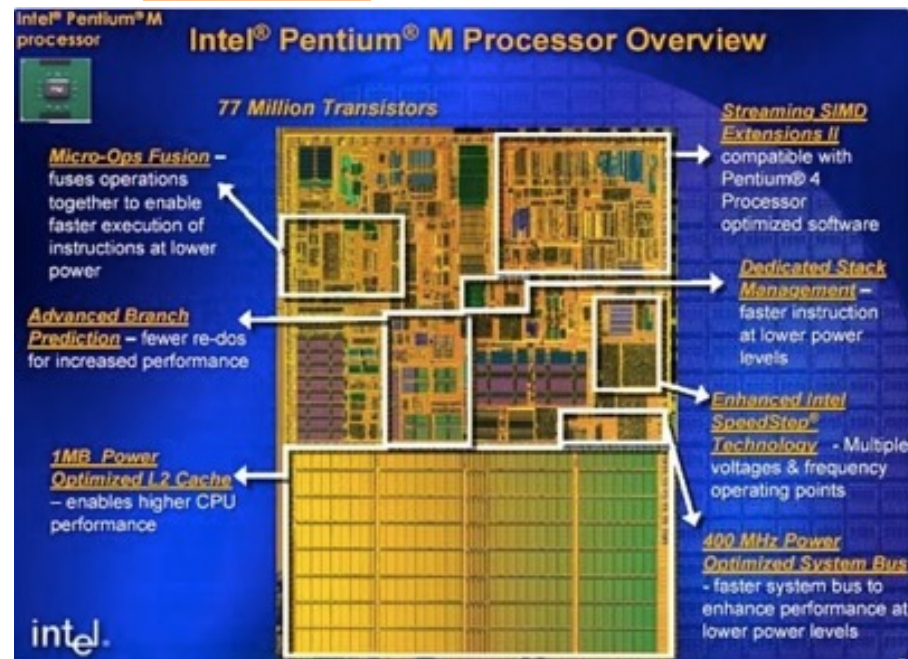
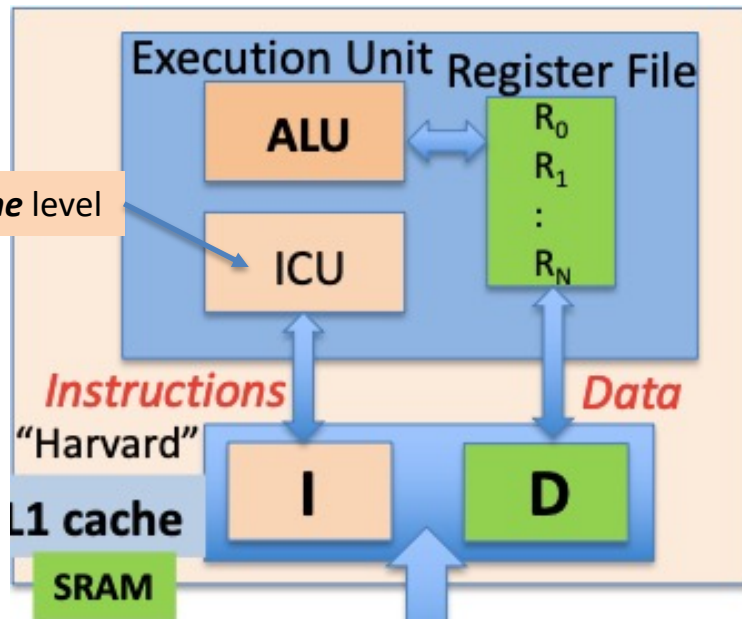


❖ Floorplan

COMP122

❖ Org + ISA *CPU Core* internals

COMP222 ❖ Micro *Pipeline* level

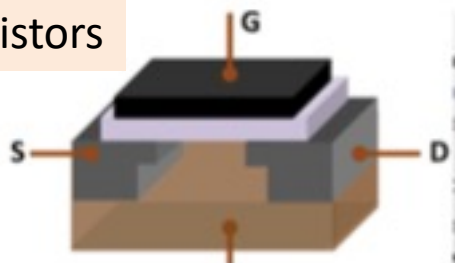


3 Levels of Integration

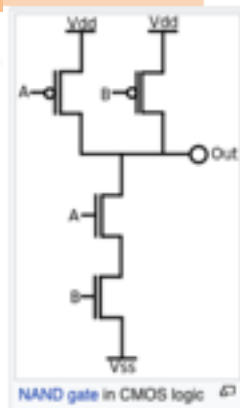
COMP222

Hardware Building Blocks

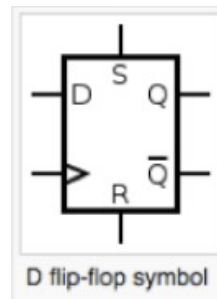
0- Transistors



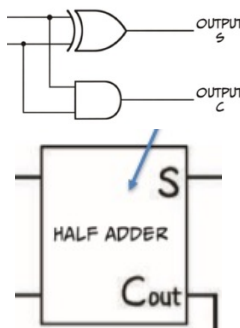
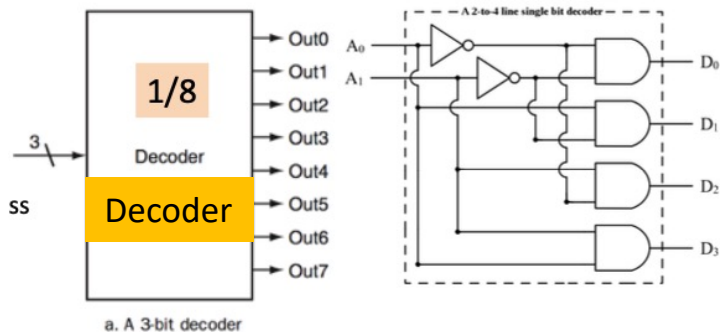
NAND



1- Gates & FF's

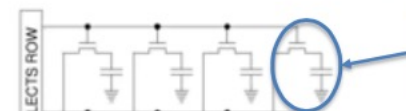


2-Single Functions



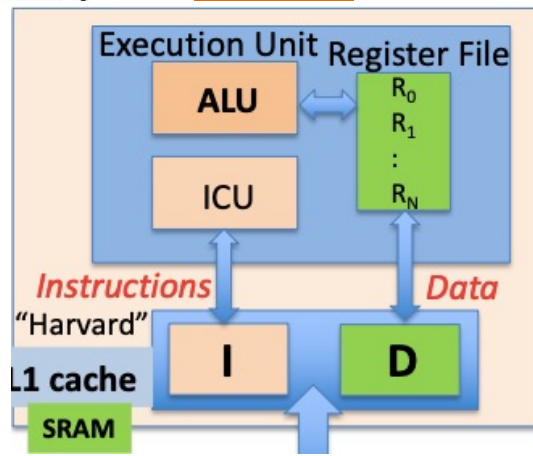
Memory Cells

The DRAM

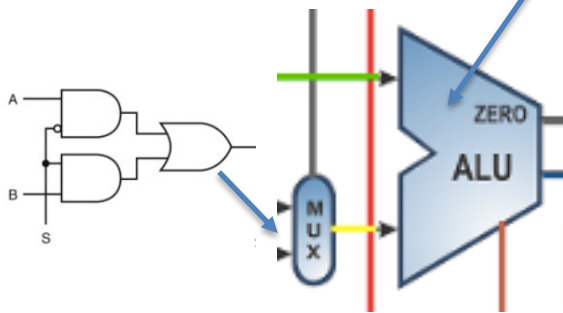
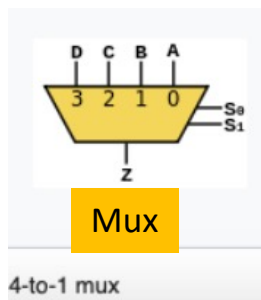
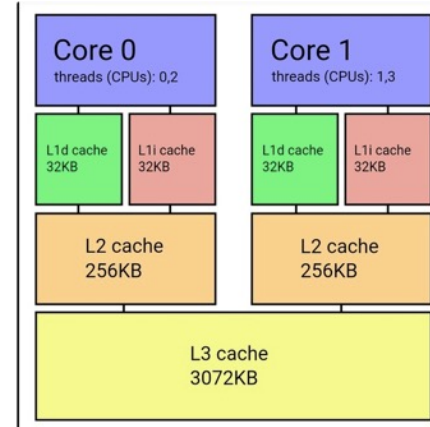


- ❖ 1 transistor
- ❖ 1 cap (parasitic)

3-CPU



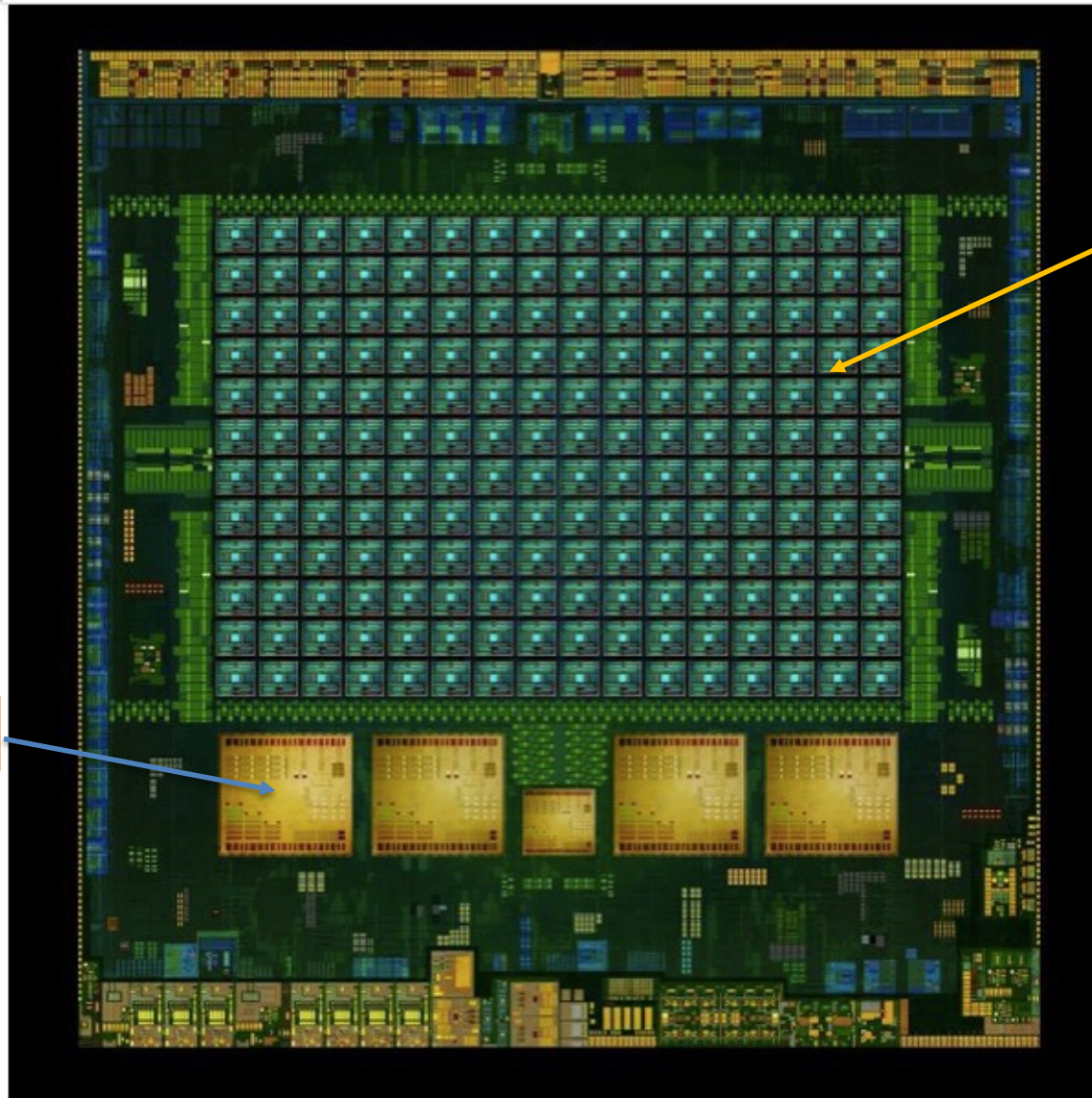
3-Multi-core CPU



SoC = CPU + GPU

CPU cores

GPU cores

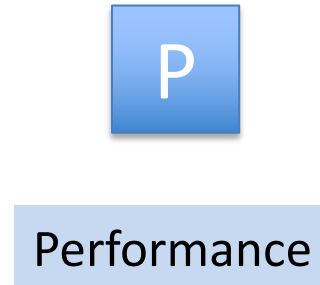
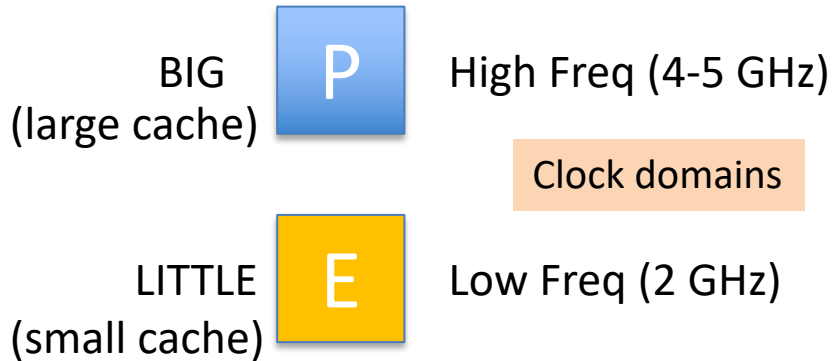


This SOC has four CPU cores (ARM Cortex) and 192 GPU cores (Kepler).

CPU Cores: P & E

Mobile & Laptop
(battery power)

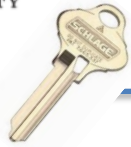
Desktop
(Server)



Efficiency (Power)

Section

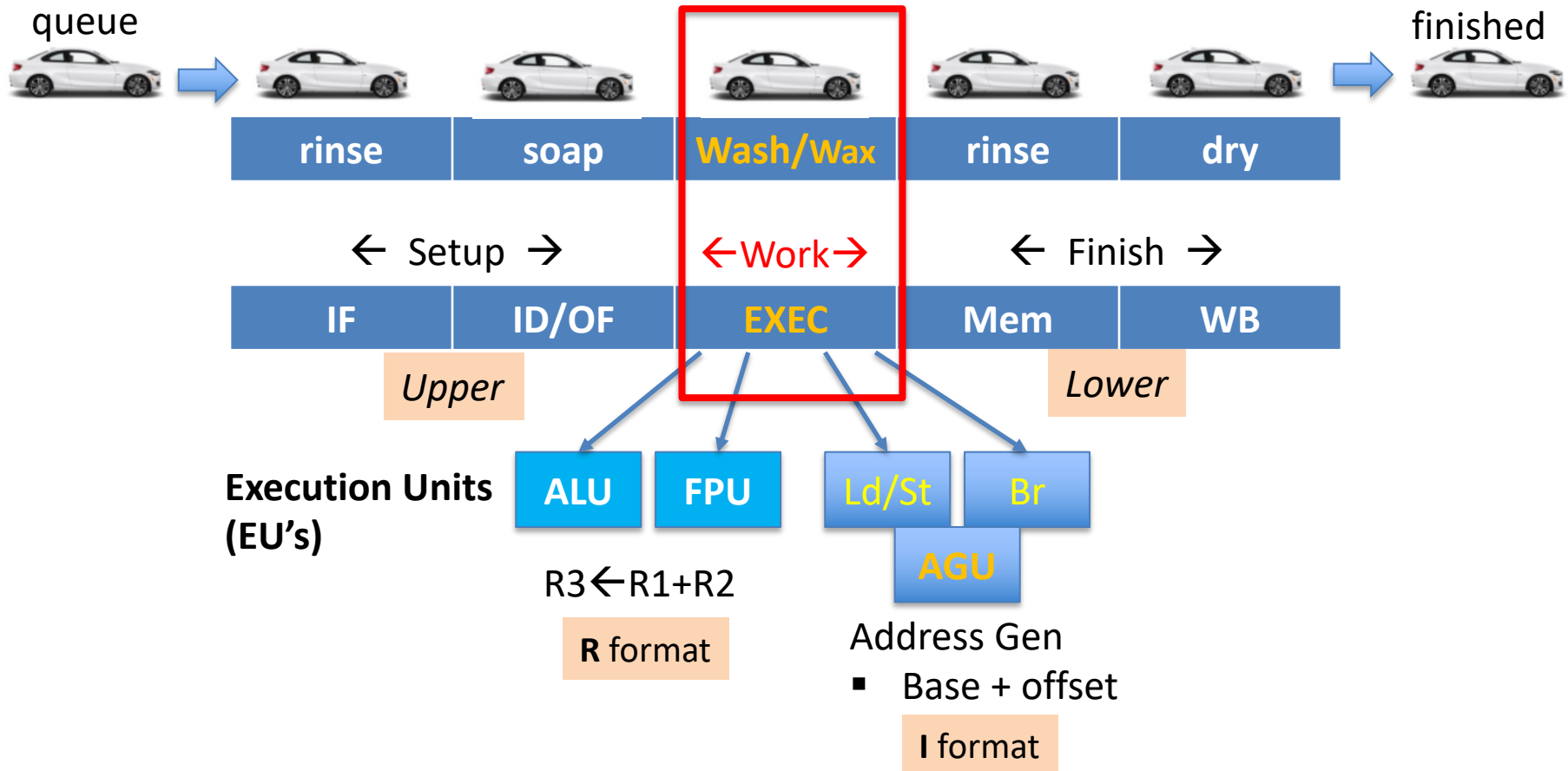
Pipelines



MIPS RISC Pipeline

5 Stages

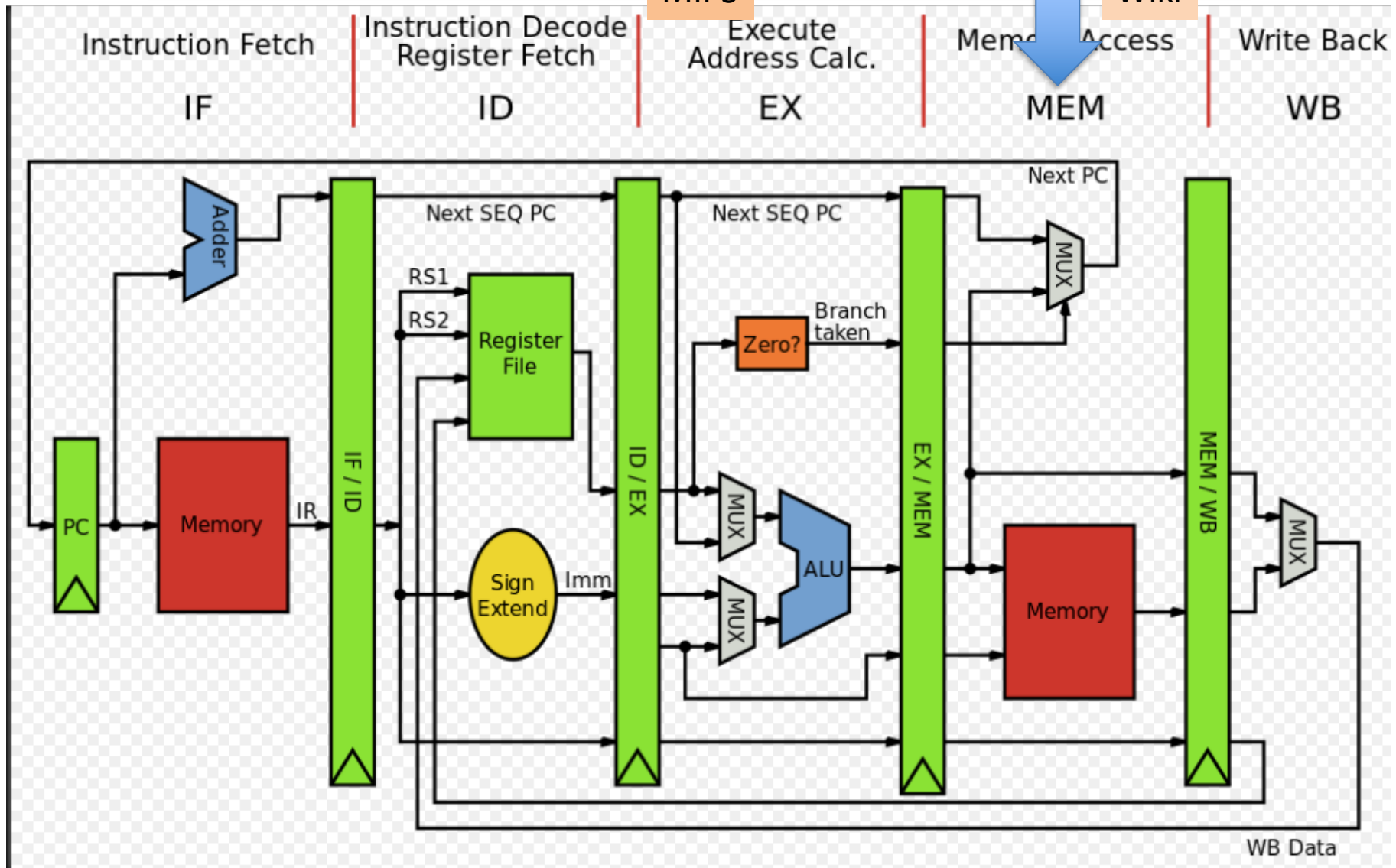
Each stage takes only 1/5 of instruction cycle: **clock F \Rightarrow 5x**



MIPS Pipelined Org

MIPS

Wiki



MIPS, showing the five stages (instruction fetch, instruction decode, execute, memory access and write back).