Rev 6-9-24

Chip Foundries Fabs

by
Dr Jeff Drobman
Dr Jeff Software & CSUN

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DR JEFF SOFTWARE
INDIE APP DEVELOPER
Jeff Drobman

Chips

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Wafer Fabs

Foundries

Chip Packaging (MCM)

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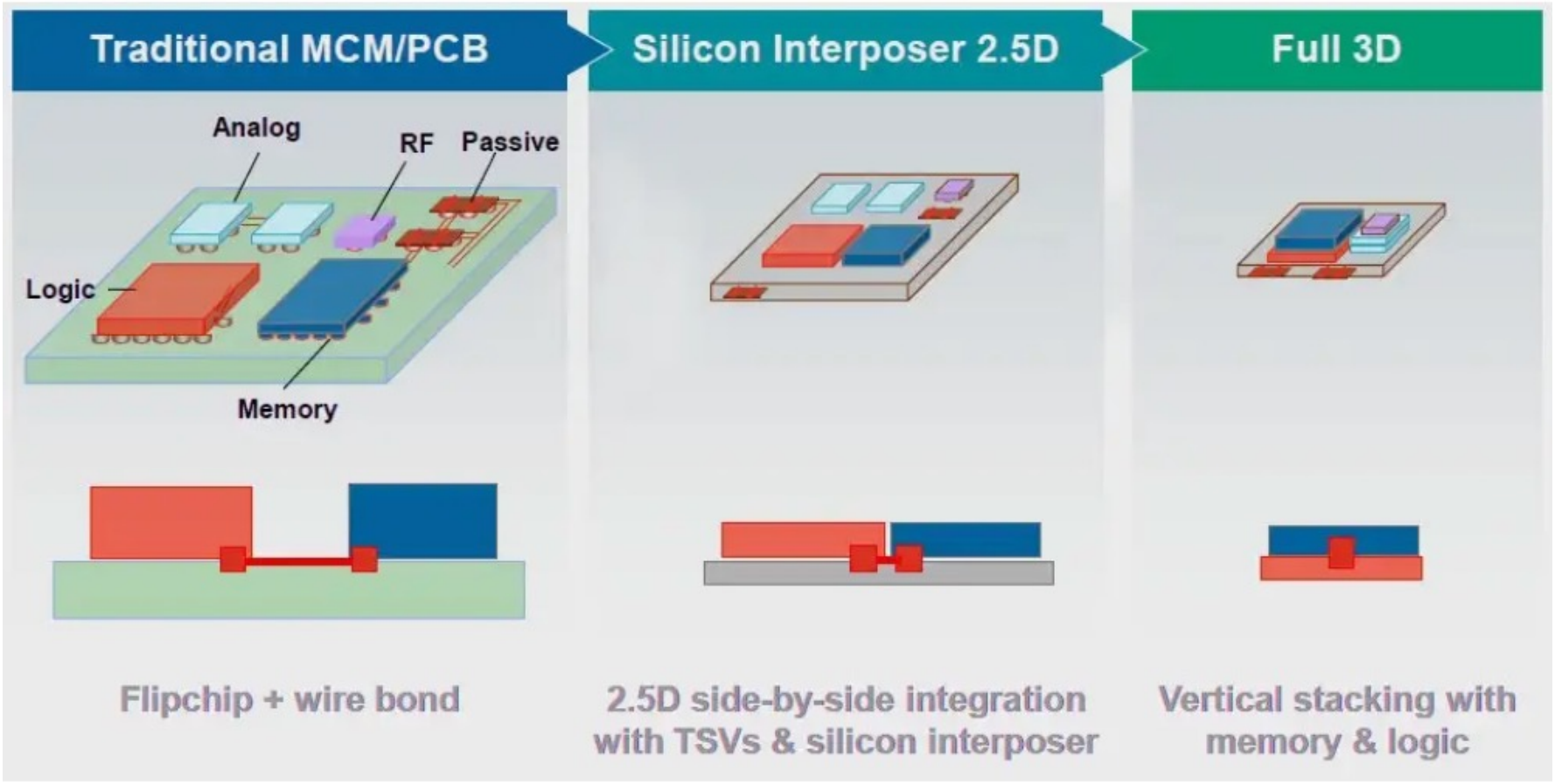

Chip Packaging: 3D Die

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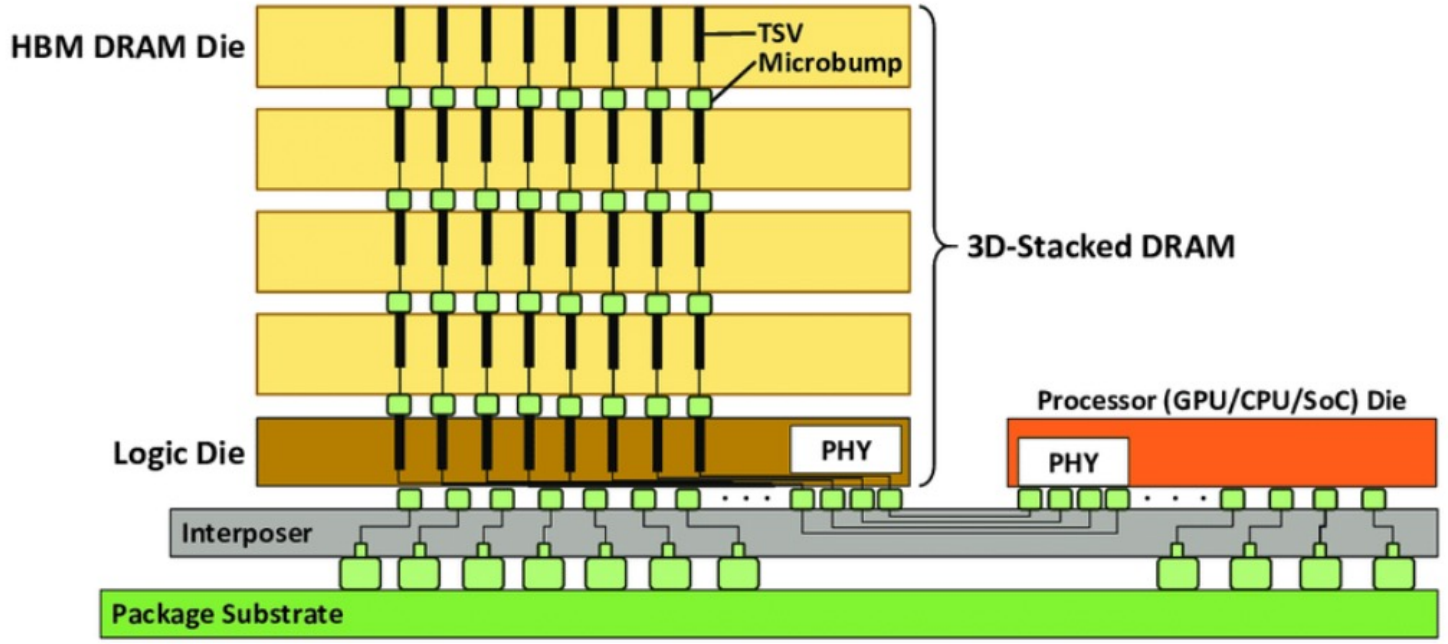
3D DRAM die stack

And what's interesting is we have a clear example of an entire semiconductor market that went 3D – Memory. Memory's push into 3D structures is a very good indication of what's to come. Part of the reason why NAND had to go 3D was that they struggled to scale at smaller geometry. Imagine memory as a large 3D skyscraper, and each of the floors is kept together by an elevator. These are called "TSV"s or Through silicon vias.



This is what the future looks like, and it's even possible we will be stacking GPU/CPU chips on each other or stacking memory on CPU. This is the final frontier

Foundries Supply Chain

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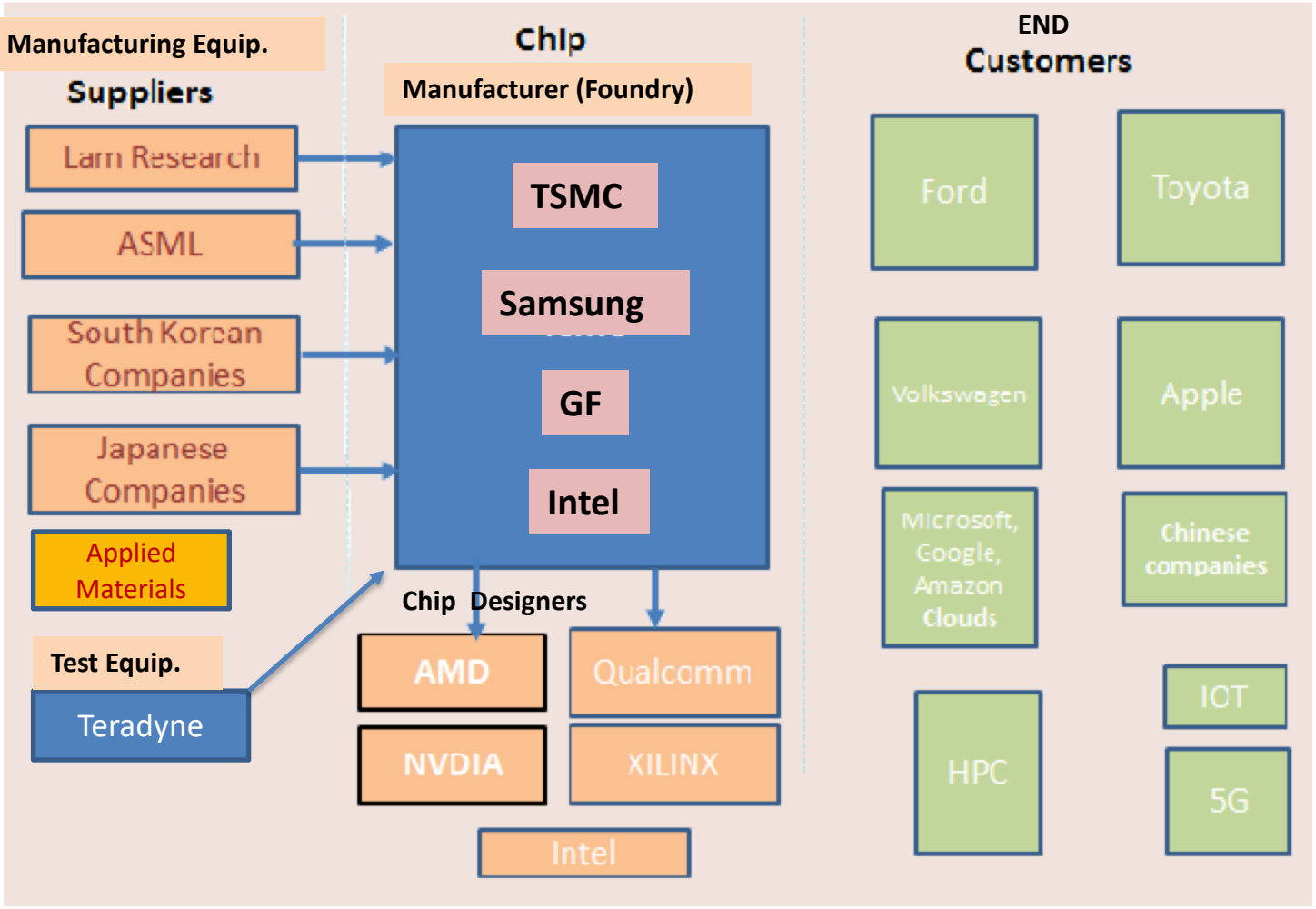
Quora

Harvey King
born in Taiwan, grew up in US, family rooted in mainland China for centuries.



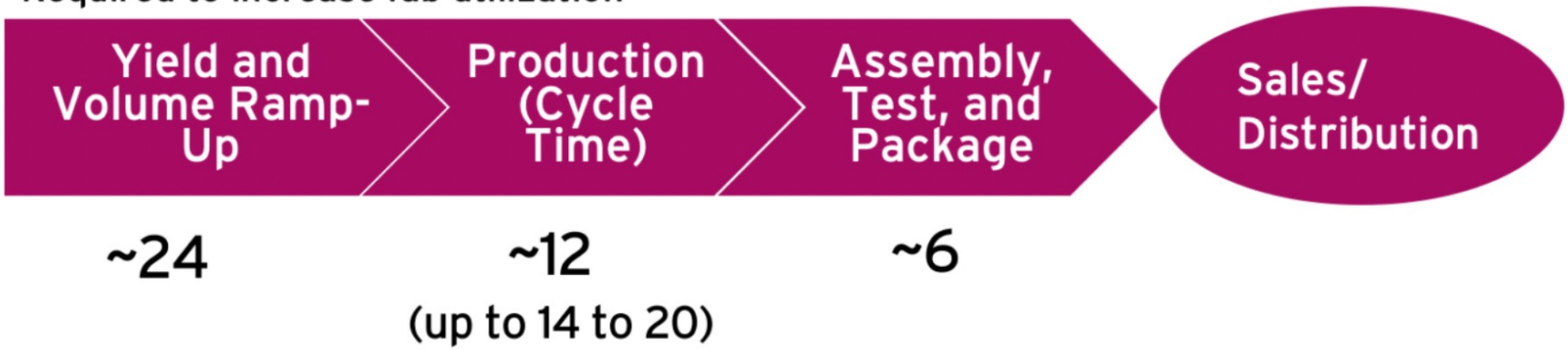
Fab Timescales

Jeff Drobman

SEMICONDUCTOR INDUSTRY ASSOCIATION

Semiconductor Fab Production Timescales

Required to increase fab utilization



Typical duration weeks	~24	~12 (up to 14 to 20)	~6

Wafer Fabs Today

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1968	❖ Intel
1978	❖ Micron**
1980	❖ Samsung
1987	❖ TSMC* (1st foundry)
2009	❖ AMD → Global Foundries*
2010	❖ Chartered → Global Foundries*
2014	❖ IBM → Global Foundries*
	❖ SMIC* (China)

*Pure Foundry

**Internal use only

Foundry Stats 2020

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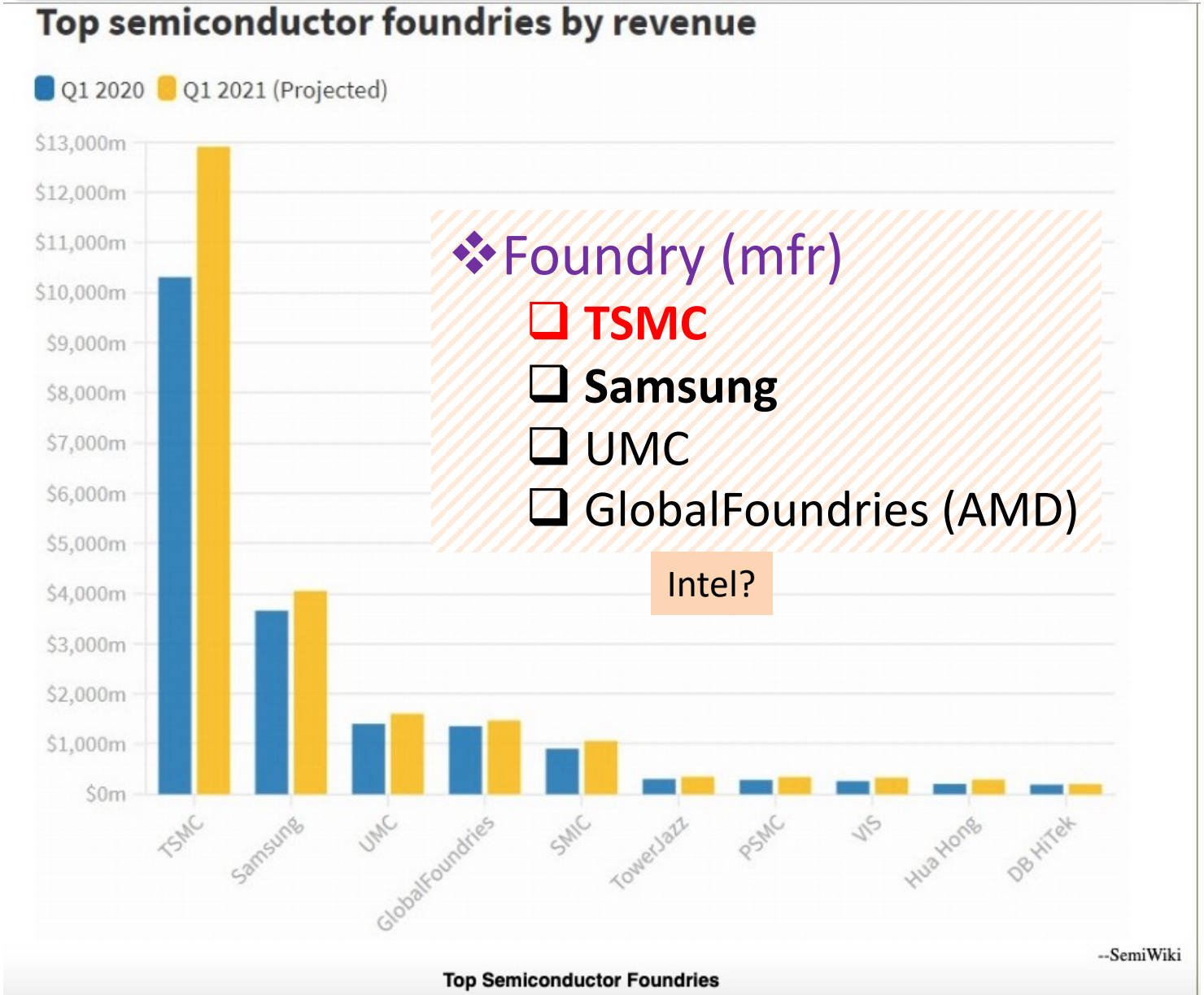

- Foundry (mfr)
  - **TSMC**
  - **Samsung**
  - UMC
  - GlobalFoundries (AMD)

Intel?

Foundry Shares 2Q22

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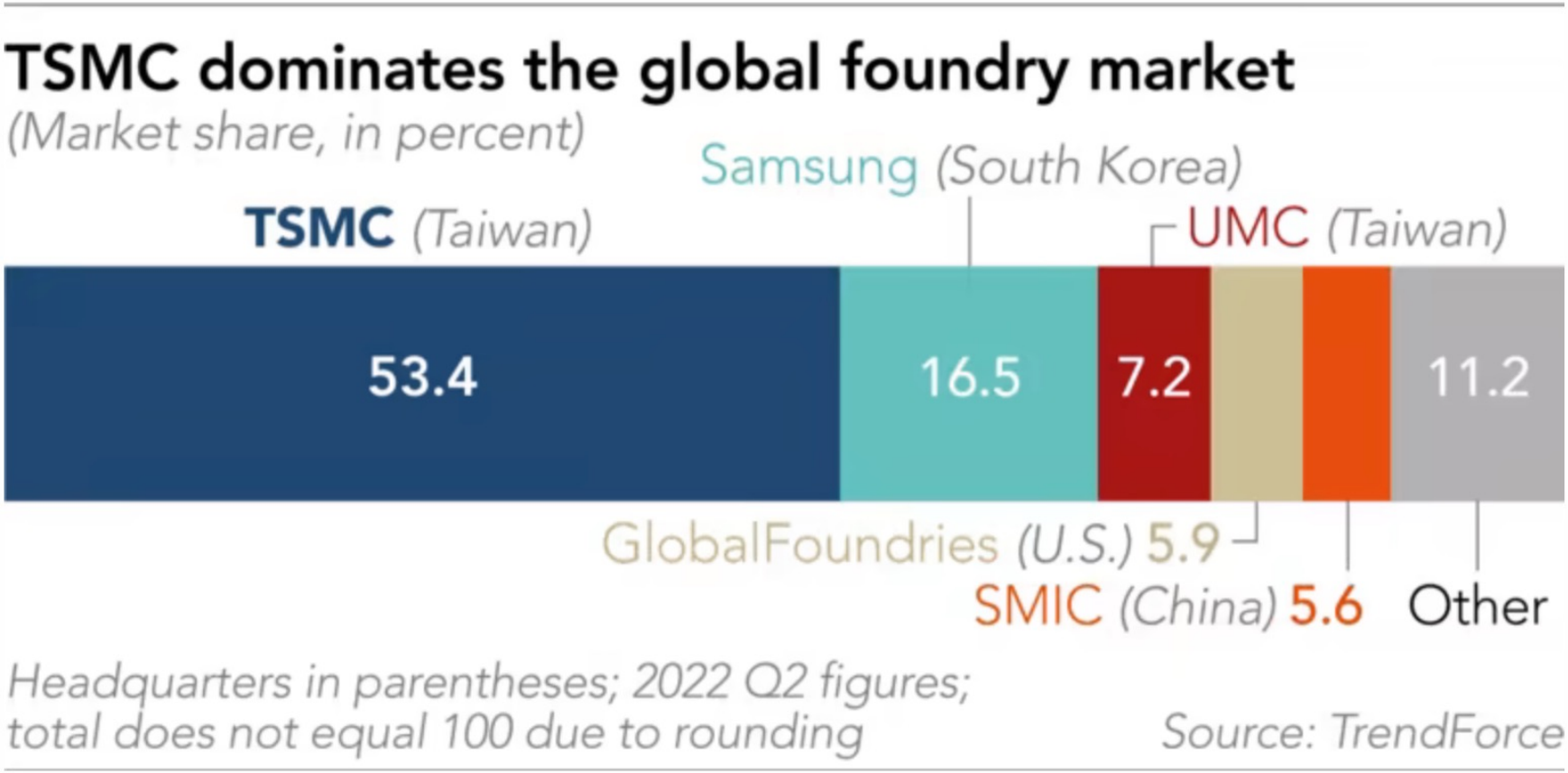

❖TSMC 1Q24 Revenue = $18.5B

Global Foundry $$$

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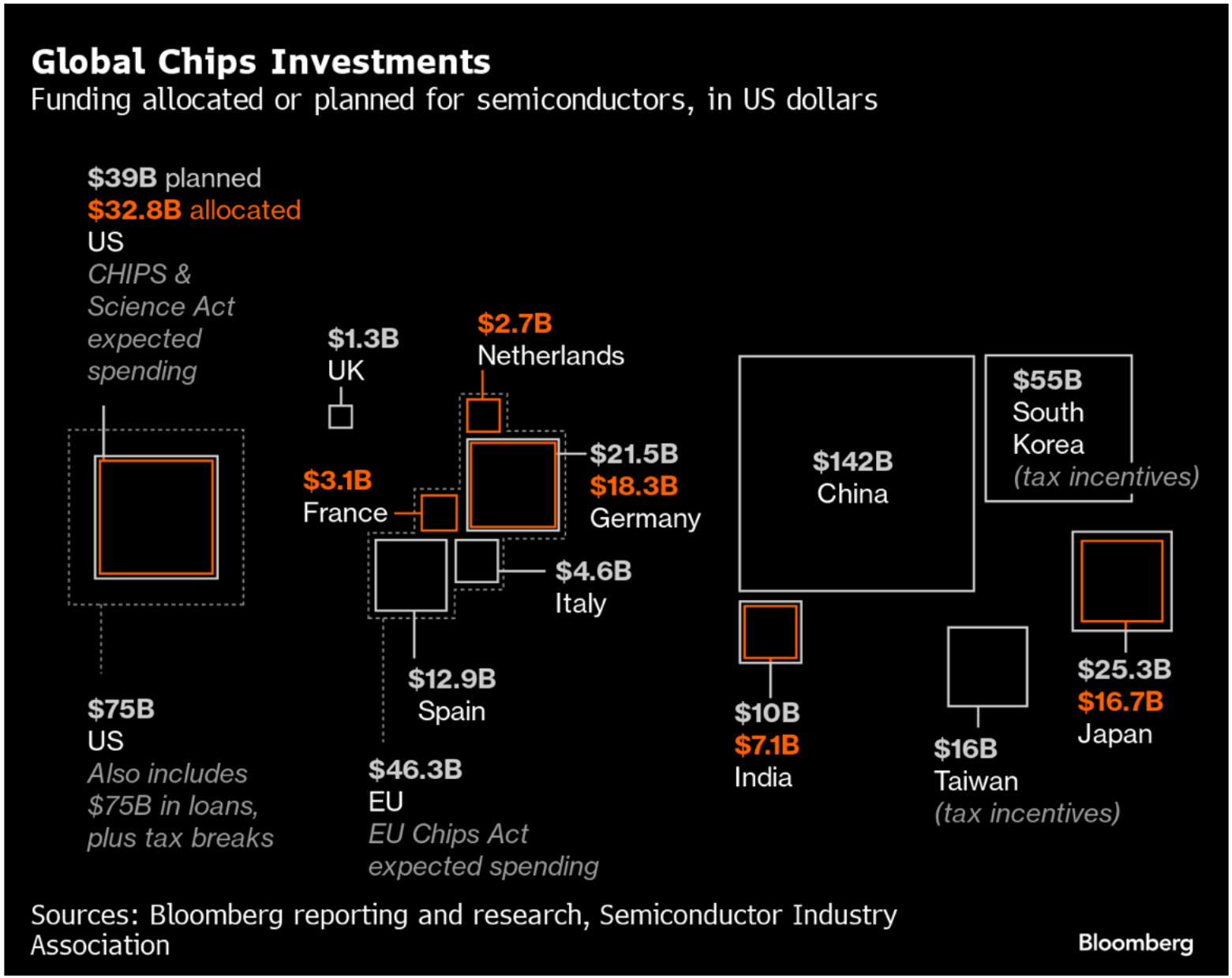

Foundry Share 2023

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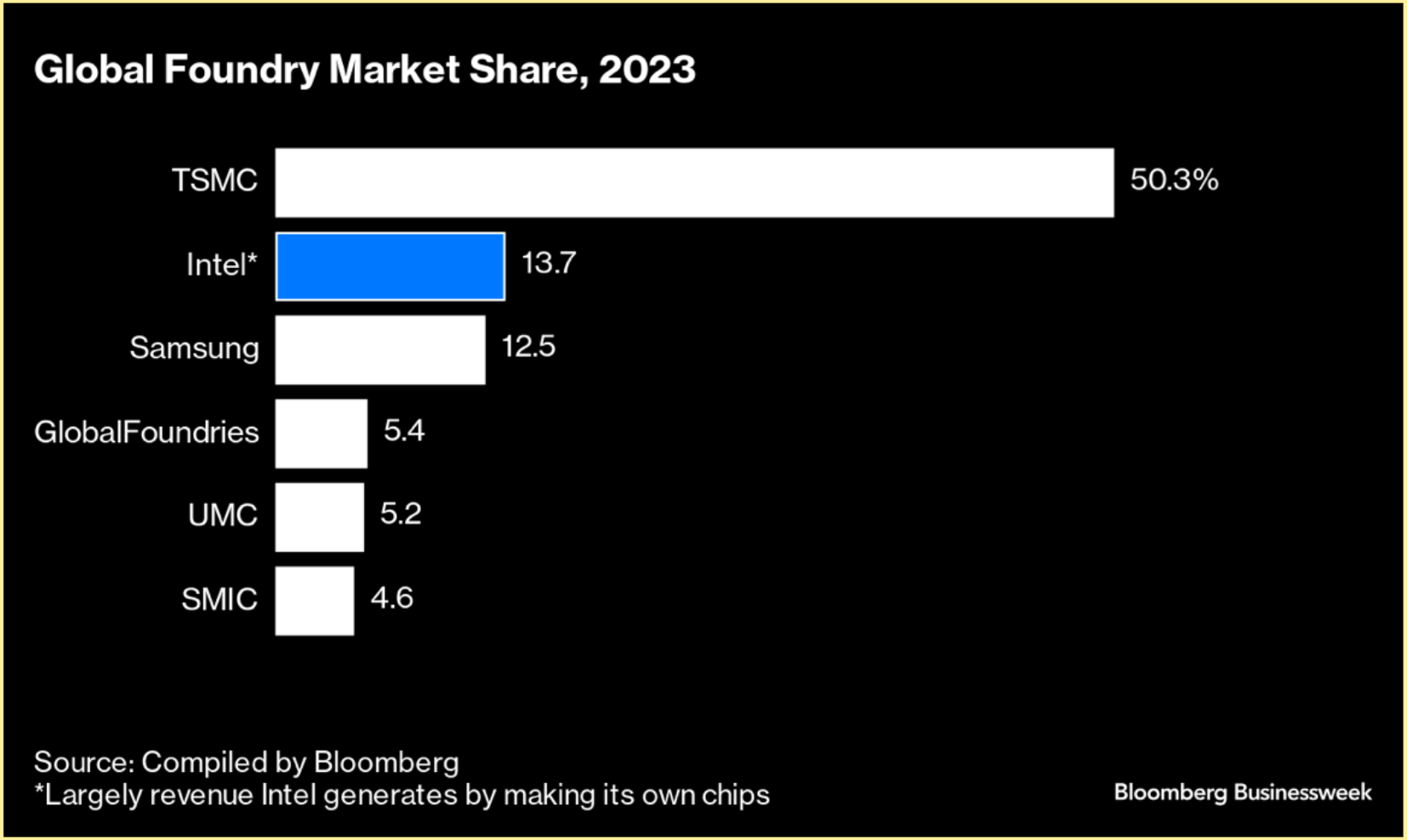
By Company



Foundry Share 2023

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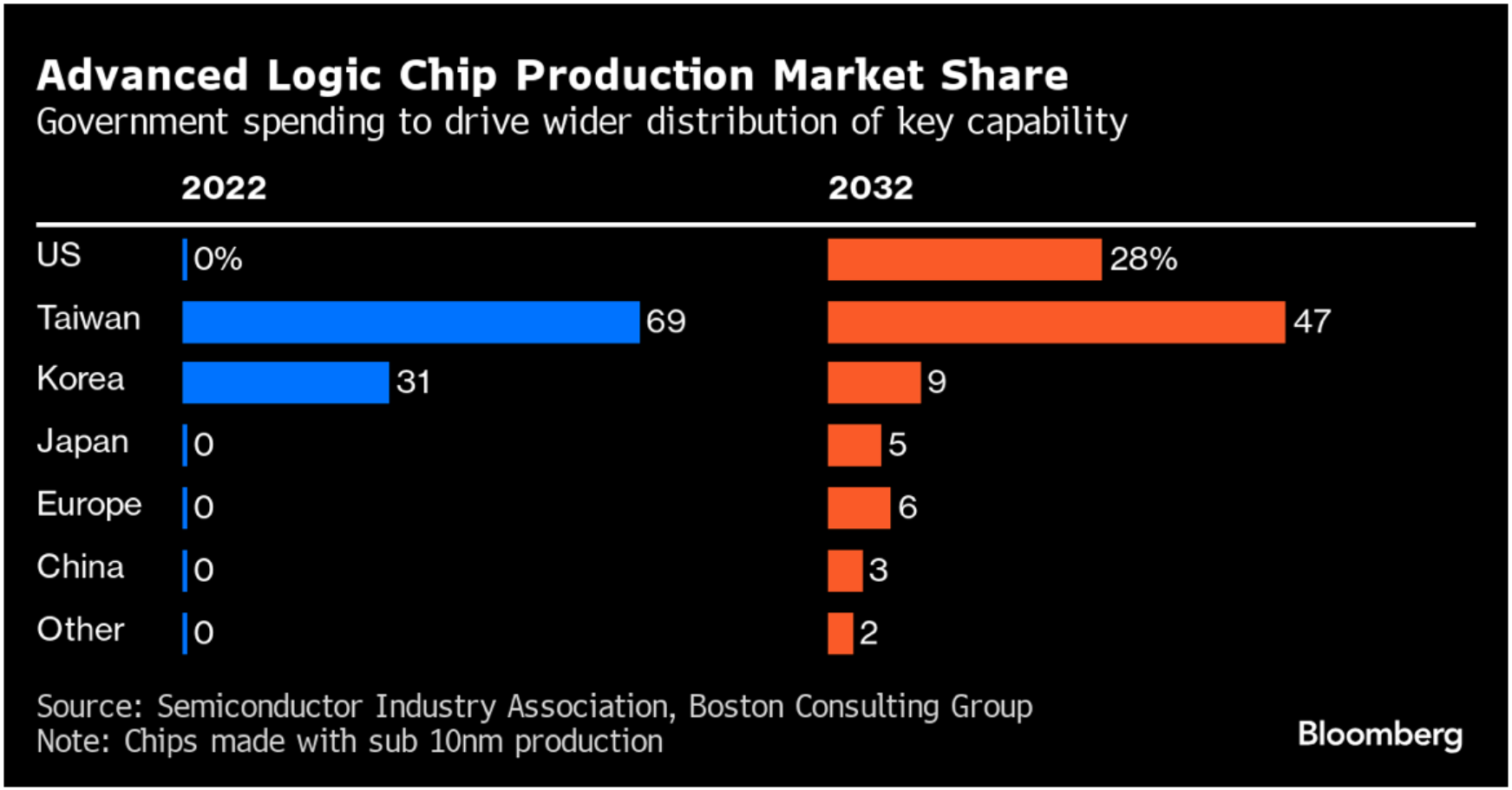
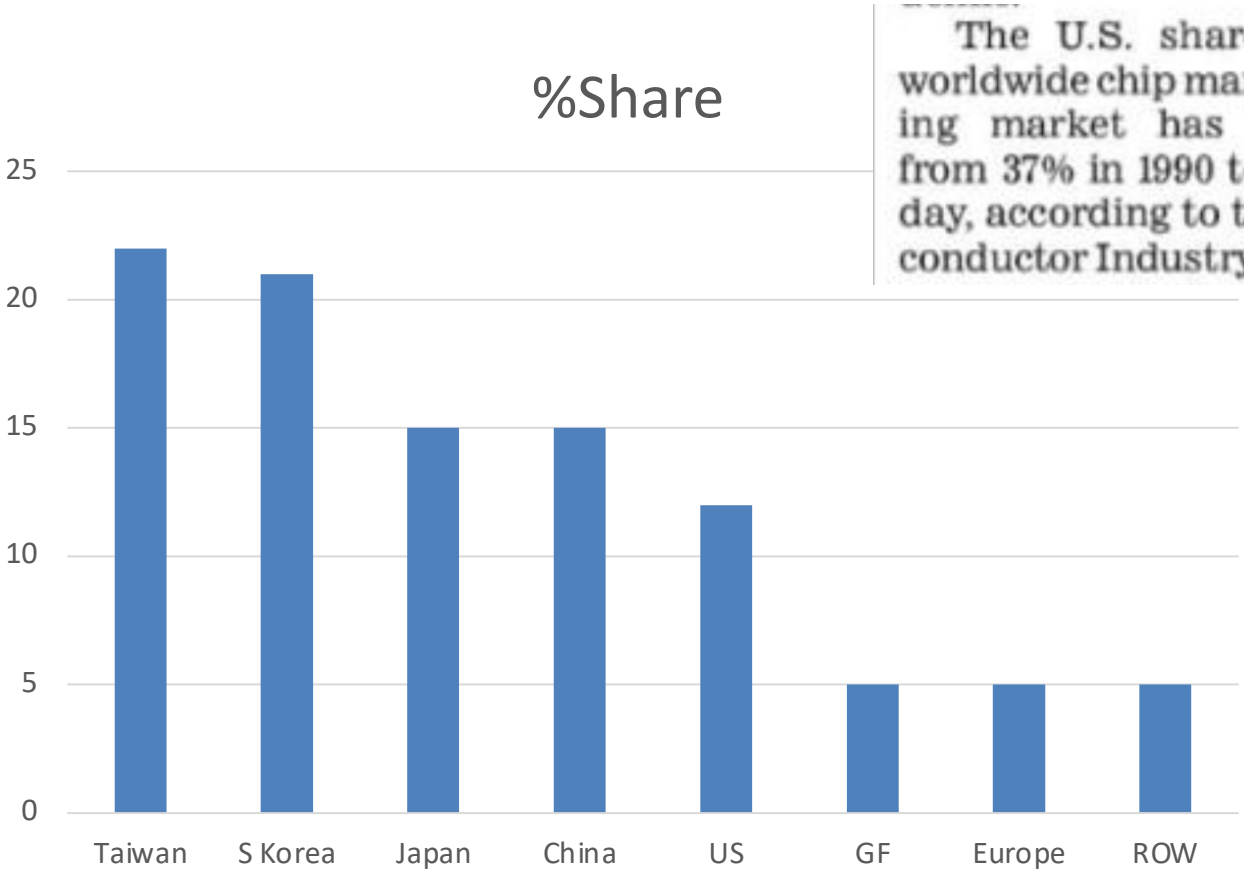
By Country



WW Fab Share by Region

Jeff Drobman



The U.S. share of the worldwide chip manufacturing market has declined from 37% in 1990 to 12% today, according to the Semiconductor Industry Assn.

Source: LA Times/SIA 1/22/22

WW Fabs

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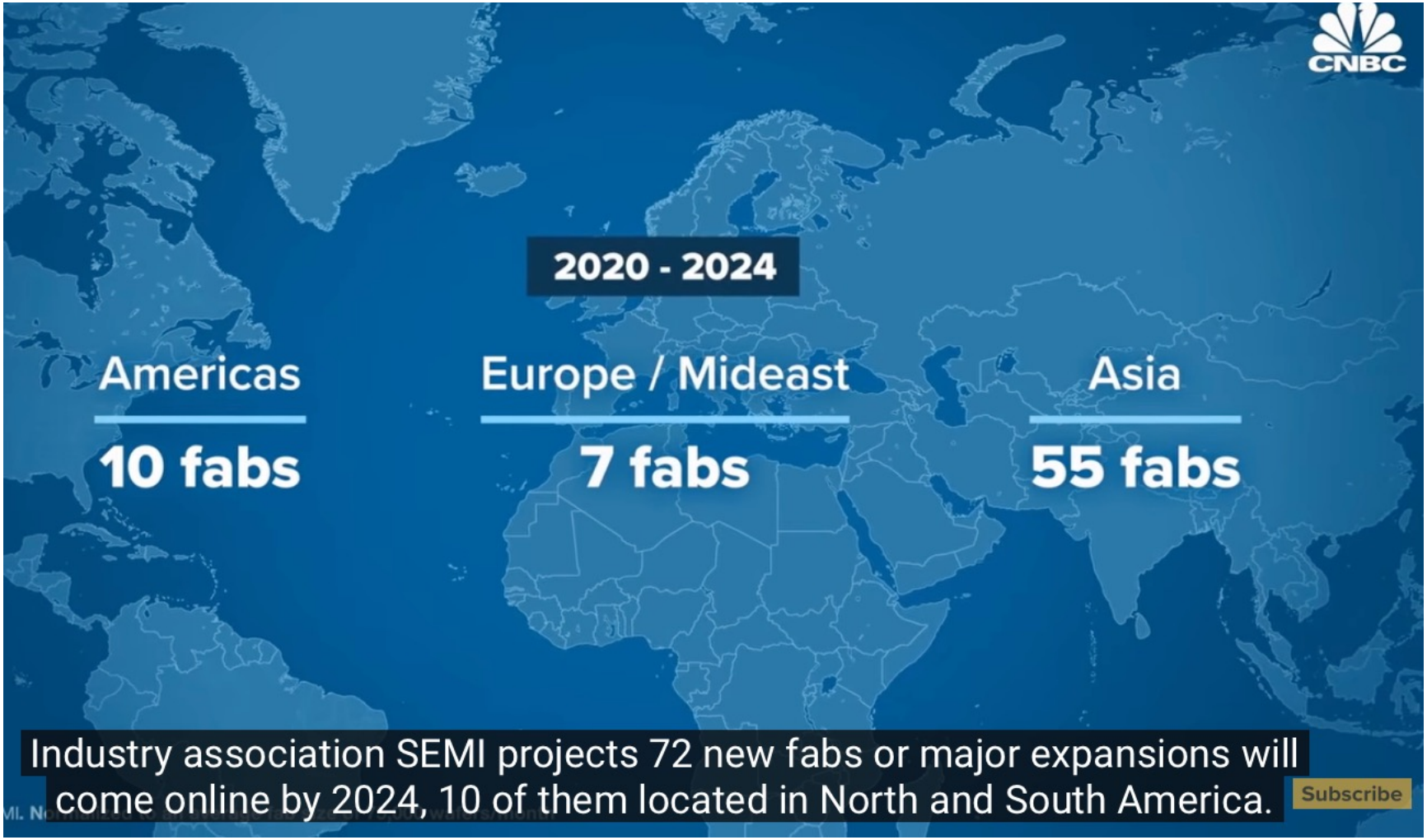

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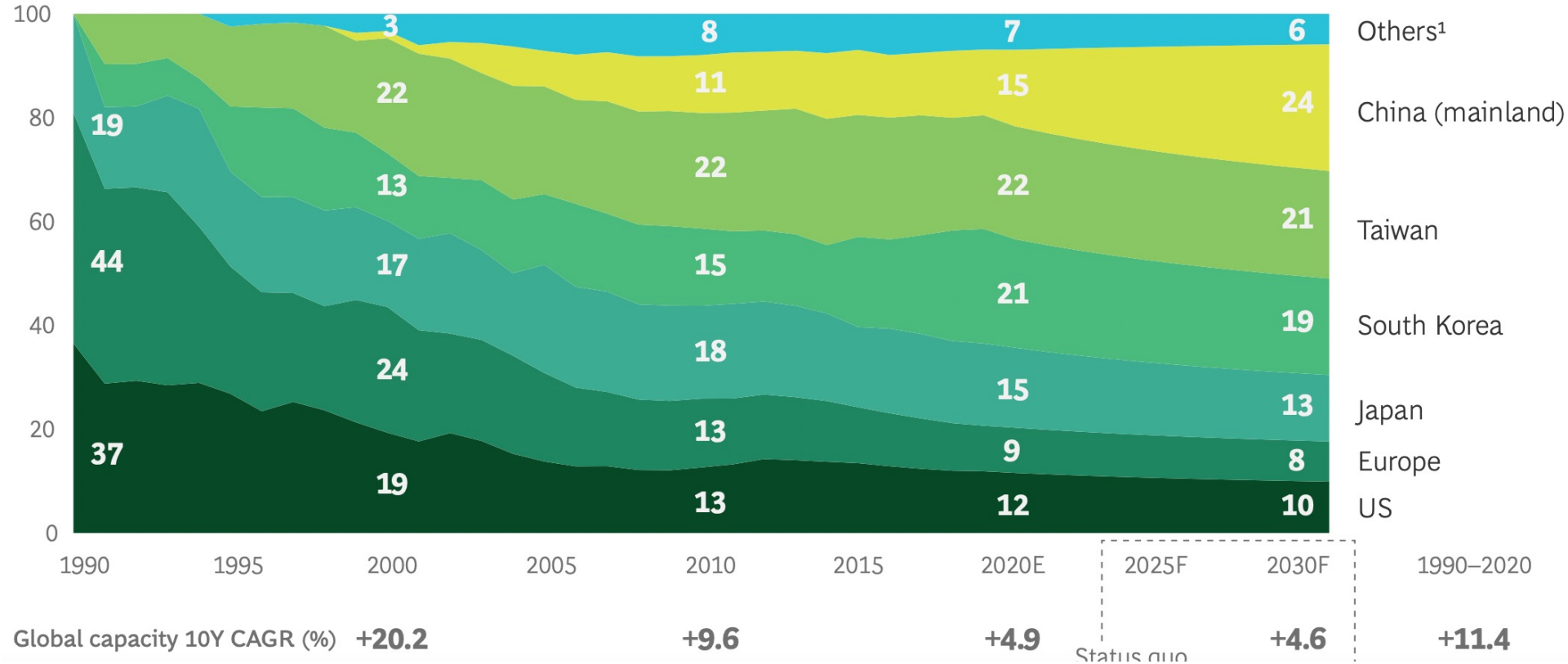
September 2020
By Antonio Varas, Raj Varadarajan, Jimmy Goodrich, and Falan Yinug

Global manufacturing capacity by location (%)



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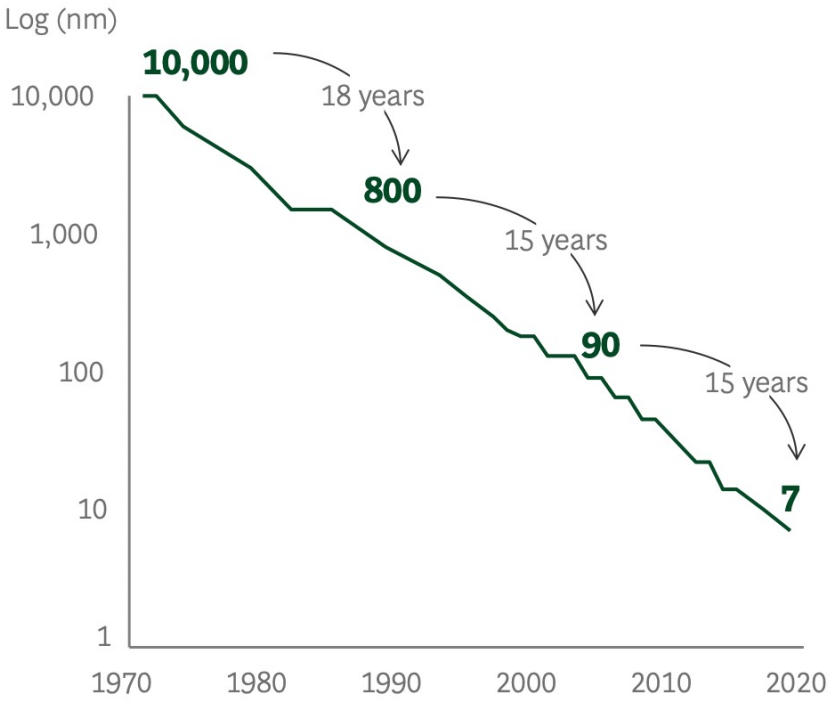
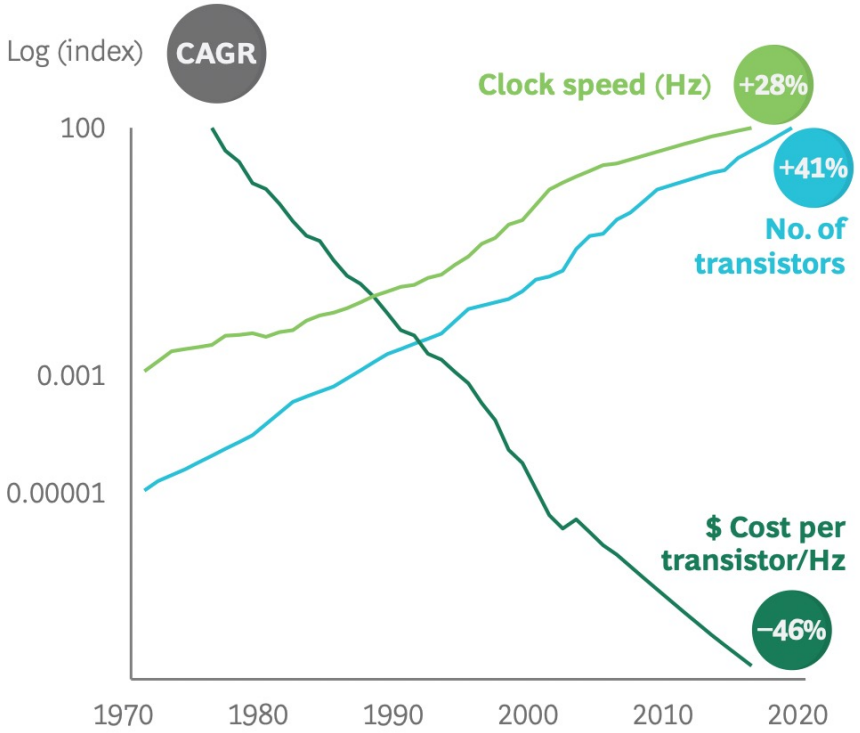
September 2020
By Antonio Varas, Raj Varadarajan, Jimmy Goodrich, and Falan Yinug

Evolution in manufacturing-process node



No. of transistors per microprocessor, performance and cost



Sources: Intel; Singularity.com; Wikipedia; BCG analysis.

Foundry Biz

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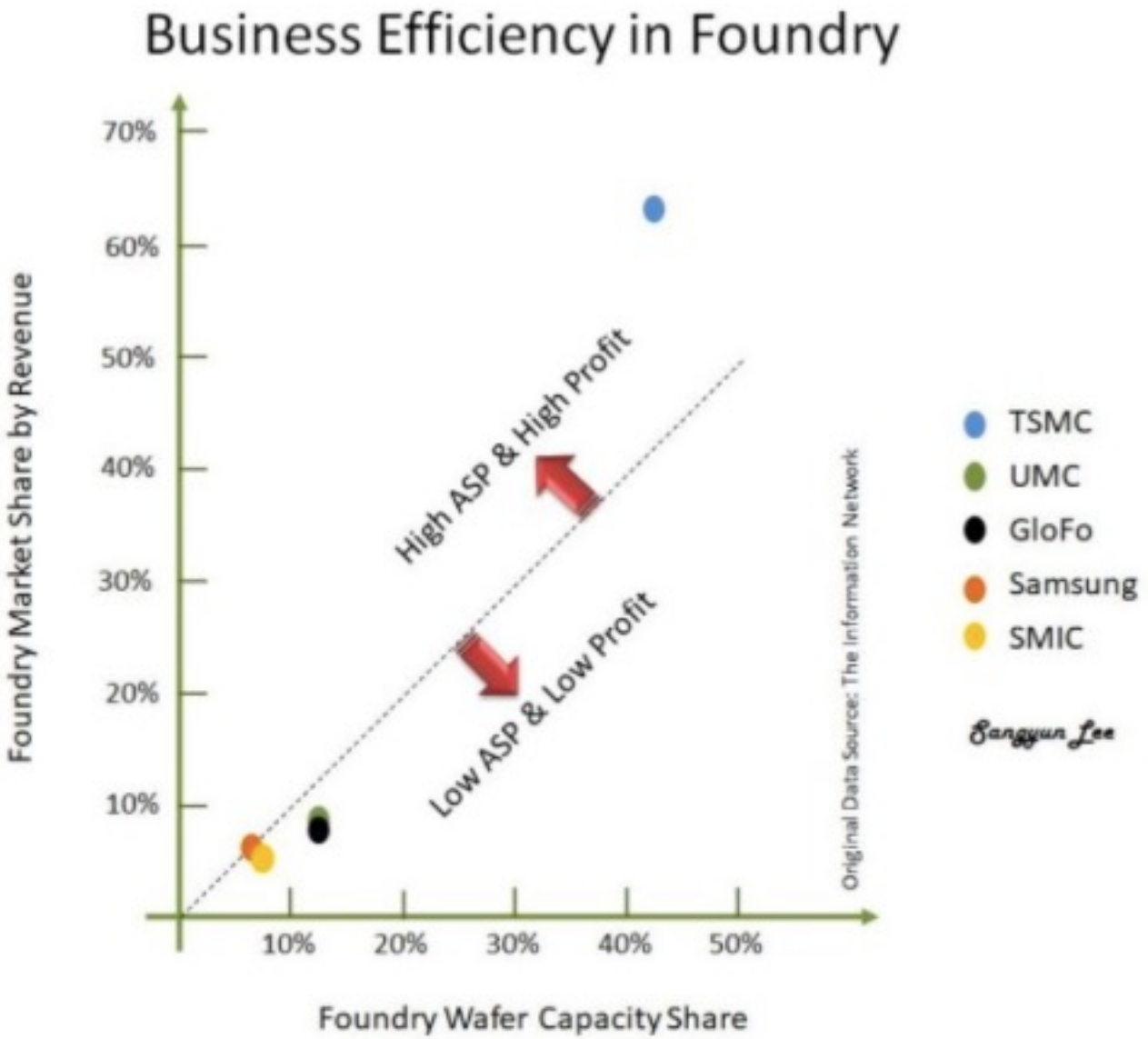

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Chip Fab:
Mask Making
ASML

ASML EUV Machines

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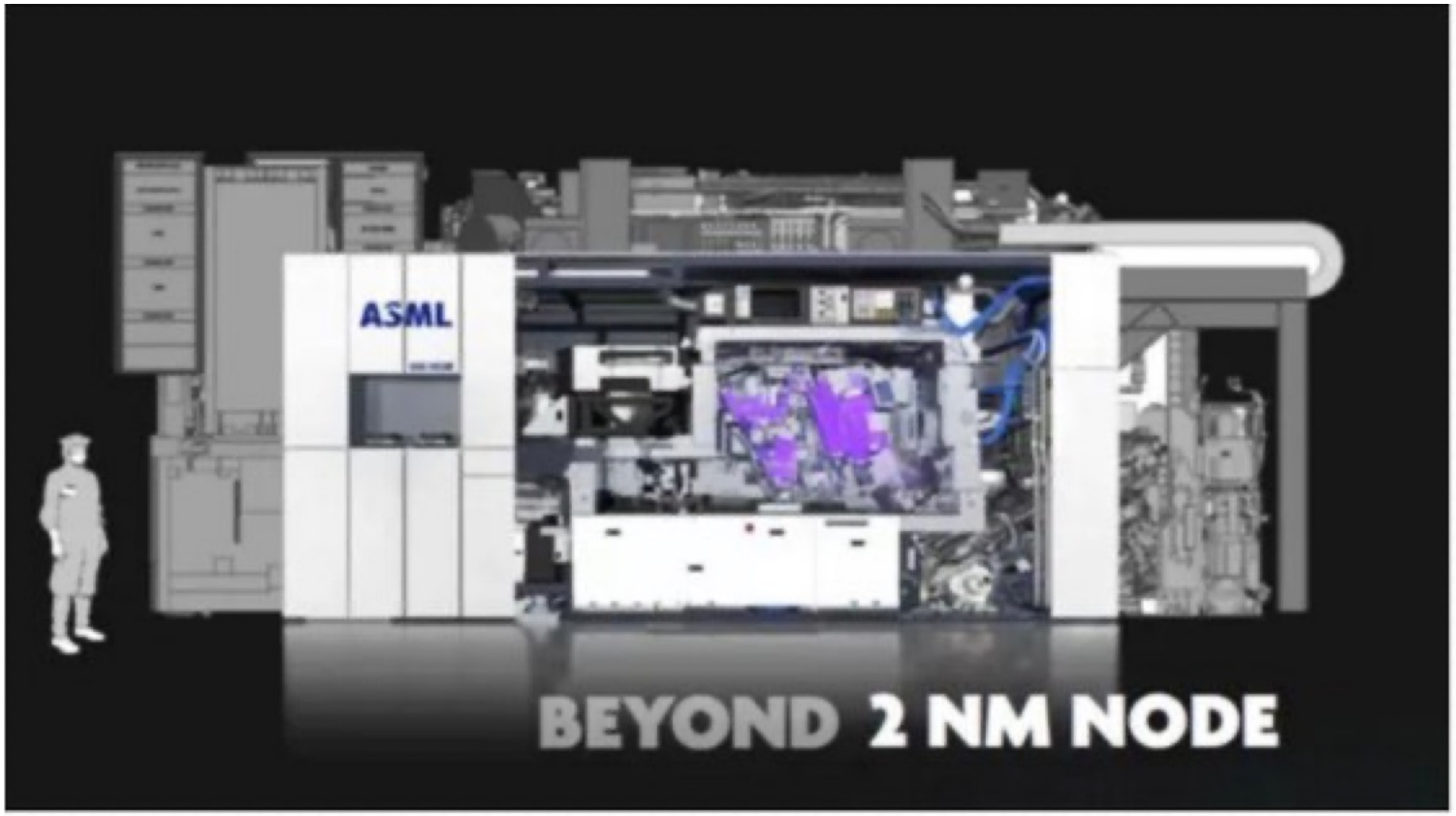
Quora



Current EUV lithography system (NA=0.33) (front) compared to the next generation of high NA EUV lithography system (NA=0.55) (back).

ASML EUV Machines

Quora

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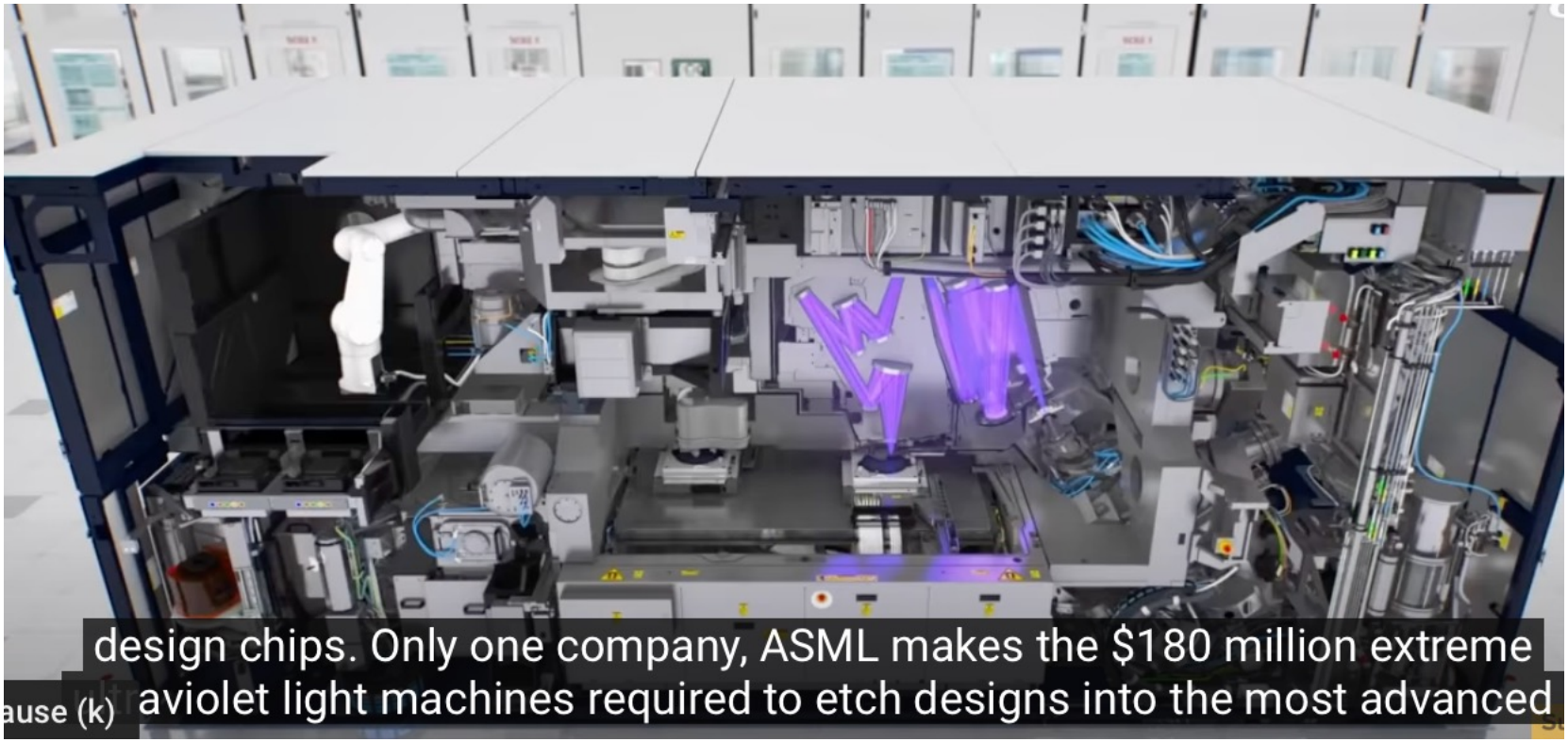

ASML: EUV for Mask Litho

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Jeff Drobman

SemiWiki
The open forum for semiconductor professionals

Semiconductor Advisors

Is ASML Immune from China Impact?
by Robert Maire on 10-21-2022 at 10:00 am
Categories: China, Lithography, Semiconductor Advisors, Semiconductor Services

ASML proves litho's place at Apex of semiconductor food chain

ASML announced a great quarter with Euro5.8B in revenue and EPS of Euro4.29/share. Outlook is for revenues of Euro6.1B to 6.6B with gross margins of 49%. Gross margin for 2022 will come in about 50% overall.

Most importantly, orders came in at a huge Euro8.9B, 77% logic, bringing backlog to a multi-year Euro38B. ASML is looking at shipping 60EUV and 375DUV systems in 2023, assuming supply chain issues are resolved.

ASML: EUV for Mask Litho

Jeff Drobman

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The open forum for semiconductor professionals

Semiconductor Advisors

Is ASML Immune from China Impact?
by Robert Maire on 10-21-2022 at 10:00 am
Categories: China, Lithography, Semiconductor Advisors, Semiconductor Services

China immunity from two factors

ASML will have 5% or less impact next year from the China issue for two simple reasons; number one, the majority of current business is non leading edge, above 14NM as ASML was already not shipping any EUV tools to China. Number two, ASML is sold out anyway and there are a large number of customers who will happily snap up any systems that China doesn't or can't take.

In our view, as we had previously commented on months ago, ASML is virtually immune to China embargo issues given their leading positioning in the industry. The semiconductor industry remains a zero sum game and litho systems not shipped to China will go elsewhere to satisfy demand.

ASML: EUV for Mask Litho

Jeff Drobman

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Semiconductor Advisors

Is ASML Immune from China Impact?
by Robert Maire on 10-21-2022 at 10:00 am
Categories: China, Lithography, Semiconductor Advisors, Semiconductor Services

Light source technology is developed by former Cymer, in San Diego, that ASML was allowed to buy by the US government. We are relatively certain that there were agreements regarding Cymers technology in order to win acquisition approval.

Many investors may not be aware that much if not most of the laser technology, especially for EUV, arose out of the "star wars" laser weapons systems of the Regan era as Cymer employed many scientists out of the ex star wars program from both the US and former Soviet Union. The technology used in the 250KW drive laser in EUV systems could be re-purposed for military applications.

77% logic mix shows resilience

The fact that 77% of orders are from logic suggests that a more rapid slowdown in memory will not impact ASML at all. Management also announced orders for High NA systems along with regular EUV systems. Though high NA was not broken out, at over Euro300M a system, the numbers can add up more than twice as fast as DUV systems. We assume that TSMC, Intel and Samsung have likely already ordered multiple High NA EUV systems. TSMC's recent capex cut clearly is not impacting their litho system orders as they understand the import of leading in litho.

ASML EUV Roadmap

Quora

EUV product roadmap

Wavelength	NA, Half pitch	2020	2021	2022	2023	2024	≥2025
EUV	0.33 NA, 13 nm	NXE:3400C 1.5 nm | 135 wph[1] / 145 wph[2]	NXE:3600D 1.1 nm | 160 wph		NXE:3800E <1.1 nm | >195 wph / 220 wph[2]		NXE:4000F <0.8 nm | >220 wph
	0.55 NA, 8 nm				EXE:5000 at ASML fab	EXE:5000 <1.1 nm | 150 wph[3]	EXE:5200B <0.8 nm | 220 wph

Wafers/hours (wph) are at dose 30mJ/cm² unless specified otherwise.
1) 170wph@20mJ/ cm²
2) Including throughput upgrade
3) 185wph@20mJ/ cm²

Product: Matched Machine Overlay (nm) | Throughput (wph)
Product status: Released | Development | Definition

ASML

SPIE. ADVANCED LITHOGRAPHY | For High NA, see: SPIE 12051-6
High NA EUV enabling cost efficient scaling for N+1 technology nodes, Greet Storms et al.

Page 15
Public

Figure 5. System Roadmap.

ASML EUV Mask Count

Jeff Drobman

Quora

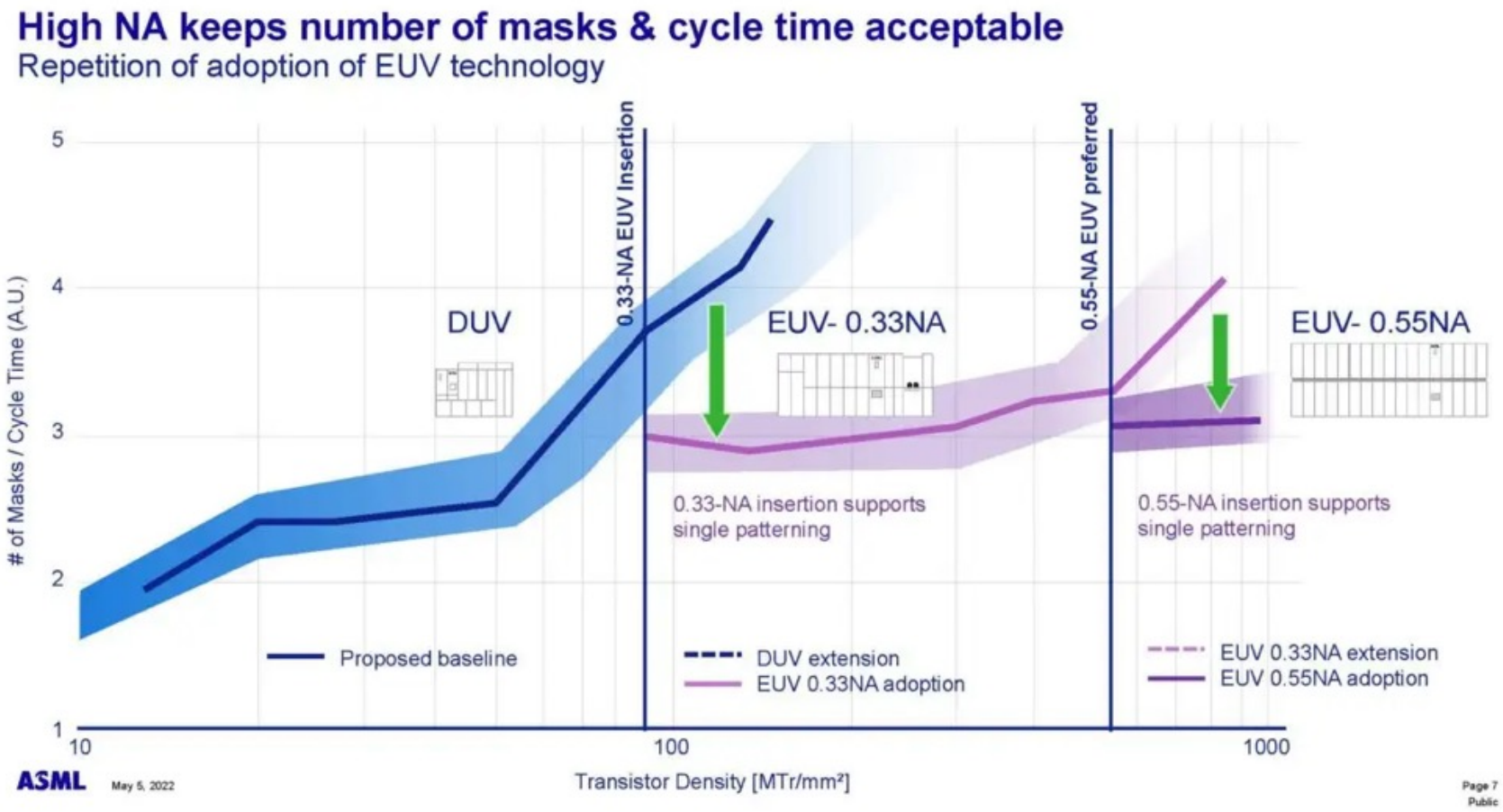

Figure 8. Mask Count Trends.

ASML EUV Wafers Out

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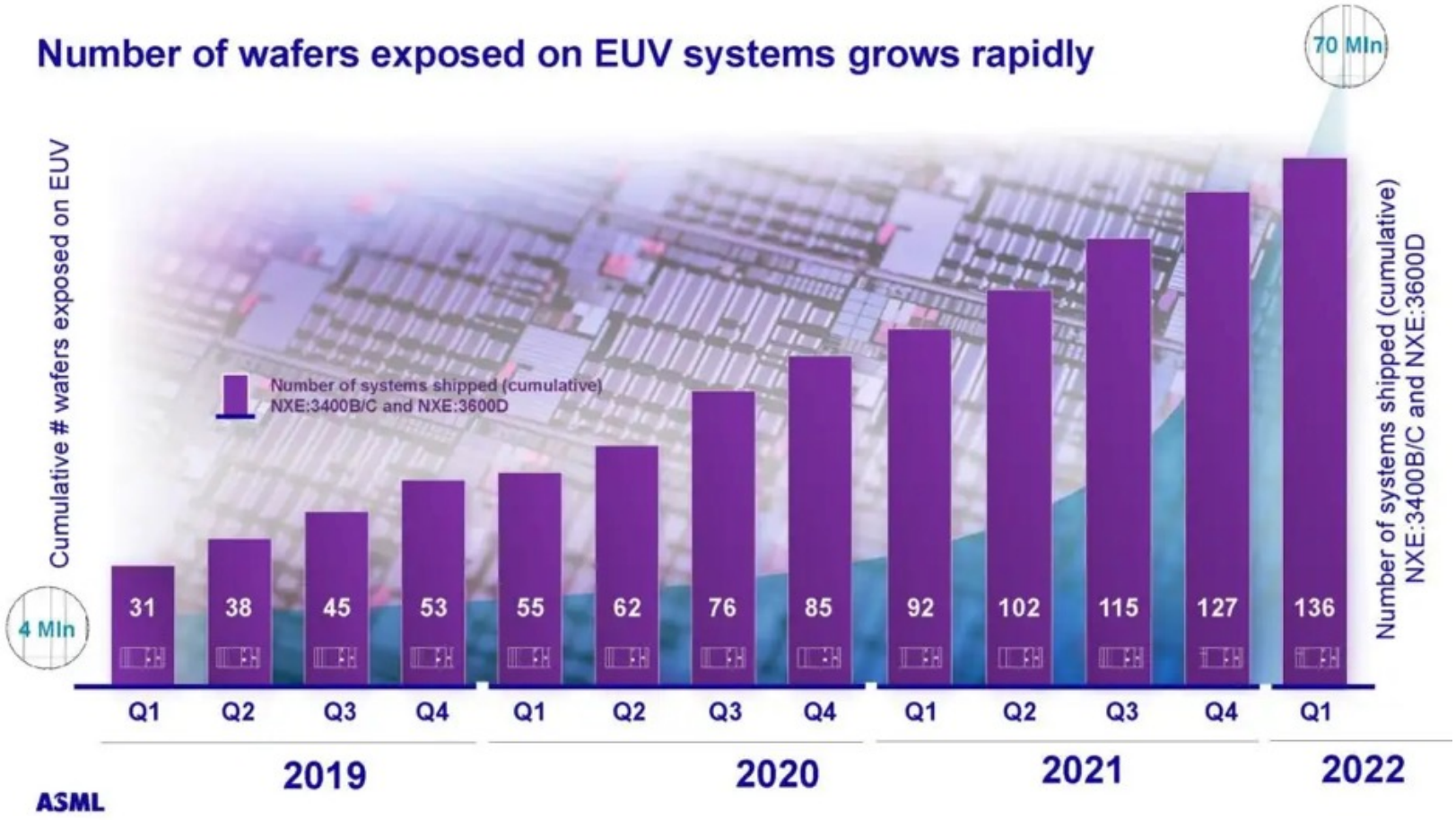

Figure 2. Number of EUV Wafers Exposed.

Chips/Fabs

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Chip Design/Fab

AMD/Intel

Fabs – AMD, Intel

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AMD Sunnyvale Fab 1 1970

$1M

Cost x10,000 in 40 years
averages to
250x per year

$10B

Intel's latest Fab in Hillsboro

An aerial view of Ronler Acres, Intel's largest silicon research and development hub.

Chip Fab

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INDIE APP DEVELOPER
Jeff Drobman

Bob McConnell
Former VP and Site Manager, Heilbronn, Germany at Atmel (company) (2003–2009) · Wed

Silicon wafer chip defects are said to happen on all chips produced. How/why does this occur, and are there ways to prevent it?

First, read Wikipedia: Semiconductor Device Fabrication. I think it explains the issues at a basic level. Secondly, there are many places for defects to occur. They DO NOT occur on the basic patterning information because that is computer generated. If it doesn't check out correctly the pattern is regenerated. The wafer can have defects due to crystal growth anomalies. This is very unlikely and causes negligible failures.

Particles are at a very low level. The wafers being processed are moved between process steps in sealed, super clean boxes. The boxes are only opened inside machines that are sealed and or have positive pressure.

Chip Fab

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Bob McConnell
Former VP and Site Manager, Heilbronn, Germany at Atmel (company) (2003–2009) · Wed

The processing of a wafer involves deposition or growth in various ways of well over a hundred or more layers of material. This includes photoresist to be exposed as part of the photo lithography process, oxide layers that are grown to be later patterned and etched, metal layers to be patterned and have the interconnect defined, and dielectric layers to be insulators between the metal layer. The dielectric layers are patterned to produce the interconnect between metal layers.

Any of these layers might have a defect caused by a flaw in the material or by a particle that somehow escaped all the controls and filters. The processes are adjusted to, as much as possible, eliminate these defects. A photo layer might be processed twice through a photo lithography step. There might be a high temperature step to allow a material to flow and close a defect. (only works when that high temp doesn't hurt any thing below the current layer) This has been the basic fight of the industry to keep allowing transistor counts to increase. Looking out 4 years and doing some math tells the process engineer and equipment engineer what has to happen to stay on that exponential curve of Moore's Law.

Chip Design vs Mfg

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Is designing computer chips the same as planning how to manufacture them?

Jeff Drobman, Lecturer at California State University, Northridge (2016-present)

Answered just now

there are many levels of design for all digital systems, including hardware and software. chips have CPU cores, GPU cores, cache memories, I/O, system logic and clocking, etc. first level is the “macro” architecture: layout of all those subsystems. Cores may be licensed (designed by others) or designed from scratch. other subsystems are usually licensed from the fab or others.

It is the design of the cores and other subsystems that is the most intricate design process. Each item needs to follow the detailed “design rules” given by the selected fab (manufacturer), as well as their interconnections.

AI in Chip Design

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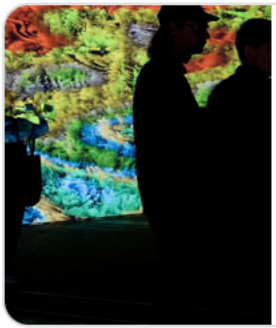
INDIE APP DEVELOPER
Jeff Drobman

8-31-21

Chuck Bluestein, A great deal of non-fiction reading.

Answered 34m ago

Here is an article that talks about this that you can read and share with others. The name of the article is:



Opinion: Computer chips are getting so advanced, companies are using artificial intelligence to make them

The introduction of AI in chip design is a necessity for performance an...

https://www.marketwatch.com/story/computer-chips-are-getting-s...

This is what the article says on it:

> **Thanks to a machine-learning technique known as reinforcement learning , artificial intelligence completed the task in only six hours, compared with weeks by humans.**

Foundries

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Intel

Founded 1968

Intel Fabs

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Fab name	Fab location	Production start year	Process (wafer, node)
D1B	USA, Oregon, Hillsboro	1996	300mm, Development
RB1	USA, Oregon, Hillsboro	2001	300mm, Development
D1C	USA, Oregon, Hillsboro	2001	300mm, Development
RP1	USA, Oregon, Hillsboro	2001	300mm, Research
D1D	USA, Oregon, Hillsboro	2003	300mm, Development
D1X	USA, Oregon, Hillsboro	2013	300mm, Development
Fab 11X	USA, New Mexico, Rio Rancho	1995 upgrade 2020/2021 with 22/14	300mm, 45 nm/32 nm, Packaging
Fab 12	USA, Arizona, Chandler	2006	300mm, 22 nm/14 nm/10 nm
Fab 22	USA, Arizona, Chandler	2002	300mm, 22 nm/14 nm/10 nm
Fab 24	Ireland, Leixlip	2006	300mm, 14 nm[2]
Fab 28a	Israel, Kiryat Gat	1996	300mm, 22 nm
Fab 28	Israel, Kiryat Gat	2023	300mm, 22nm/14nm/10nm[3][4]
Fab 38	Israel, Kiryat Gat	2024	300mm, 22 nm[5]
Fab 32	USA, Arizona, Chandler	2007	300mm, 22 nm/14 nm/10 nm
Fab 34	Ireland, Leixlip	2023	300mm, 7 nm[6]
Fab 42	USA, Arizona, Chandler	2020	300mm, 10 nm/5 nm (2024)
Fab 52	USA, Arizona, Chandler	(2024)[7]	300mm, 7 nm
Fab 62	USA, Arizona, Chandler	(2024)[7]	300mm, 5 nm
	USA, Ohio, Licking County	(2024-2025)	300mm, 5 nm
SC2	USA, California, Santa Clara		Reticle/Masks, Intel Mask Operations[8]
	Malaysia, Kedah, Kulim	(2024)	300mm, Packaging[9]
	Germany, Magdeburg, Saxony-Anhalt	(2027)	[10]
	Italy	(2025-2027)	300mm, Packaging[11]

Chip Shortage

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Intel New Fabs in Phoenix

Intel New Fabs

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INDIE APP DEVELOPER
Jeff Drobman

Intel Breaks Ground on Two New Leading-Edge Chip Factories in Arizona

Daniel Nenni · Today at 5:44 AM

Daniel Nenni

ADMIN

Staff member

Today at 5:44 AM

New $20 billion capacity expansion will bring Intel's total Arizona investment to more than $50 billion.

Intel CEO Pat Gelsinger signals to the crowd from earth-moving equipment in Chandler, Arizona, on Friday, Sept. 24, 2021, for a groundbreaking ceremony to celebrate the largest private-sector investment in Arizona's history. The construction of two new computer chip factories is a $20 billion project that will bolster U.S. semiconductor leadership and help bring geographical balance to the global supply chain. (Credit: Intel Corporation)

Intel New Fabs

DR JEFF SOFTWARE
INDIE APP DEVELOPER
Jeff Drobman

September 24, 2021 03:21 PM Eastern Daylight Time

CHANDLER, Ariz.--(BUSINESS WIRE)--**What's New:** Intel today broke ground on two new leading-edge chip factories at the company's Ocotillo campus in Chandler, Arizona. In a groundbreaking ceremony attended by senior government officials and community leaders, Intel CEO Pat Gelsinger celebrated the start of construction on the largest private investment in state history and reiterated the company's commitment to investing in U.S. semiconductor leadership.

"Today's celebration marks an important milestone as we work to boost capacity and meet the incredible demand for semiconductors: the foundational technology for the digitization of everything. We are ushering in a new era of innovation – for Intel, for Arizona and for the world. This $20 billion expansion will bring our total investment in Arizona to more than $50 billion since opening the site over 40 years ago. As the only U.S.-based leading-edge chipmaker, we are committed to building on this long-term investment and helping the United States regain semiconductor leadership."

–Pat Gelsinger, Intel CEO

Why It's Important: Advanced domestic chipmaking capacity and capabilities are critical for the sake of both economic and national security. The United States has lost ground in semiconductor manufacturing and is at risk of falling farther behind. With its new IDM 2.0 strategy, Intel is doing its part to help rebuild U.S. leadership and bring more balance to the global supply chain. Intel is the only semiconductor manufacturer with leading-edge process and packaging research capabilities in the United States, and the company is investing in domestic capacity to support the surging worldwide demand for chips across multiple segments, from PCs to automobiles to the data center and more.

Intel New Packaging

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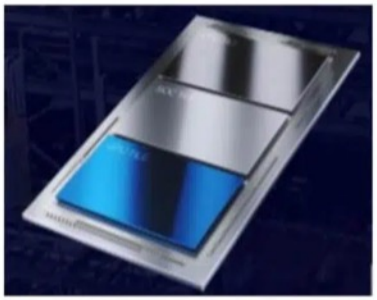
INDIE APP DEVELOPER
Jeff Drobman

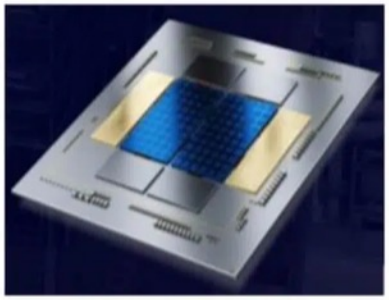
Chiplets (MCM)

Intel's Heterogenous System-in-Package Examples

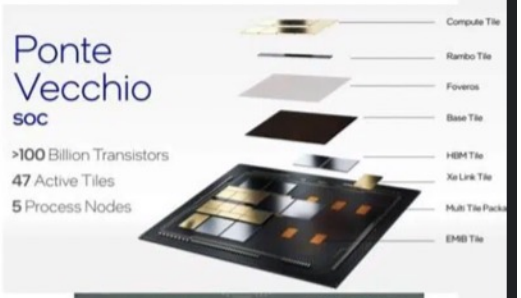
Intel Agilex™ (FPGA)
EMIB Technology

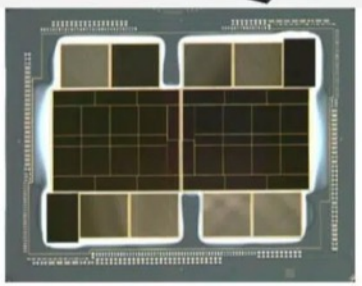


Intel Meteor Lake (Client)
Foveros Technology



Intel Granite Rapid (Server)
EMIB Technology





Ponte Vecchio – Xᵉ (HPC)
EMIB+Foveros Technologies

Heterogenous Packaging Technology Enabling Products Across All Market Segments

Sapphire Rapids is slated to be the first lineup from Intel to adopt the chiplet (MCM) or tiled design (plus some SKUs using on-die HBM) and Granite Rapids refining it. The former is expected to feature up to four (15-core, 1 disabled) tiles, resulting in a total core count of 56.

Intel New Processes

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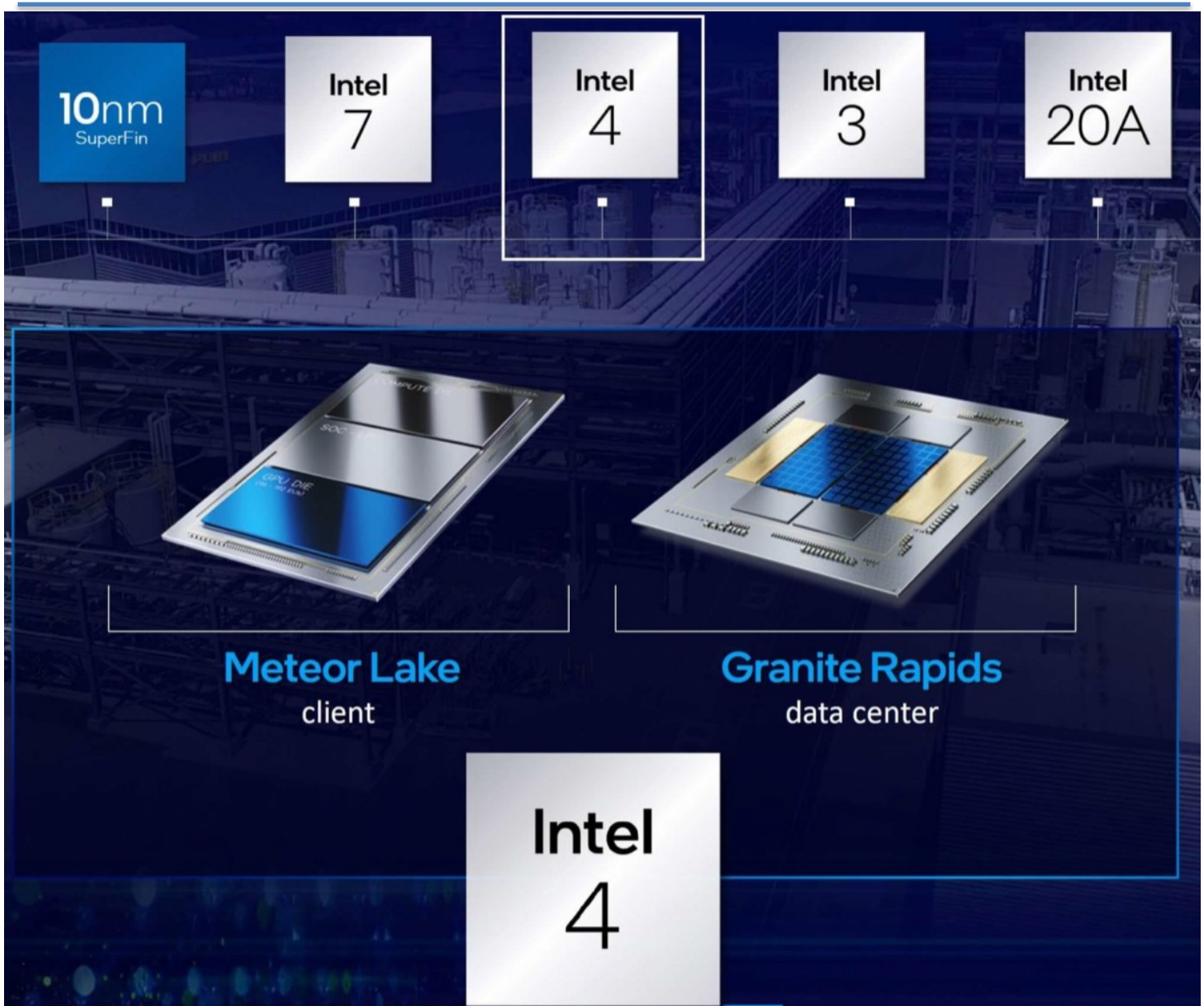
INDIE APP DEVELOPER
Jeff Drobman



Intel's New Foundry Strategy

The central tenants of IDM 2.0 for Intel are:

1. Utilize the Intel internal factory network to build the majority of Intel's products internally.
2. Expand use of foundries so that all products have some level of foundry production.
3. Increasing engagement with TSMC, Samsung, GLOBALFOUNDRIES (GF) and UMC.
4. Plan to be a major foundry with US and European based manufacturing to balance the reliance on Asia.

There was slide that showed something like 80% of leading edge in Asia centered around Taiwan and South Korea, 15% in the US and 5% in Europe.

Intel’s New Foundry Strategy

DR JEFF SOFTWARE
INDIE APP DEVELOPER
Jeff Drobman

Intel is said to have made a $2B takeover offer for chipmaker SiFive?!?!?

Daniel Nenni · Thursday at 11:51 AM

Daniel Nenni

ADMIN

Staff member

Thursday at 11:51 AM #1

Intel is said to have offered to purchase SiFive for more than $2B. SiFive, a designer of semiconductors, has been talking to its advisors to see how to proceed, according to a Bloomberg report, which cited people familiar. SiFive has received multiple bids from other interested parties and has also received offers for an investment. SiFive last raised more than $60M in a Series E financing round last year and was valued at about $500M, according to PitchBook. In June 2019, Qualcomm (NASDAQ:QCOM) participated in a $65.4M Series D round for SiFive, a fabless semiconductor company building customized silicon based on the open RISC-V instruction set architecture.

Wow, great move if it is true. If Intel wants to get into the foundry business doing turnkey ASICs is definitely the way to go. Intel already acquired eASIC. That way Intel can closely control and protect IP and make sure designs/chips are done the Intel way, absolutely.

The ASIC business has changed quite a over the last couple of years as fabless chip companies take control (Marvell, Broadcom, and Mediatek). Exciting times in the semiconductor ecosystem, absolutely!

Intel Process Nodes

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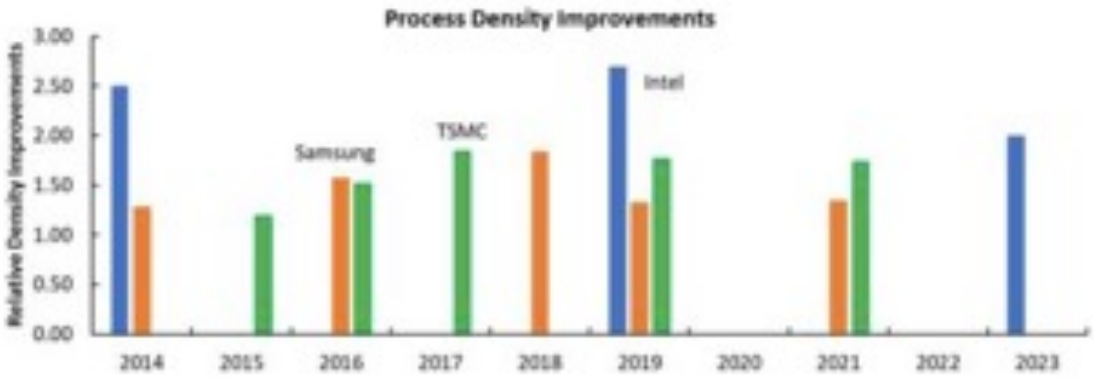
Slower Node Transitions Versus Foundries

IC KNOWLEDGE LLC

	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023
Intel	14nm					10nm				7nm
Samsung	14nm		10nm		7nm	5nm			3nm	
TSMC		16nm	10nm	7nm		5nm		3nm		2nm?

- Intel takes bigger density jumps but less often.
- TSMC and Samsung take smaller jumps more frequently, 5 nodes versus Intel's 3.



3/24/2021 4

Figure 4. Node Introductions.

Intel Process Nodes

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INDIE APP DEVELOPER
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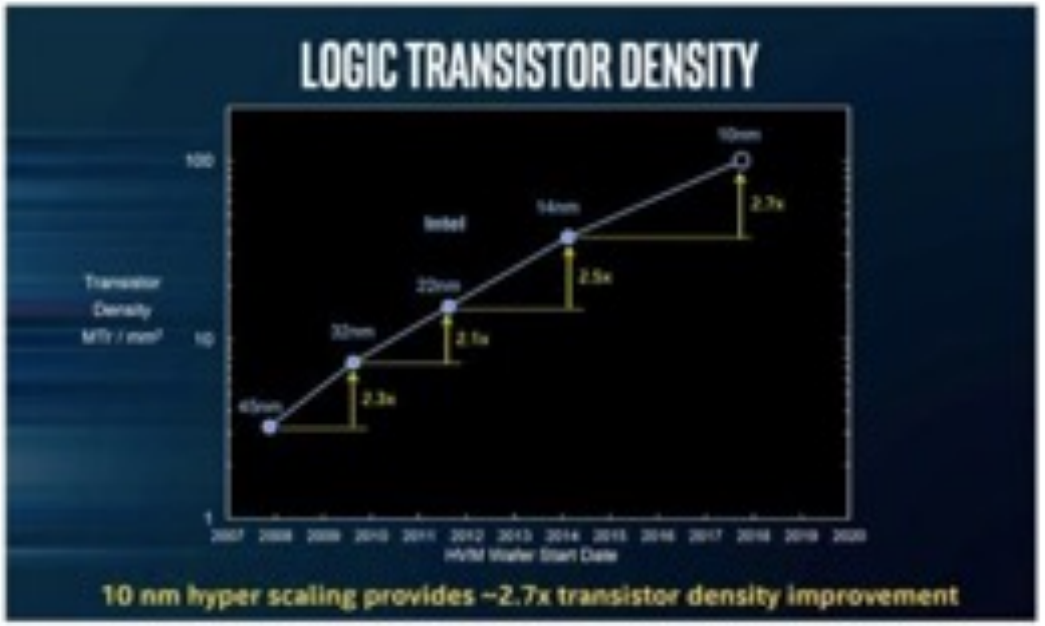
Figure 3. illustrates Intel's hyper scaling.

Hyper Scaling

IC KNOWLEDGE LLC

- Intel started hyper scaling at the same time that scaling was getting harder.
- 2.5x density improvement for 14nm was 1 year late.
- 2.7x density improvement for 10nm was 2+ years late and still has yield issues.



Moore's Law Leadership, Mark Bohr, Intel Manufacturing Day 2017

Intel MOSFET

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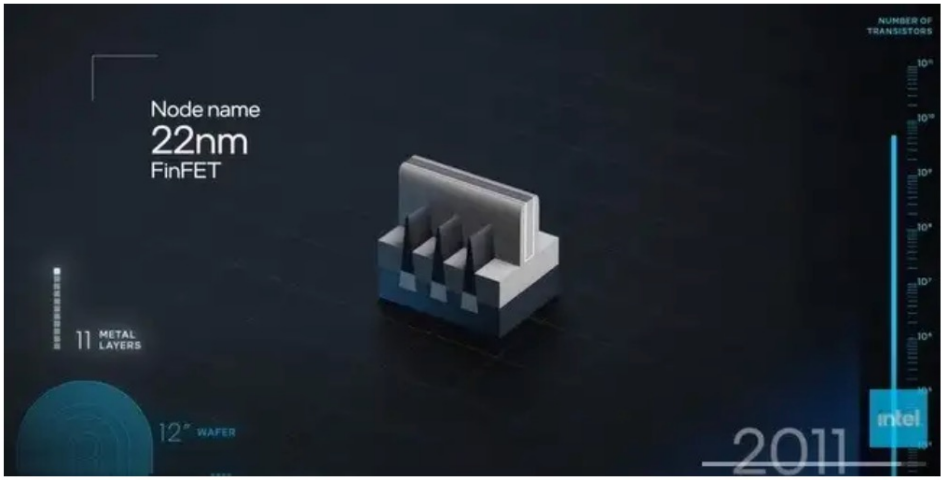
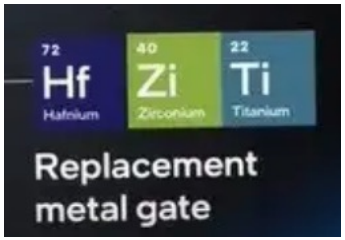
Intel video

https://www.youtube.com/watch?v=Z7M8etXUEUU&t=47s

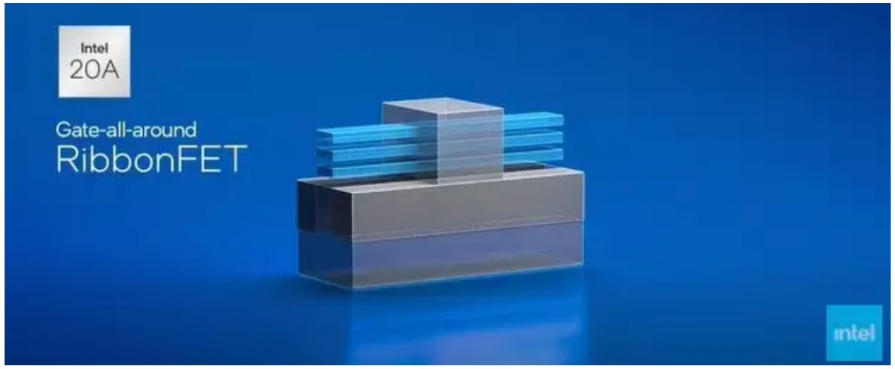
FinFET: 2011



Intel amazed the industry with its aggressive adoption of a new transistor topology at the 22nm process node – the FinFET (also known as the "tri-gate FET").

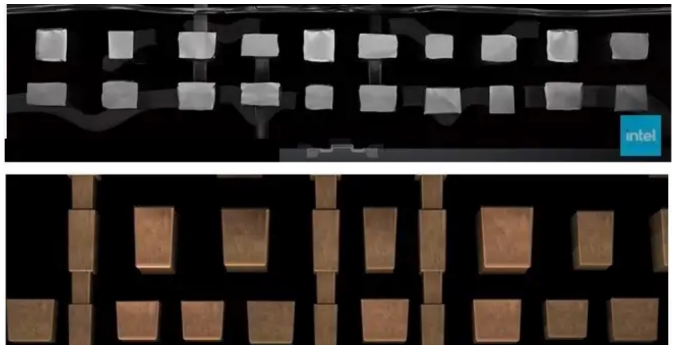


Gate-All Around (GAA) Ribbon FET: Intel 20A in 2024



To further improve the electrostatic gate control over the channel, another major evolution in the transistor topology is emerging to replace the FinFET. A gate-all-around configuration involves a vertical stack of electrically isolated silicon channels. The gate dielectric and gate input utilize an atomic layer deposition (ALD) process flow to surround all channel surfaces in the stack.

Intel will be releasing their GAA *Ribbon FET* 20A process in 1H 2024.



Intel's Newest Fabs

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$**20B** in Ohio

Online end of **2025**

SATURDAY, JANUARY 22, 2022 A9

Intel to build chip factories in Ohio

Company will invest $20 billion as a global shortage highlights the risks of reliance on manufacturers in Asia.

Samsung in Texas

Chipmakers are diversifying their manufacturing sites in response to the shortages. Samsung said in November that it planned to build a $17-billion factory outside Austin, Texas.

Micron Technology, based in Boise, Idaho, said it would invest $150 billion globally over the next decade in developing its line of memory chips, with a potential U.S. manufacturing expansion if tax credits can help make up for the higher costs of American manufacturing.

Micron globally

10,000 jobs in Ohio

Two chip factories on the 1,000-acre site in Licking County, just east of Columbus, are expected to create 3,000 company jobs and 7,000 construction jobs, and to support tens of thousands of additional jobs for suppliers and partners, the com-

CHIPS for America Act

Lawmakers have been urging House and Senate leaders to fully fund a law meant to address the semiconductor shortage. They want Congress to fully fund the $52-billion CHIPS for America Act, allowing for stateside investment in semiconductor factories.

More on Intel's New Fabs

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Semi Wiki

$52B Chips for America is barely a rounding error

When you assume that the Chips for America act is a one time, one shot disbursement spread over a number of years and a number of companies it becomes clear that its not much against TSMC's spend.

It also does not compare to what China as a whole is spending on semiconductor technology.

Basically the US is being outclassed and outgunned by both China and Taiwan (probably part of China in the not too distant future).

Even if Intel got the whole $52B it still couldn't keep up as the spend would be over several years. Never mind that only $10B of the $52B is for fab projects with a $3B limit per project. Essentially the $52B will be spread so thin as to be ineffective versus the focused sharp spend of TSMC.

More on Intel's New Fabs

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Semi Wiki

Can the US fabs being built make a difference?

Intel announced two fabs in Arizona at $10B each along with TSMC announcing a 5NM fab in Arizona which by the time its operational will be a drop in the bucket trailing edge fab perhaps meant to mollify the US.

Samsung has announced a $17B in Texas in addition to existing facilities there. It looks like Intel has chosen Ohio for its "megafab" project and Micron is eyeing North Carolina.

While details are scarce, it sounds like the Intel Ohio and Samsung Texas fabs are the most impactful on the US. Samsung would be somewhat less impactful as we assume that bleeding edge technology R&D will continue to be done in Korea making the Texas fab a "fast follower" much as the existing Samsung fab in Texas is today. That leaves Intel Ohio as the only trail blazing R&D facility in the US.

It also remains to be seen if the brain trust in Portland can either be moved or shared with Ohio or if Portland remains the R&D center with Ohio for production.

Intel's New Fab Equip.

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EUV from ASML

Intel Places Order for ASML's Extreme Ultraviolet Technology

04:49 AM EST, 01/19/2022 (MT Newswires) -- Intel (INTC) and ASML Holding (ASML) said Wednesday that the US chip maker has placed its first purchase order for ASML's TWINSCAN EXE:5200 extreme ultraviolet high-volume production system. The purchase ... (MT Newswires 04:49 AM ET 01/19/2022)

CHIPS Act in Ohio

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Sept 2022

CHIPS Act in Ohio

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Intel New Euro Fab

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INTEL CORP (INTC) (*47.70* *-0.01*) *I*

Market Chatter: Intel Reportedly Chooses Germany's Magdeburg as Location for New European Chip Factory

08:22 AM EST, 02/28/2022 (MT Newswires) -- Intel (INTC) has picked the city of Magdeburg in Germany as the location for a new European chip factory, Reuters reported on Saturday, citing an unnamed person familiar with the matter. The US ... (MT Newswires 08:22 AM ET 02/28/2022)

Read more

Intel – Italy Deal

Jeff Drobman
8-10-22

Italy, Intel close to $5 billion deal for chip assembly and packaging factory

I think Intel believes it can manage the cost in Italy that is comparable or cheaper to what other Intel assembly and packaging sites in Vietnam, Malaysia, Philippines, China, and Costa Rica. It's hard to believe it unless it's almost fully automated and use few workers.

Exclusive: Italy, Intel close to $5 billion deal for chip factory

Italy is close to clinching a deal initially worth $5 billion with Intel to build an advanced semiconductor packaging and assembly plant in the country, two sources briefed on discussions told Reuters on Thursday.

www.reuters.com

Intel News: Italy Fab

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Jeff Drobman

Market Chatter: Intel, Italy Reportedly Pick Veneto Region as Location for Proposed Chip Factory

4:39 AM ET, 09/26/2022 - MT Newswires

04:39 AM EDT, 09/26/2022 (MT Newswires) -- Intel (INTC) and the Italian government have selected the town of Vigasio in the country's Veneto region as the location for a proposed chip factory, Reuters reported Sunday, citing anonymous sources familiar with the matter.

The factory, with an initial investment of some 4.5 billion euros ($4.36 billion), is part of the company's planned investment of 80 billion euros ($77.34 billion) to grow capacity in Europe, according to the report.

The new facility is expected to create 1,500 jobs and is slated to start operations between 2025 and 2027, Reuters reported.

Intel to Fab MediaTek

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Intel, MediaTek Enter Into Chip-Manufacturing Agreement

5:50 AM ET, 07/25/2022 - MT Newswires05:50 AM EDT, 07/25/2022 (MT Newswires) -- Intel (INTC) said Monday it entered into an agreement with MediaTek to manufacture chips using Intel Foundry Services.

The chipmaker said MediaTek aims to use Intel's process technologies to produce multiple chips for *smart edge* devices.

Financial details of the agreement were not disclosed.

Intel 14th Gen *Meteor Lake*

DR JEFF SOFTWARE
INDIE APP DEVELOPER
Jeff Drobman

SemiWiki.com
The Open Forum for Semiconductor Professionals

Rumor Mill 8-8-22

> ➢ Intel **14th Gen** *Meteor Lake* Rumored To Drop TSMC 3nm Node For tGPU, Might Be Used in **15th Gen** *Arrow Lake* CPUs

Meteor Lake is supposed to be **3 chipsets** - so they'll still need capacity for the I/O die and the iGPU from somewhere. N3 was only to be used for the iGPU where I/O was an older node. This seems like something specific to the iGPU (Intel design not ready) and/or N3 (capacity, timing, etc).

It is neither. ***Meteor Lake*** is yielding fine: Intel 4 CPU, TSMC N3 GPU, TSMC N5 base die and SoC.

Intel New Fabs

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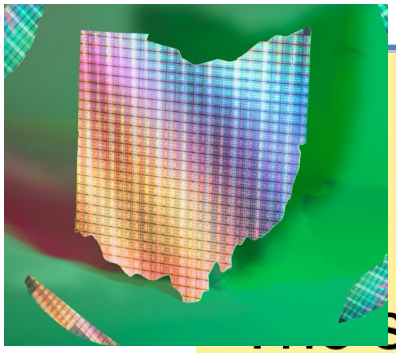

Intel Inside Ohio

struggling chipmaker is attempting a comeback with massive spending on new factories and lots of help from the Biden administration.

In Ohio, Intel promised to hire 7,000 construction workers and 3,000 employees and spend at least $20 billion

Intel New Fabs

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Jeff Drobman

$28B

This is Ohio One, a future "mega fab"—or factory—being built by Intel Corp. The company has committed $28 billion to build a fab that, if all goes well, will be able to credibly compete for contracts to manufacture state-of-the-art chips used in smartphones and in the training of next-generation artificial intelligence algorithms. Ohio One, says Chief Executive Officer Patrick Gelsinger, could eventually be the biggest chip factory on Earth. Not to be

Intel One in Ohio

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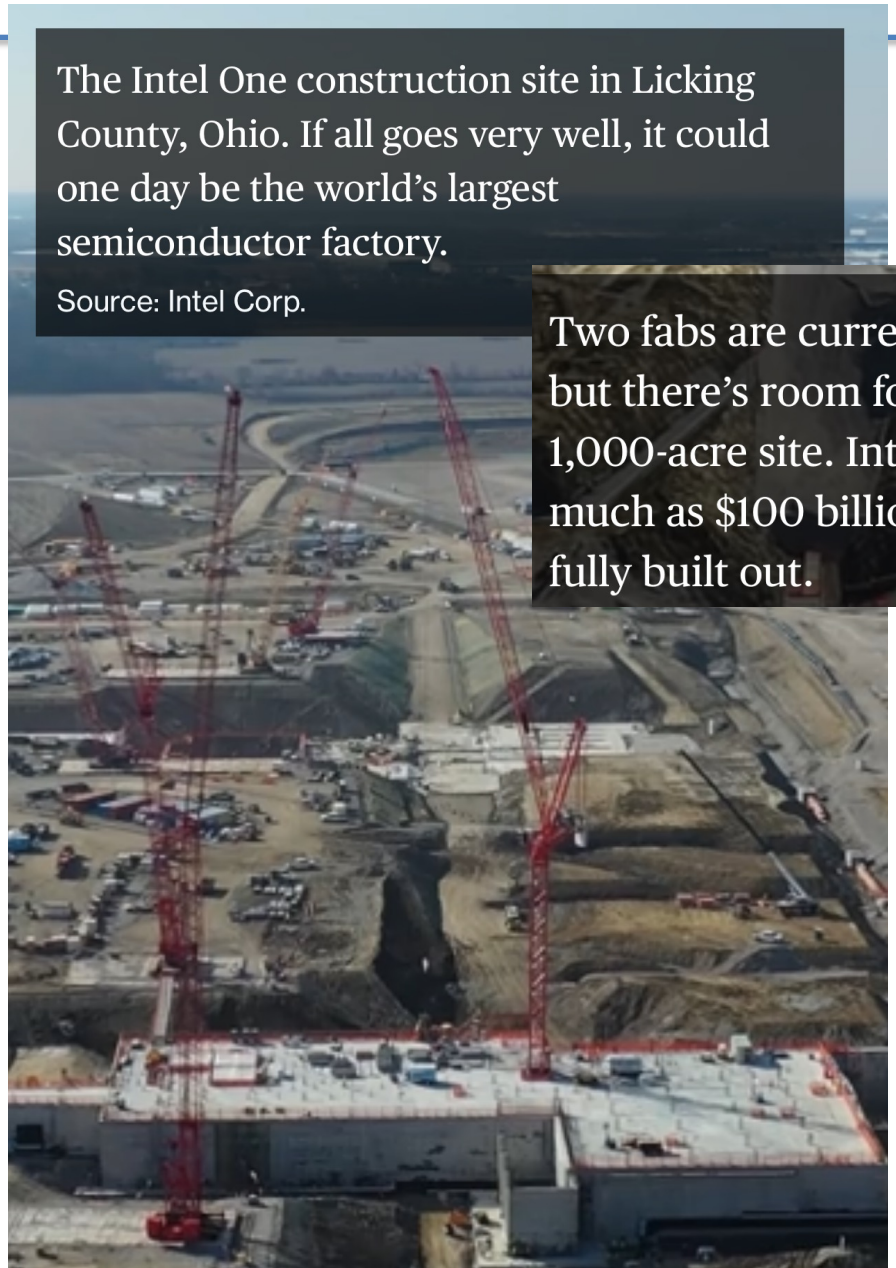
$100B



The Intel One construction site in Licking County, Ohio. If all goes very well, it could one day be the world's largest semiconductor factory.

Source: Intel Corp.

Two fabs are currently under construction, but there's room for eight in total on the 1,000-acre site. Intel has said it will put as much as $100 billion into the project if it's fully built out.

Intel New Fabs

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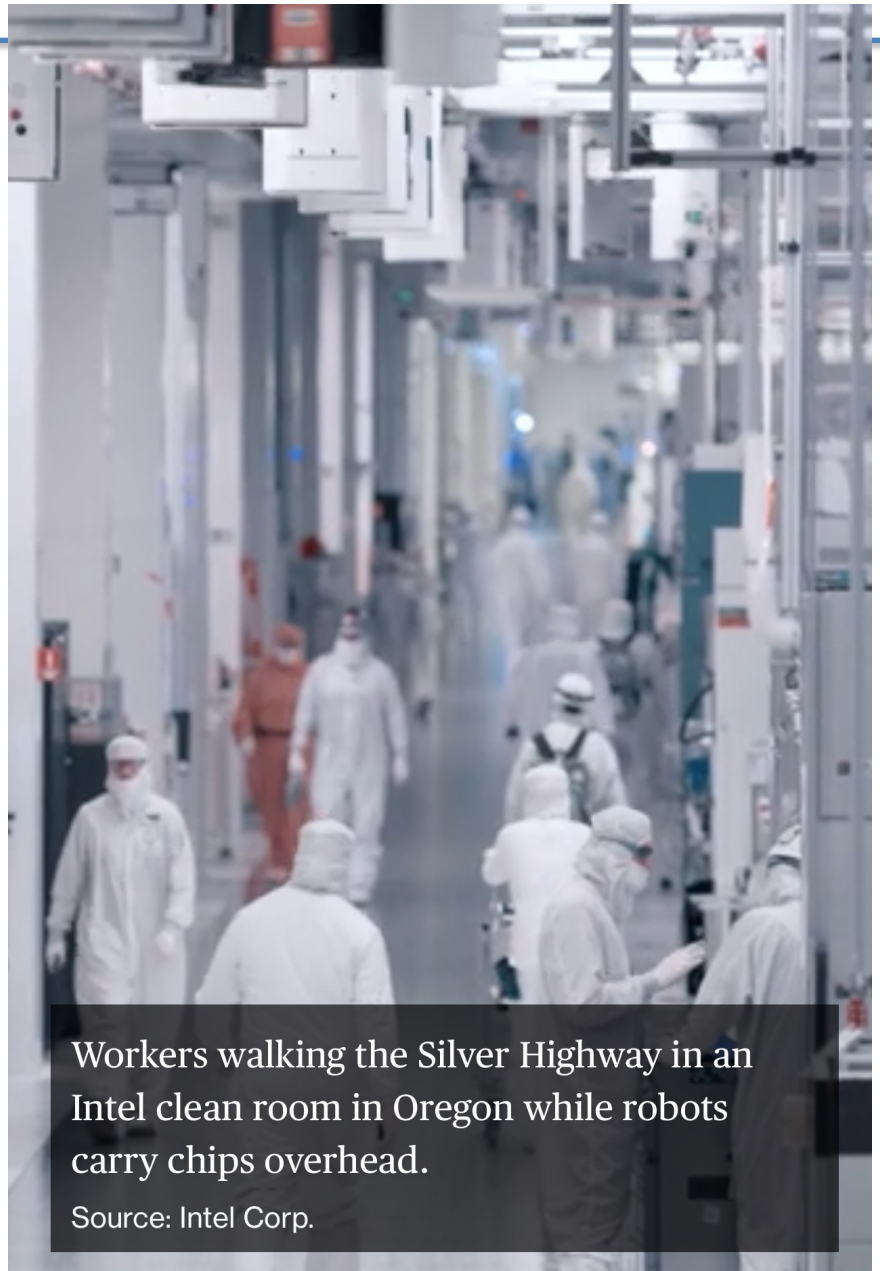

Workers walking the Silver Highway in an Intel clean room in Oregon while robots carry chips overhead.

Source: Intel Corp.

Intel New Fabs

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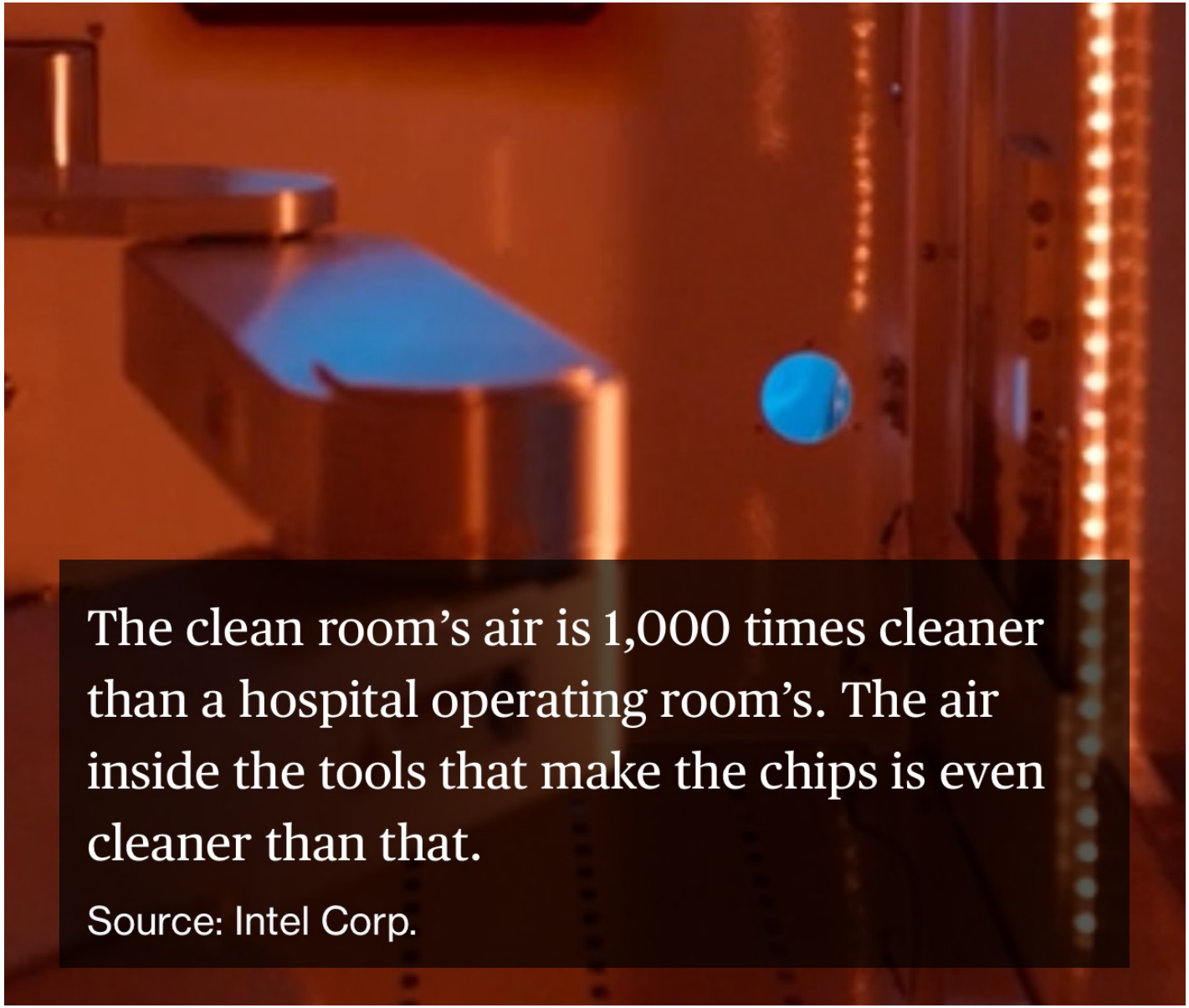

Intel New Fabs

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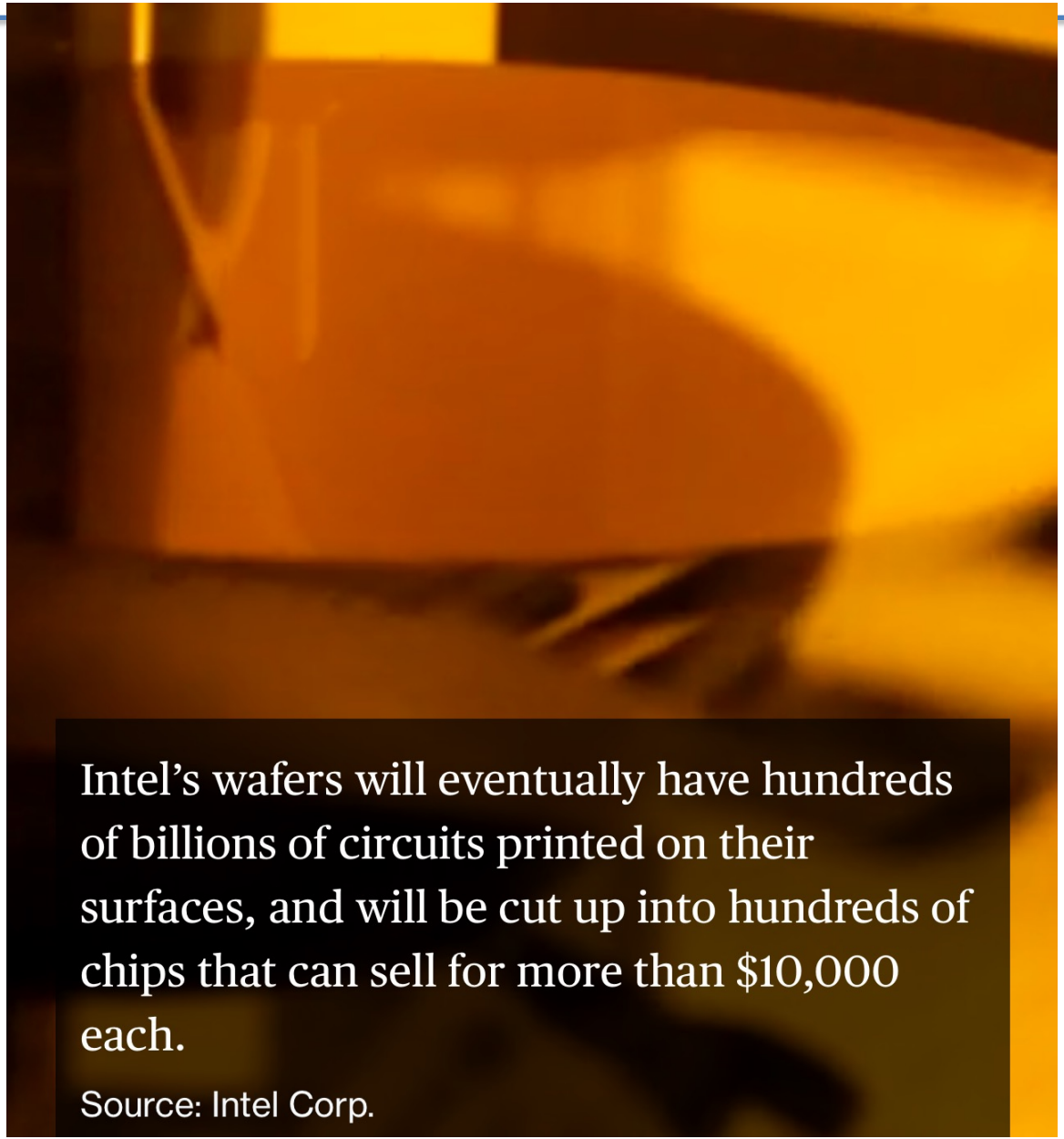

Intel New Fabs

$380M

The largest tool was also the newest: ASML's latest EUV machine, which is the size of a tennis court and costs $380 million. This "high numerical aperture"—or high NA—EUV machine was positioned in a section of the fab some engineers had taken to calling "the billion-dollar bay," because of the wildly expensive tools involved. It arrived in Oregon from the Netherlands last year in 43 specially constructed shipping containers. Assembly took months and was only just finished.

Intel New Fabs

$380M

That extreme ultraviolet light bounces off a series of mirrors before it hits the wafer. The entire operation–the lasers, the tin hotter than the surface of the sun, the mirrors, the wafer–is a single step in a process that takes three to six months to yield a finished product. During that time, each wafer will go through thousands of steps of layering, etching, measuring and washing until there's an intricate pattern of hundreds of billions of transistors. Some of these layers will be as thin as a single atom.

Intel New Fabs

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Even today, even with all of Gelsinger's swagger, roughly 30% of the top-of-the-line chips Intel sells are made by TSMC. Those chips cost Intel extra money to make and they also reduce volumes, making its aging factories even less profitable than they would be. The hope is that by investing in new fabs and by touting state-of-the-art machines, Intel can reverse the death spiral–"bringing more of those wafers home," as Gelsinger put it in a recent call with analysts. Of course, TSMC and Samsung are also building new fabs and will get their own high NA EUV machines. In fact, just

Chips/Fabs

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Chip Design/Fab

Micron

- D/SRAM
- Flash

More Chips $$

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relief rally, though. Intel was up more than 2%, and Micron Technology was 1.1% up, while Taiwan Semiconductor Manufacturing's (TSMC) American depositary receipts climbed 0.2%. Meanwhile, Advanced Micro Devices stock was flat.

There was more good news for the chip sector after Samsung Electronics was granted up to $6.4 billion by the U.S. government to build facilities in Texas. It comes after TSMC was granted $6.6 billion last week, while Intel has also received $8.5 billion under the 2022 Chips Act.

Micron Gets $6.1B

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Biden administration agrees to provide $6.1bn for Micron Technology to produce advanced memory chips in New York and Idaho

by Josh Boak and The Associated Press / Apr 18, 2024 / 5:36 AM

Micron joins **Intel**, **TSMC** and **Samsung**
To receive **$6B+** in CHIPS Act funds

The Biden administration has reached an agreement to provide $6.1 billion in government support for Micron Technology to produce advanced memory computer chips in New York and Idaho.

Senate Majority Leader Chuck Schumer, D-N.Y., personally courted Micron to build what would ultimately be a set of four chip factories near Syracuse in the town of Clay.

Micron Taiwan Fab

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4-11-24

Micron says Taiwan earthquake will have mid-single digit percentage impact on quarterly DRAM supply

By Ciara Linnane
Updated April 11, 2024, 12:30 pm EDT

Memory-chip maker says fab activity is recovering well after 7.4-magnitude earthquake

Micron Fab

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DRAM's Moore's Law Is Still Going Strong

Micron Technology pushes ahead with 35 percent density boost and does it without advanced lithography tool

SAMUEL K. MOORE
1 NOVEMBER 2022

Micron says it is shipping samples of **LPDDR5X** chips, memory made for power-constrained systems such as smartphones.
(LPDDR5X unpacked means: a revved-up twist on the low-power version of the 5th generation of the double data rate memory communications standard, capable of transferring 8.5 gigabits per second.)

It's the first chip made using Micron's new manufacturing process, called 1-beta, which the company says maintains the lead it took a year ago over rivals including Samsung and SK Hynix.

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Micron New US Fabs

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Micron Technology Plans US Manufacturing Investments, Welcomes Passage of Chips and Science Act

10:30 AM ET, 07/29/2022 - MT Newswires10:30 AM EDT, 07/29/2022 (MT Newswires) -- Micron Technology (MU) said Friday it plans to invest further in its US memory manufacturing capabilities as the semiconductor company welcomed the passage of the Chips and Science Act in Congress.

"The competitive incentives passed yesterday will allow Micron, *the only US-based manufacturer of memory*, to grow domestic production of memory significantly in the years ahead," the company said.

The legislation, which is expected to be signed into law in the coming days, will provide **$52 billion** in subsidies for domestic chip manufacturers and over **$100 billion** in technology and sciences investments, according to the Financial Times.

Micron in NY

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Chipmaker Micron to build $20 billion N.Y. factory amid semiconductor boom

Chipmaker Micron to build $20 billion N.Y. factory amid semiconductor boom

The company eventually could spend up to $100 billion over 20 years

BY JEANNE WHALEN
OCTOBER 4 AT 11:16 AM

Tech giant Micron said it will invest $20 billion in a new chip factory in Upstate New York, and up to $100 billion over twenty years if it decides to expand — another sign of a domestic semiconductor manufacturing boom.

Fabs

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Foundries

Global Foundries

Founded 2009

Global Foundries

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July 2021

GlobalFoundries

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4Q2021

Major 2021 Accomplishments and Key Fourth Quarter Business Highlights:

•In 2021, GF entered into 30 significant long-term customer agreements that provide assurance to our customers and provide revenue visibility to GF.

•In 2021, GF broke ground on a new fab on its **Singapore** campus, expanded capacity in Fab 1 (**Dresden**) by over 25%, and announced expansion plans for its most advanced manufacturing facility in **upstate New York**.

•GF set a "Journey to Zero Carbon" goal to reduce greenhouse gas emissions by 25% while expanding global manufacturing capacity.

•On October 28, 2021, GF began trading on **Nasdaq** Stock Market under the ticker "GFS."

•In the fourth quarter, GF announced an extension of its wafer supply agreement with **AMD**, increasing the number of chips GF will supply, as well as extending the terms of the agreement to secure supply through 2025.

•In the fourth quarter, **BMW** signed a direct supply assurance agreement with high-tech microchip developer INOVA Semiconductors and GF to secure long-term semiconductor supplies.

•In the fourth quarter, GF and **Ford** announced a non-binding strategic collaboration to advance semiconductor manufacturing and technology development within the US, aiming to boost chip supplies for Ford and the US auto industry.

AMD Orders Wafers

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News

ADVANCED MICRO DEVICES (AMD) (*154.36 +8.22*) *I*

Advanced Micro Devices to Buy $2.1 Billion of GlobalFoundries Wafers Under Expanded Deal

10:19 AM EST, 12/27/2021 (MT Newswires) -- GlobalFoundries (GFS) said Dec. 23 that semiconductor company Advanced Micro Devices (AMD) will now buy nearly $2.1 billion worth of its wafers starting 2022 through 2025 under an expanded deal. A wafer is ... (MT Newswires 10:19 AM ET 12/27/2021)

GlobalFoundries

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12LP 12nm FinFET Technology

Ideal for high-performance, power-efficient SoCs in demanding, high-volume applications

GLOBALFOUNDRIES 12LP platform with 12nm 3D FinFET transistor technology provides best-in-class performance and power with significant cost advantages from 12nm area scaling. 12LP technology can provide up to 75% higher device performance and 60% lower total power compared to 28nm technologies. 12LP was **announced** in 2017 based on GF's proven existing 14nm offering, and the offering has transitioned from 14LPP to 12LP in 2018.

Global Foundries

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GlobalFoundries

From Wikipedia, the free encyclopedia

Coordinates: 37.415293°N 121.974448°W

> This article **contains content that is written like an advertisement**. Please help improve it by removing promotional content and inappropriate external links, and by adding encyclopedic content written from a neutral point of view. *(May 2021) (Learn how and when to remove this template message)*

GlobalFoundries Inc. (**GF**) is a United States-based semiconductor manufacturer headquartered in Malta, New York.[3] GlobalFoundries was created by the divestiture of the manufacturing arm of Advanced Micro Devices (AMD) and is owned by Mubadala Investment Company.

GlobalFoundries is the world's fourth largest semiconductor manufacturer[4][5] and produces chips for more than 7% of the $86 billion semiconductor manufacturing services industry. The company manufactures chips designed for high-growth markets such as mobility, automotive, computing and wired connectivity, consumer internet of things (IoT) and industrial.

As of 2021, GlobalFoundries is the only semiconductor manufacturer with simultaneous operations in Singapore, the European Union, and the United States. The company has one 200mm and one 300mm fabrication plants in Singapore; one 300 mm plant in Dresden, Germany; one 200 mm plant in Burlington, Vermont (where it is the largest private employer)[6] and two 300 mm plants in New York: one in East Fishkill and one in Malta.[7]

GlobalFoundries is a "Trusted Foundry" for the U.S. federal government and has similar designations in Singapore and Dresden including certified international Common Criteria standard (ISO 15408, CC Version 3.1).[8][9]

The company has more than 250 customers around the world and has 15,000 employees representing 92 nationalities in 14 countries. GlobalFoundries holds more than 10,000 patents and applications.

CEO Thomas Caulfield has said GlobalFoundries plans to become a publicly traded company in 2022.[10]

Contents [hide]

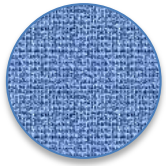
GlobalFoundries Inc.

GLOBALFOUNDRIES

Type	Private
Industry	Semiconductor manufacturer
Founded	March 2, 2009; 12 years ago
Headquarters	Malta, New York, U.S.
Key people	Dr. Thomas Caulfield (CEO)[1]
Products	Semiconductor
Number of employees	15,000
Parent	Mubadala Investment Company
Website	globalfoundries.com

Footnotes / references
[2]

200mm & 300mm wafers



Global Foundries

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Jeff Drobman

Overview [edit]

On October 7, 2008, AMD announced it planned to go fabless and spin off their semiconductor manufacturing business into a new company temporarily called The Foundry Company. Mubadala announced their subsidiary Advanced Technology Investment Company (ATIC) agreed to pay $700 million to increase their stake in AMD's semiconductor manufacturing business to 55.6% (up from 8.1%). Mubadala will invest $314 million for 58 million new shares, increasing their stake in AMD to 19.3%. $1.2 billion of AMD's debt will be transferred to The Foundry Company.[11] On 8 December 2008, amendments were announced. AMD will own approximately 34.2% and ATIC will own approximately 65.8% of The Foundry Company.[12]

On March 4, 2009, GlobalFoundries was officially announced.[13] On September 7, 2009, ATIC announced it would acquire Chartered Semiconductor for S$2.5 billion (US$1.8 billion) and integrate Chartered Semiconductor into GlobalFoundries.[14] On January 13, 2010, GlobalFoundries announced it had finalized the integration of Chartered Semiconductor.[15]

On March 4, 2012, AMD announced they divested their final 14% stake in the company, which concluded AMD's multi-year plan to divest its manufacturing arm.[16]

On October 20, 2014, IBM announced the sale of its microelectronics business to GlobalFoundries.[17]

As of 2015, the firm owned ten fabrication plants. Fab 1 is in Dresden, Germany. Fabs 2 through 7 are in Singapore. Fabs 8 through 10 are in the northeast United States. These sites are supported by a global network of R&D, design enablement, and customer support in Singapore, China, Taiwan, Japan, India, the United States, Germany, and the United Kingdom.[18] In February 2017, the company announced a new 300 Fab [Fab 11] in China for growing semiconductor market in China.[19]

In 2016, GlobalFoundries licensed the 14 nm 14LPP FinFET process from Samsung Electronics. In 2018, GlobalFoundries developed the 12 nm 12LP node based on Samsung's 14 nm 14LPP process.[20]

On August 27, 2018, GlobalFoundries announced it had cancelled their 7LP process due to a strategy shift to focus on specialized processes instead of leading edge performance.[21]

On January 29, 2019, AMD announced an amended wafer supply agreement with GlobalFoundries. AMD now has full flexibility for wafer purchases from any foundry at 7 nm or beyond. AMD and GlobalFoundries agreed to commitments and pricing at 12 nm for 2019 through 2021.[22]

On May 20, 2019, Marvell announced it would acquire Avera Semi from GlobalFoundries for $650 million and potentially an additional $90 million. Avera Semi was GlobalFoundries' ASIC Solutions division, which had been a part of IBM's semiconductor manufacturing business.[23] On February 1, 2019, GlobalFoundries announced the $236 million sale of its Fab 3E in Tampines, Singapore, to Vanguard International Semiconductor (VIS) as part of their plan to exit the MEMS business by December 31, 2019.[24] on April 22, 2019, GlobalFoundries announced the $430 million sale of their Fab 10 in East Fishkill, New York, to ON Semiconductor. GlobalFoundries has received $100 million and will receive $330 million at the end of 2022 when ON Semiconductor will gain full operational control. The 300mm fab is capable of 65 nm to 40 nm and was a part of IBM.[25] On August 15, 2019, GlobalFoundries announced a multi-year supply agreement with Toppan Photomasks. The agreement included Toppan acquiring GlobalFoundries' Burlington photomask facility.[26]

Process Technology

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Fabs

- Spanning three continents across 14 locations

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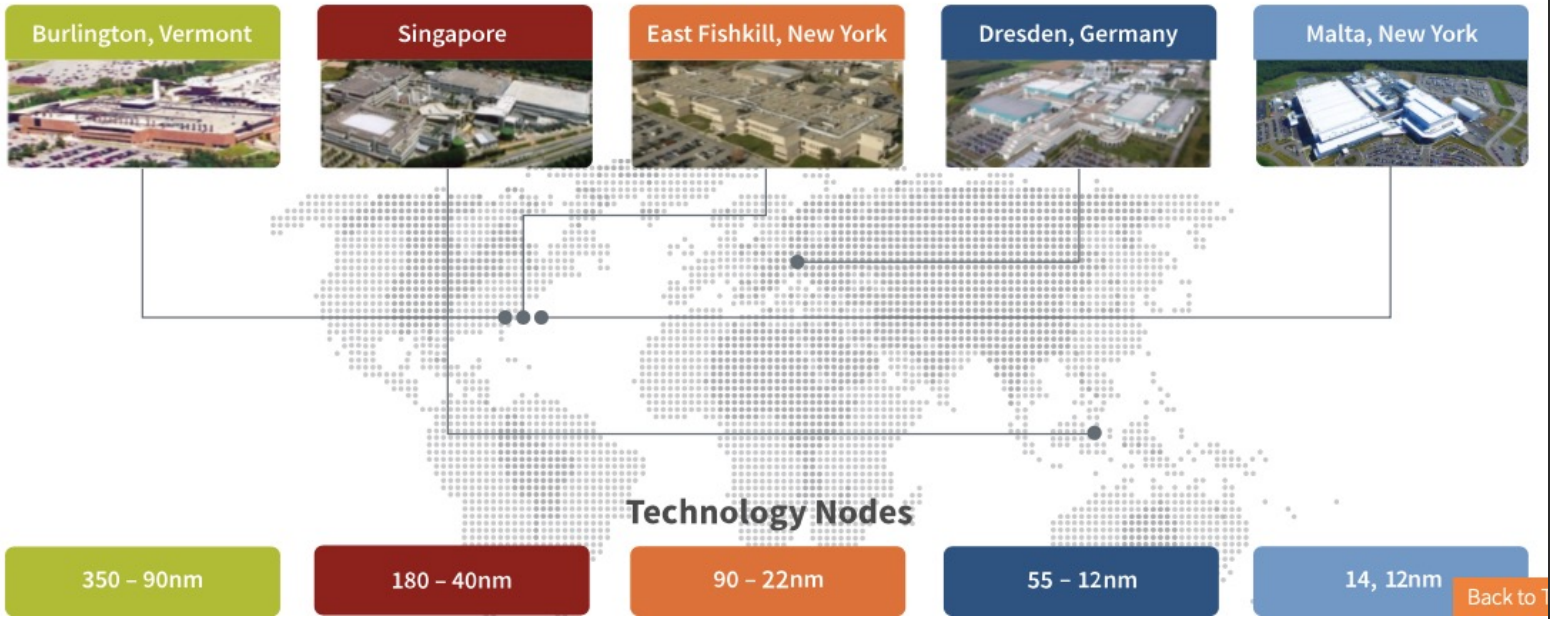
Our Manufacturing Capabilities



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Technology Solutions

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ASICs

Silicon Photonics

Global Foundries Fabs

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Fabrication foundry [edit]

Name	Wafer	Location		Process
Fab 1	300 mm	Dresden, Germany	51.125°N 13.716°E	55, 45, 40, 32, 28, 22 nm, 12 nm
Fab 2	200 mm	Woodlands, Singapore	1.436°N 103.766°E	600–350 nm
Fab 3/5	200 mm	Woodlands, Singapore	1.436°N 103.766°E	350–180 nm
Fab 3E	200 mm	Tampines, Singapore (2019: sold to VIS)	1.371°N 103.929°E	180 nm
Fab 6	200 mm	Woodlands, Singapore (converted to 300 mm and merged into Fab 7)	1.436°N 103.766°E	180–110 nm
Fab 7	300 mm	Woodlands, Singapore	1.436°N 103.766°E	130–40 nm
Fab 8	300 mm	Luther Forest Technology Campus, Saratoga County, New York, United States	42.970°N 73.756°W	28, 20, 14 nm
Fab 9	200 mm	Essex Junction, Vermont, United States	44.48°N 73.10°W[44]	350–90 nm
Fab 10	300 mm	East Fishkill, New York, United States (2019: started transfer to ON Semiconductor)	41.540°N 73.822°W	90–22 nm, 14 nm

Global Foundries Financials

Written by

KHAVEEN Investments

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Revenue Forecast ($ mln)	2018	2019	2020	2021	2022F	2023F	2024F
Wafer Shipments 300mm equivalents ('000s) ('a')	1,863	1,758	2,030	2,374	2,586	3,036	3,358
Growth %		-5.6%	15.5%	16.9%	8.9%	17.4%	11%
Wafer ASP (Revenue per wafer) ('b')	3,326	3,306	2,389	2,774	3,051	3,034	3,017
Growth %		-0.6%	-27.7%	16.1%	10.0%	-0.6%	-0.6%
Revenue ($ mln) ('c')	**6,196**	**5,813**	**4,851**	**6,585**	**7,890**	**9,212**	**10,133**
Growth %		**-6.2%**	**-16.6%**	**35.8%**	**19.8%**	**16.7%**	**10.0%**

Foundries

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TSMC

Founded 1987

TSMC 3Q22/1Q24

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3Q22

- Revenue = $20.23B
- EPS = $1.79
- Wafer revenue shares
  - 5nm = 28%
  - 7nm = 26%

1Q24

- Revenue = $18.5B

Samsung **7nm** did pretty good but Samsung **5nm** and **4nm** had serious PDK/yield problems and Samsung **3nm** is not really competitive against TSMC N3 and it requires new design considerations for **GAA**.

More US $$ for TSMC

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Taiwan Earthquake

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TSMC shutdown

- Intel
- AMD
- Nvidia
- Qualcomm
- Apple

Alibaba, Intel, AMD, Taiwan Semi, Super Micro, and Other Tech Stocks in Focus Today

Intel Foundry Biz lost **$7B**

Intel said its foundry business had an operating loss of $7 billion in 2023. **Credit:** DREAMSTIME

TSMC in Taiwan

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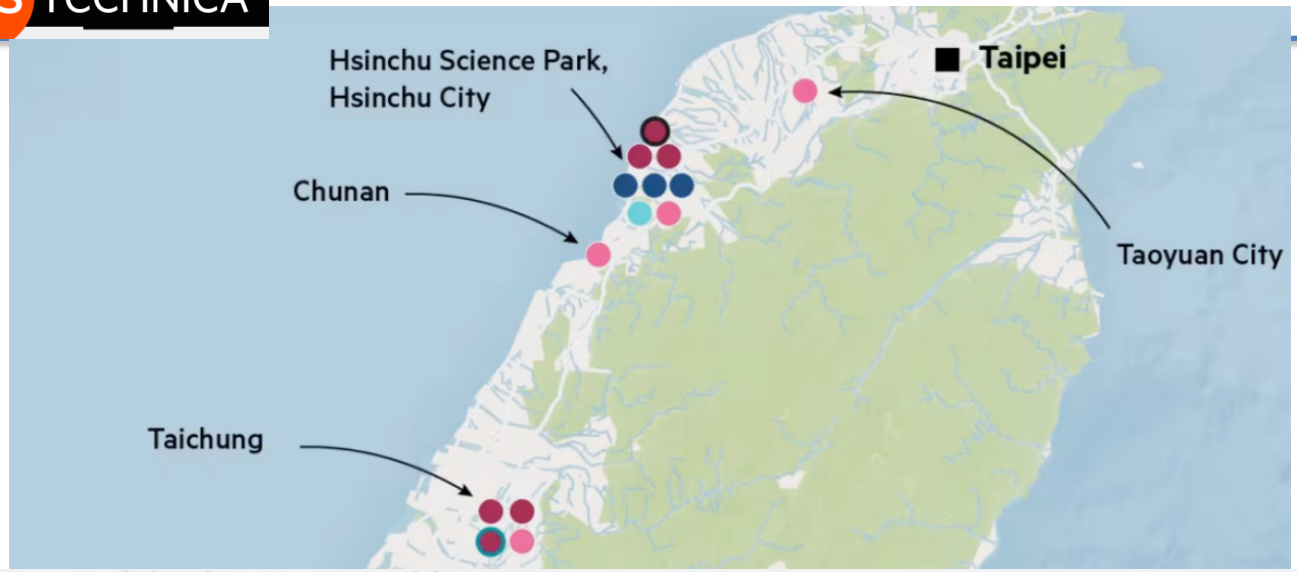

Group's fabs by type and location

12-inch 8-inch 6-inch Backend Under construction Planned

TSMC Global

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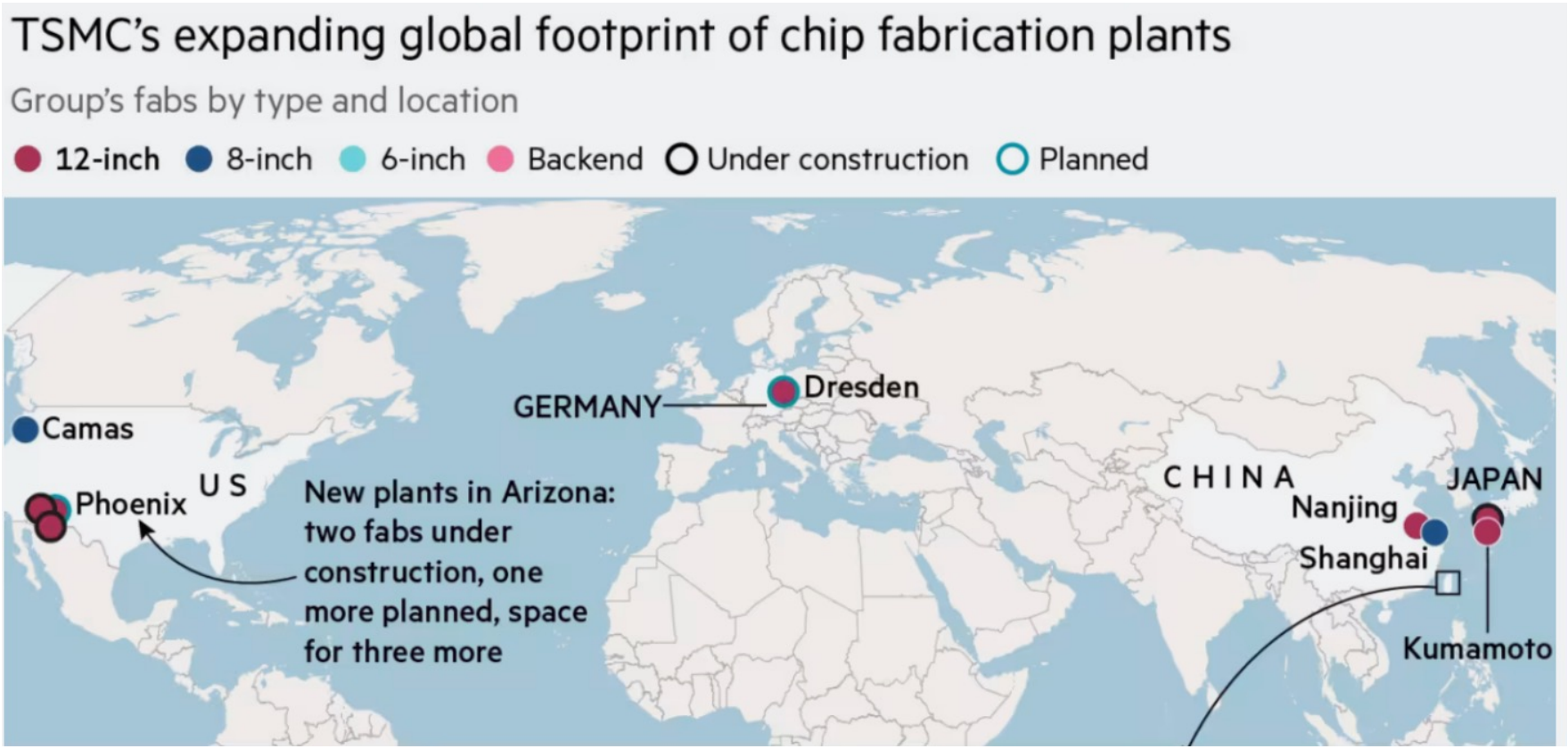

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For TSMC to move more quickly would disrupt one of its key advantages as a chipmaker—its ability to outperform rivals in achieving high yields for new process technology, keeping defective chips to a minimum. Its research and development engineers in Taiwan, managing the start of the production stage, are considered vital.

"It's not that we don't want to bring new process [technology] to the US even earlier," said a person familiar with TSMC's considerations. "But we need the vicinity to our global research and development center whenever we ramp up a new node. That means we have to ramp in Taiwan first."

Mobile chips made for Apple, TSMC's largest client, may bear the heaviest impact from the resulting gap between capacity in US and Taiwan. TSMC usually makes smartphone chips first with its latest processing technology, serving high-performance computing products a year or two later.

"Apple has always been the first adopter of a node. So if the Arizona fabs are a bit behind, then maybe they could only meet Apple's needs for older models," Xie said.

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TSMC—which makes chips under contract at hugely complex and expensive fabrication plants, or fabs—plans to start manufacturing 2-nanometer chips in the US in 2028. This is an upgrade from the company's previous plans. At that time 2 nm technology is expected to be the latest in mass production worldwide, whereas previously the company had intended each new US fab to start operating with process technology one generation behind Taiwan.

TSMC has also committed to offer a third plant using 2 nm or even newer technology by 2030.

Washington is paying a hefty price for the upgrade, with US$6.6 billion in grants and up to $5 billion in loans for TSMC. The money comes from the 2022 Chips and Science Act, which aims to onshore advanced chipmaking for the US. Commerce secretary Gina Raimondo has said the US will be on track to make about 20 percent of the world's most advanced chips by the end of the decade.

But while Washington's money offers some incentive, TSMC's most important motive for stepping up its commitment to the US was to bring its own US strategy in line with the needs of Nvidia and other vendors of the AI chips that have become the most potent driver of global semiconductor demand.

TSMC

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TSMC to launch chipmaking plant in Japan, but US plant to face delays

Taiwan's TSMC will open its latest chipmaking foundry on Japan's Kyushu island on February 24, but a plant in the United States will face further delays, the company said Thursday.

Taiwan Semiconductor Manufacturing Company -- which counts Apple and Nvidia as clients -- controls more than half the world's output of silicon wafers, used in everything from smartphones to cars and missiles.

TSMC New Fab

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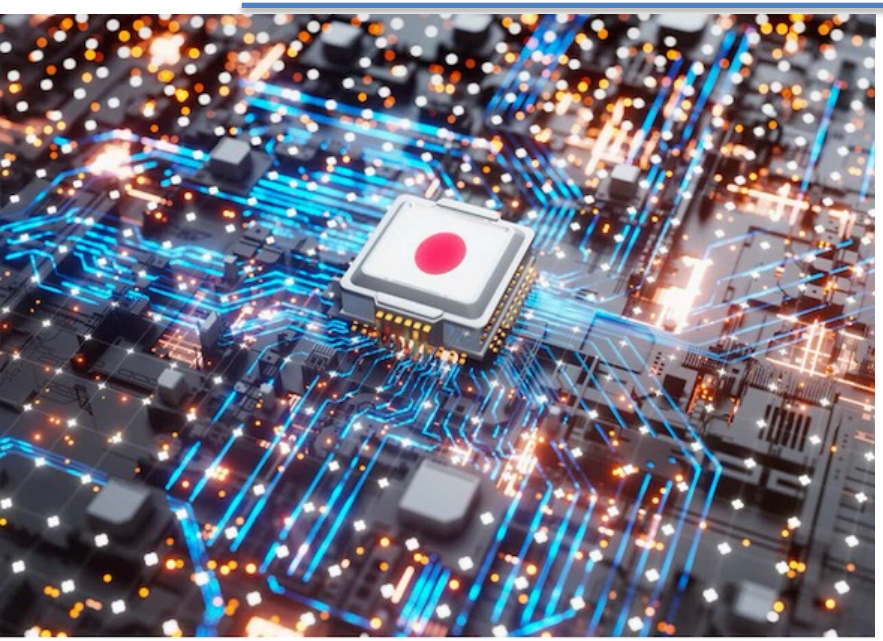

Taiwan Semiconductor, Sony others team up to build 2nd chip facility in Japan

Feb 06, 2024 8:34 AM ET | **Taiwan Semiconductor Manufacturing Company Limited (TSM)** | Ravikash, SA News Editor

Taiwan Semiconductor Manufacturing (NYSE:TSM) will build a second chip fabrication facility in Japan with help from Sony (SONY), Denso, Toyota (TM) and the Japanese government.

Overall investment in Japan Advanced Semiconductor Manufacturing, or JASM — TSM's majority-owned manufacturing subsidiary, will exceed $20B.

Chip Shortage

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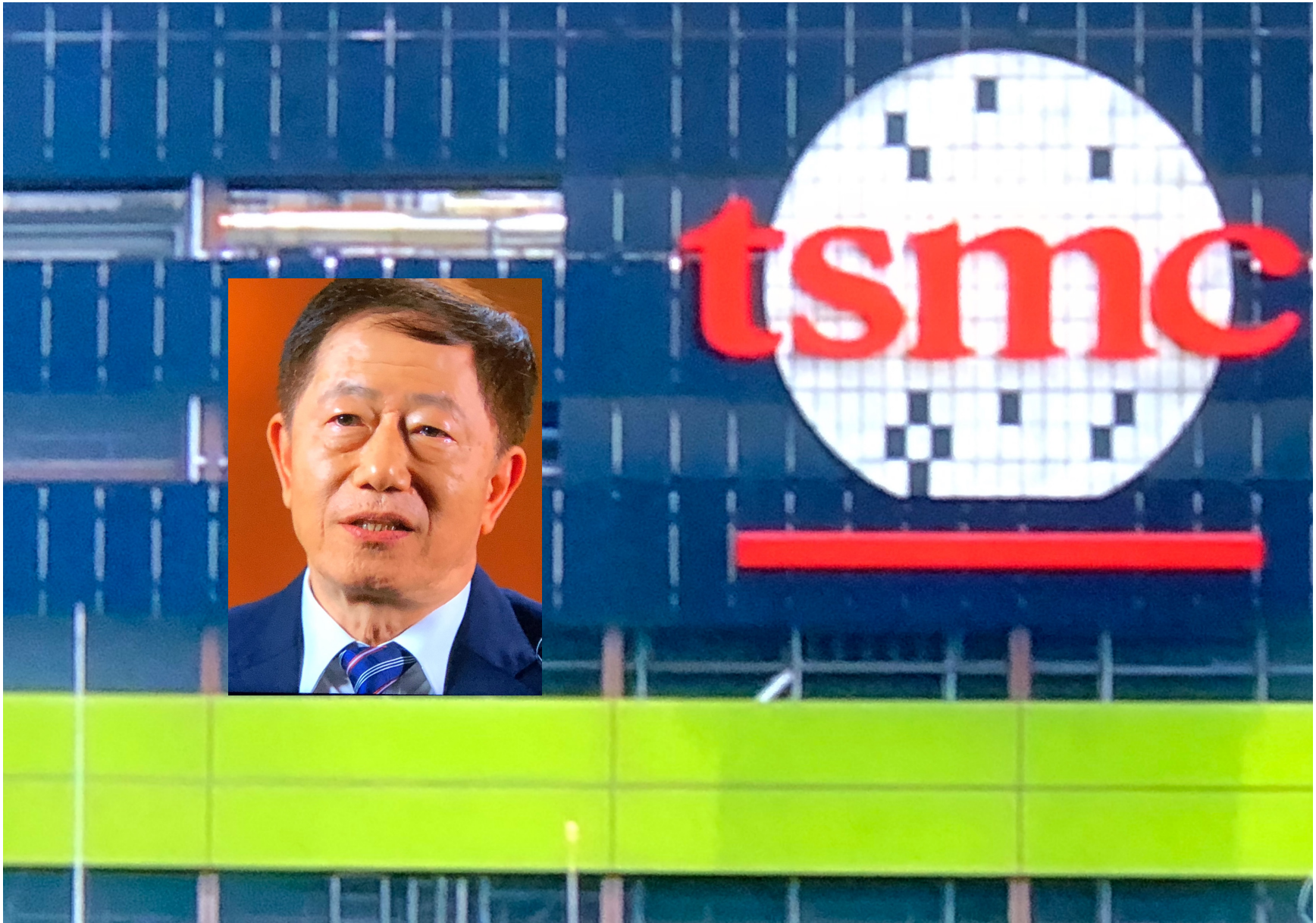

Chip Shortage

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- TSMC also building new fabs (6) in AZ

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Table 4 – TSMC Customer Share of Revenues 2019-2021			
	2019	2020	2021
Apple	24.0%	24.2%	25.4%
Hi-Silicon	15.0%	12.8%	0.0%
Qualcomm	6.1%	9.8%	7.6%
NVIDIA	7.6%	7.7%	5.8%
Broadcom	7.7%	7.6%	8.1%
AMD	4.0%	7.3%	9.2%
Intel	5.2%	6.0%	7.2%
Mediatek	4.3%	5.9%	8.2%
Source: The Information Network (www.theinformationnet.com)			

TSMC Process Revenue

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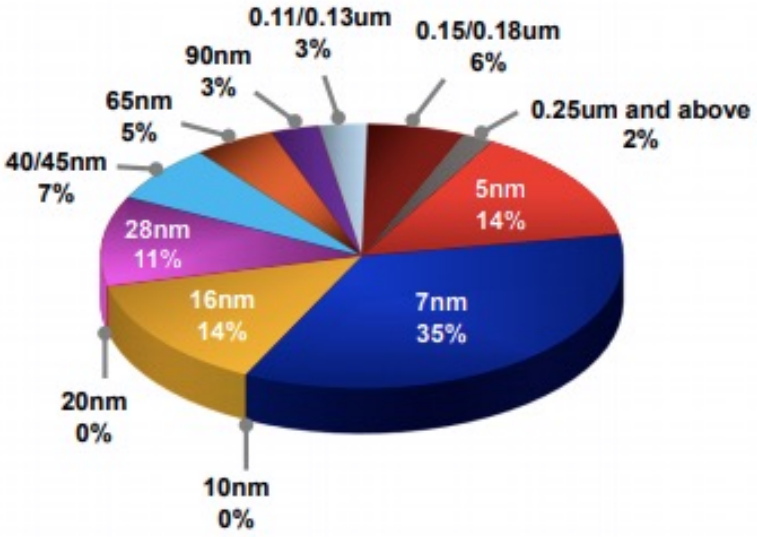
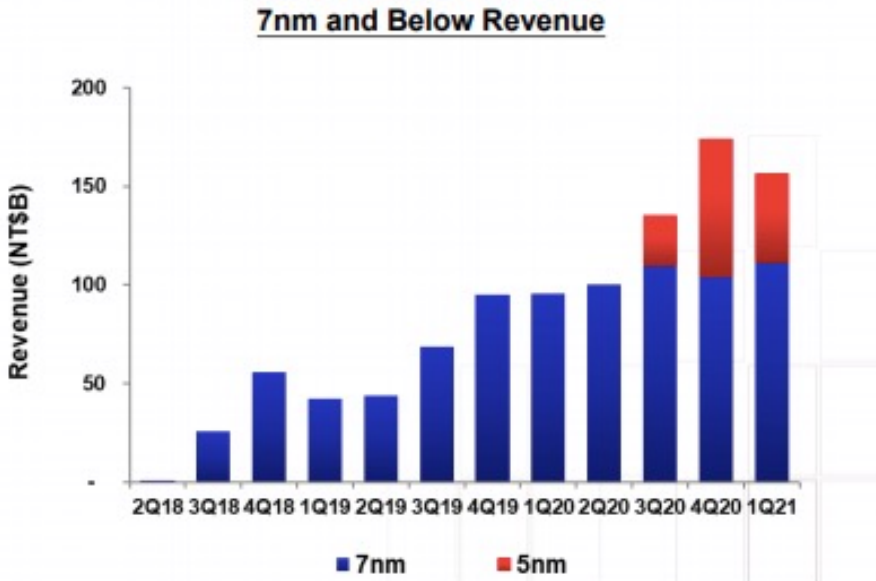
tsmc
Unleash Innovation

1Q21 Revenue by Technology





TSMC vs Samsung 5nm

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	Samsung[24]	TSMC[25]
Process name (nm)	5LPE	N5
Transistor density (MTr/mm^2)	127	173[27]
SRAM bit-cell size (μm^2)	0.026	0.017–0.019
Transistor gate pitch (nm)	57	48
Interconnect pitch (nm)	36	28[29]

TSMC vs Samsung 5/7nm

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5nm

Samsung[24]	TSMC[25]
5LPE	N5
127	173[27]
0.026	0.017–0.019
57	48
36	28[29]

These are real sizes for 7nm node from TSMC, Samsun

7nm

	TSMC N7FF[71]	Samsung 7LPP[72][73]	Intel 10 nm
Transistor density (MTr/mm^2)	96.5[75]	95.3 (7LPE)[76] 81.07 (57PP) 85.57 (54PP)[77]	100.76[78]
SRAM bit-cell size	0.027 µm^2[79]	0.0262 µm^2[79]	0.0312 µm^2
Transistor Gate Pitch	54 nm	54 nm	54 nm
Transistor Fin Pitch	Unknown	27 nm	34 nm
Transistor Fin Height	Unknown	Unknown	53 nm
Minimum (metal) pitch	40 nm	46 nm	36 nm

TSMC's New Fabs in US

Jeff Drobman

TSMC

TSMC Plans Six Wafer Fabs in Arizona

by Scotten Jones on 03-10-2021 at 10:00 am
Categories: Foundries, TSMC
7 Comments

Larger than Taiwan?

$35B

There are reports in the media that TSMC is now planning six Fabs in Arizona (the image above is Fab 18 in Taiwan). The original post I saw referred to a Megafab and claimed six fabs with 100,000 wafers per month of capacity (wpm) for $35 billion dollars. The report further claimed it would be larger than TSMC fabs in Taiwan.

TSMC New Fabs in AZ

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Now here is a YouTube channel doing the same thing at TSMC's new Phoenix fab.

TSMC New Fabs in AZ

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https://www.youtube.com/watch?v=GU87SH5e0eI

https://semiwiki.com/forum/index.php?threads/tsmc-mega-factory-north-phoenix-video-5.15643/

TSMC MEGA Factory North Phoenix Video 5

TSMC in US

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TSMC's glass-walled office building at the construction site on the outskirts of northern Phoenix in March 2024.

TSMC in US

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Taiwan Semiconductor Manufacturing Co **(2330.TW)** said on Wednesday that a new chip manufacturing technology called "A16" will enter production in the second half of 2026, setting up a showdown with longtime rival Intel **(INTC.O)** over who can make the world's fastest chips.

TSMC, the world's biggest contract manufacturer of advanced computing chips and a key supplier to Nvidia **(NVDA.O)** and Apple **(AAPL.O)**, announced the news at a conference in Santa Clara, California, where TSMC executives said that makers of AI chips will likely be the first adopters of the technology rather than a smartphone maker.

TSMC in US

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Zhang said that TSMC does not believe it needs to use a ASML's **(ASML.AS)** new "High NA EUV" lithography tool machines to build the A16 chips. Intel last week revealed that **it plans to be the first to use the machines**, which can cost $373 million each, to develop its 14A chip.

TSMC also revealed a new technology for suppling power to computer chips from the backside of the chip, which helps speed up AI chips and will be available in 2026.

Intel has announced a similar technology intended to be one of its primary competitive advantages.

TSMC in US

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In mid-2023, TSMC announced delays in the construction of its first facility in Arizona, dubbed Fab 21 — production at the facility would start in 2025 instead of 2024 as planned. TSMC blamed a shortage of skilled workers. Construction unions, however, complained of safety hazards and questioned if TSMC was using this as an excuse to bring in cheap labor from Taiwan.

TSMC in Japan

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Although the factory in Japan will make less-advanced chips than the American one, the news out of Kumamoto prompted feelings of envy in Phoenix. There, engineers felt that they were falling even further behind.

The same weekend as the opening of the Japanese plant, Taiwanese engineers discussed the struggle of working with Americans at a gathering in Phoenix. “The Japan factory opened first. I’m very frustrated,” a Taiwanese engineer said.

TSMC in US

TSMC Arizona's first two facilities are expected to make 600,000 wafers a year — a fraction of the company's current annual capacity of 16 million wafers. Many of the chips made in the U.S. still need to be shipped back to Asia for assembly, testing, and packaging. Chip packaging company Amkor, which has most of its factories in Asia, will build a plant in Arizona to package Apple chips made at TSMC.

TSMC in US

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Jobs for Americans

Some 2,200 employees now work at TSMC's Arizona plant, with about half of them deployed from Taiwan. While tension at the plant simmers, TSMC has been ramping up its investments, recently securing billions of dollars in grants and loans from the U.S. government. Whether or not the plant succeeds in making cutting-edge chips with the same speed, efficiency, and profitability as facilities in Asia remains to be seen, with many skeptical about a U.S. workforce under TSMC's army-like command system. "[The company] tried to make Arizona Taiwanese," G. Dan Hutcheson, a

TSMC in US

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Jobs for Americans

duction. Chang has since also warned against the lack of manufacturing talent in the U.S., and how hard it would be for Taiwanese managers to supervise Americans. Speaking to the Vying for Talent podcast in April 2022, Chang concluded that the U.S.' attempt to onshore semiconductor manufacturing would be "a very expensive exercise in futility."

TSMC in US

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Jobs for Americans

There simply are too few U.S. workers with the skills necessary for semiconductor manufacturing.

"TSMC was the worst possible place to work on Earth."

TSMC in US

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Jobs for Americans

But over the next two years, Bruce came to realize that the reality of working at TSMC wasn't exactly what he had envisioned. While working on nanometer-level processes to make state-of-the-art chips, he struggled with language barriers, long hours, and a strict hierarchy. Bruce soon began second-guessing what he had signed up for. The plant, which was originally set to begin operating in 2024, fell woefully behind schedule; production at the facility is now set to start in 2025. Bruce, who said he

TSMC on Moore's Law

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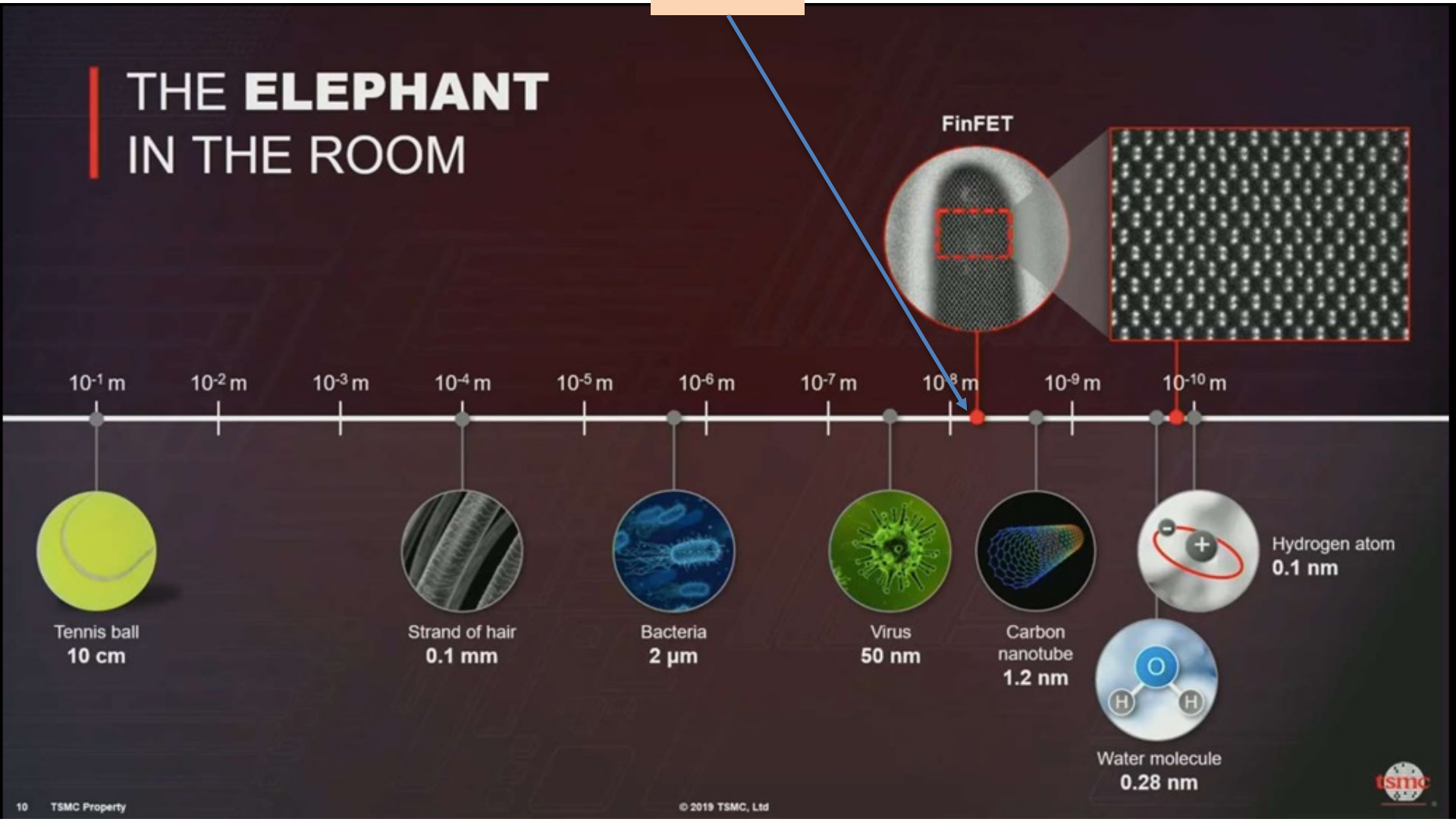
7-10 nm



TSMC Roadmap

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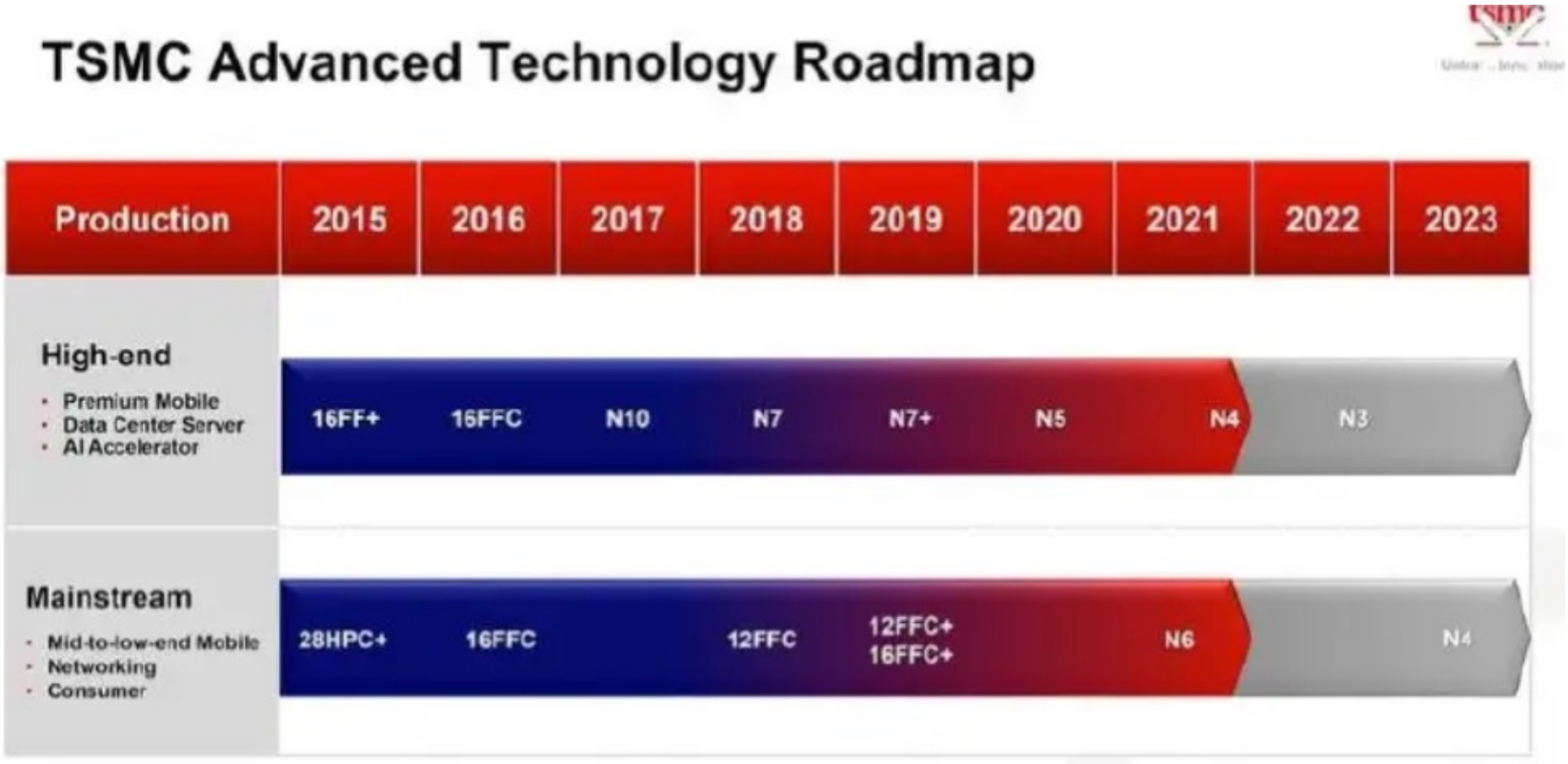
June 2021



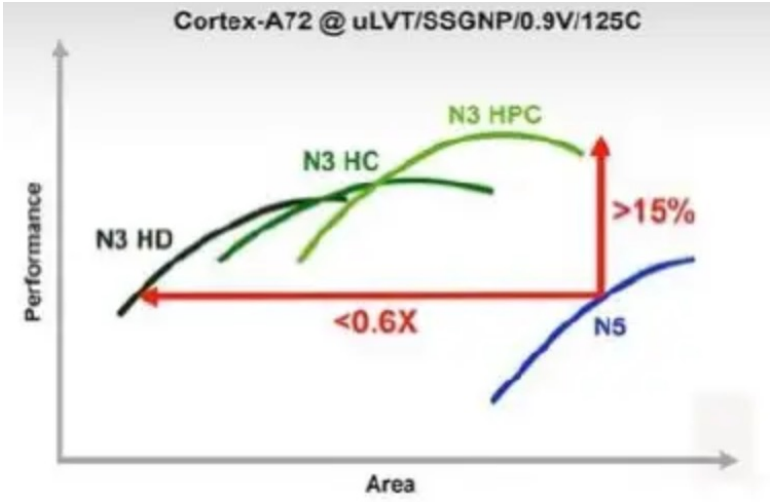
TSMC Roadmap

June 2021

N7+ represents the introduction of EUV lithography to the baseline N7 process. N5 has been in volume production since 2020.

N3 will remain a FinFET-based technology offering, with volume production starting in 2H2022. Compared to N5, N3 will provide:

- +10-15% performance (iso-power)
- -25-30% power (iso-performance)
- +70% logic density
- +20% SRAM density
- +10% analog density



TSMC foundation IP has commonly offered two standard cell libraries (of different track heights) to address the unique performance and logic density of the HPC and mobile segments. For N3, the need for "full coverage" of the performance/power (and supply voltage domain) range has led to the introduction of a third standard cell library, as depicted below.

TSMC Roadmap- RF

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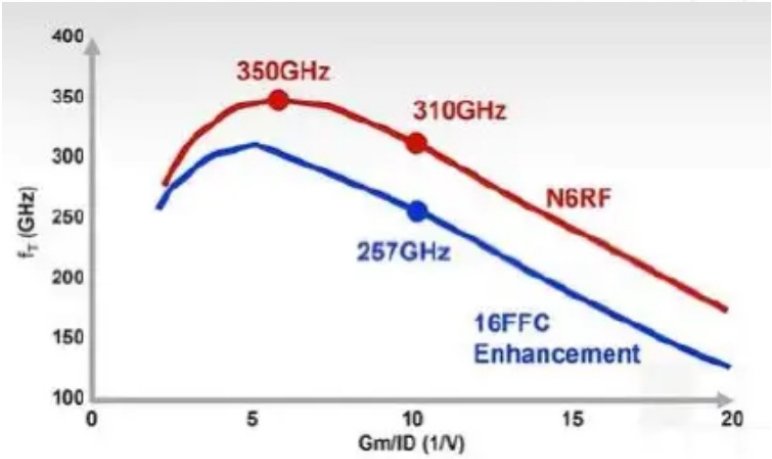
June 2021

TSMC RF Technology Roadmap

Production		2018	2019	2020	2021	2022	2023
General RF (<=10GHz)	Premium	16FFC RF Enh I			N6RF		N6RF Enh
	Mainstream	28HPC+ RF V1.0			22ULP/ULL RF V1.2		
mmWave RF (>=24GHz)	Premium	16FFC RF Enh I					
	Mainstream	22ULP/ULL RF V1.2					
RF Frontend (<= 10GHz)	Premium	N40SOI			N40SOI Enh		
	Mainstream	0.13SOI					

General RF applications: 5G (sub 6 GHz)/4G RF transceiver, WLAN, Bluetooth and etc.
mmWave RF applications: 5G mmWave FEM, automotive radar and etc.
RF Frontend applications: LNA and switch



TSMC Roadmap: Packaging

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New Plant June 2021

TSMC's planned U.S. plant would involve its latest 3D stacking technologies to arrange chips with different functions in one package, sources told Nikkei Asia.

TSMC is also building an advanced chip packaging facility in the Taiwanese city of Miaoli that is set to go into production in 2022. Advanced Micro Devices and Google will be among the first customers, Nikkei Asia has reported.

The facility would be TSMC's first chip packaging plant outside of Taiwan so this is a very big deal. Chip packaging is an increasingly competitive field but TSMC is on par or even ahead of Intel and Samsung in a short amount of time. The big TSMC advantage is the tight collaboration with big name customers and ecosystem partners.

Per the 2021 TSMC Symposium:

In 2020, TSMC extended their support to encompass 281 distinct process technologies, shipping 11,617 products to 510 customers. As in previous years, TSMC proudly stated “we have never shut down a fab.”

Current capacity in 2020 exceeds 12M (12” equivalent) wafers, with expansion investments for both advanced (digital) and specialty process nodes.

TSMC plans to invest a total of US$100 billion over the next three years, including a US$30 billion capital expenditure this year, to support global customer needs.

TSMC’s global 2020 revenue was $47.78B – the $30B annual commit to fab expansion certainly would suggest an expectation of significant and extended semiconductor market growth, especially for the 7nm and 5nm process families. For example, new tapeouts (NTOs) for the 7nm family will be up 60% in 2021.

TSMC has begun construction of a US fab in Phoenix, AZ – volume production of the N5 process will commence in 2024 (~20K wafers per month).

TSMC + ARM in 3D

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ARM quad core A72

7nm ***chiplet***

Technology
3D Multi-chip Systems

The world's largest foundry joined with partner Arm to announce their new 7nm chiplet system using TSMC's advanced packaging at TSMC's Open Innovation Platform Ecosystem Forum in Santa Clara, Calif., last week.

Rather than the typical SoC with system components arranged on a single die, a chiplet system is optimized for modern HPC processors that partition large multi-core designs into smaller chipsets. This approach allows each chiplet — each die in a package of multiple dice — to be built in different process technologies. The approach is expected to deliver better yields and overall cost-effectiveness.

The TSMC/Arm system is a dual-chiplet implemented in 7nm, with each chiplet containing four Arm Cortex-A72 processors and an on-die interconnect mesh bus. The die-to-die inter-chiplet connection features scalable 0.56pJ/bit (pico-Joules per bit) power efficiency, 1.6Tbps/mm^2 (terabits per second per square millimeter) bandwidth density, and 0.3V LIPINCON low-voltage interface reaching 8GT/s (giga transactions per second) and 320 Gpbps bandwidth.

"TSMC has the most advanced semiconductor nodes in production, and that gives them some advantages from a silicon side," TechSearch President Jan Vardaman told EE Times. "From a packaging side, each company has an approach that could deliver a similar solution, with TSMC and Intel releasing the most information so far."

TSMC, Arm Show 3DIC Made of Chiplets
Source: EE Times (02 Oct 2019)

TSMC New Techs

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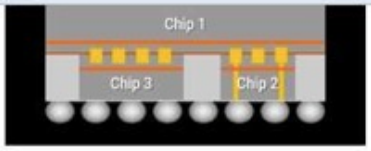
Abbreviation	What does it stand for?	What is it?
3DIC	Three-dimensional integrated circuit	
CoWoS	Chip on Wafer on Substrate	TSMC's CoWoS (Chip-on-Wafer-on-Substrate) packaging technology integrates logic and memory chips in a three-dimensional configuration. CoWoS packaged chips are used in artificial intelligence, cloud computing, data center and super computer applications.
InFO	Integrated Fan-Out	TSMC's InFO (Integrated Fan-Out) packaging technology eliminates the substrate used in traditional electronic packages, enabling smaller size, lower power and higher interconnect density.
LIPNCON	Low voltage In Package INterConect	Low-voltage-In-Package-INterCONnect (LIPINCON) is a proprietary system interconnect architecture that facilitates data transmission across all linked components. LIPINCON is an interconnect architecture designed for chiplet designs with advanced packaging technologies such as InFO and CoWoS.
RDL	Redistribution Layer	A redistribution layer (RDL) is an extra metal layer on a chip that makes the IO pads of an integrated circuit available in other locations of the chip, for better access to the pads where necessary.
SoIC		SoIC is a frontend wafer-process that integrates multi-chip, multi-tier, multi-function and mix-and-match technologies to enable high speed, high bandwidth, low power, high pitch density and minimal footprint and stack-height heterogeneous 3DIC integration.

SoC

TSMC

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TSMC operates four major 300mm manufacturing sites in Taiwan and one in China. The four sites in Taiwan are all GigagFab sites, Fab 12, Fab 14, Fab 15 and Fab 18 are each made up of 6 or 7 wafers fabs sharing central facility plants. This Gigafab approach is believed to reduce construction costs by about 25% versus building a single stand-alone fab. The china fab location is smaller with 2 fabs at one location but the fab was equipped with used equipment transferred from fabs in Taiwan because the fab is trailing edge. If TSMC really builds a single US fab running 20,000 wpm the resulting cost to produce a wafer will be roughly 1.3% higher than for a GigaFab location due to higher construction costs. I believe it is unlikely the site will be equipped with used equipment transferred from Taiwan. The cost to build and equip the fab for 20,000 wpm should be approximately $5.4 billion dollars.

Gigafabs

Locating a fab in the US versus Taiwan will result in the fab incurring US labor and utility costs, this will add approximately 3.4% to the wafer manufacturing cost.

The capacity of the fab is also smaller than a "typical" fab at advanced nodes, the three 5nm fabs TSMC is operating or planning for Taiwan are all 30,000 wpm. A 20,000 wpm fab will have an approximately 3.8% increase in costs versus a 30,000 wpm fab under the same conditions.

20-30K wpm

In total, wafers produced at the TSMC Arizona fab will be approximately 7% more expensive to manufacturer than a wafer made in Fab 18 in Taiwan. This does not account for the impact of taxes that are likely to be higher in the US than in Taiwan.

In the announcement TSMC has said the total spending on the project between 2021 and 2029 would be $12 billion dollars. That leaves money for a future expansion or conversion to 3nm. That would be almost enough money to add a second 20,000 wpm fab running 3nm as one possible example.

$12B

In summary the "announced" fab would likely be TSMC's highest cost production site. It will be interesting to see if the fab materializes.

TSMC in US

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Cost Analysis of the Proposed TSMC US Fab

by Scotten Jones on 05-19-2020 at 10:00 am
Categories: IC Knowledge, Semiconductor Services, TSMC
29 Comments

On May 15th TSMC "announced its intention to build and operate an advanced semiconductor fab in the United States with the mutual understanding and commitment to support from the U.S. federal government and the State of Arizona."

The fab will run TSMC's 5nm technology and have a capacity of 20,000 wafers per month (wpm). Construction is planned to start in 2021 and production is targeted for 2024. Total spending on the project including capital expenditure will be $12 billion dollars between 2021 and 2029.

This announcement is undoubtedly the result of intense pressure on TSMC by the US government and it is also coming out today that TSMC will stop taking orders from Huawei also under pressure from the US.

New Chip Fabs

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THE VERGE

TSMC in Arizona

The chip-making industry has production capacity increases planned, but many of the new plants won't be online anytime soon. TSMC and Sony's new $7 billion chip factory in Japan won't see production start until the end of 2024, the same year as TSMC's new $12 billion Arizona plant. TSMC has said it plans to invest over $100 billion in new chip factories over the next three years, while Intel plans to spend a similar amount over the next decade on investments in the US and Europe.

New Chip Fabs

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Quora

TSMC in Arizona

What is Intel's plan to regain chip market dominance from the likes of TSMC? What are its chances of doing so?

Jeff Drobman, Lecturer at California State University, Northridge (2016-present)

Answered just now

Apple's mobile A14/15 and MacBook M1 chips are fabbed by TSMC at 5nm. TSMC is the world leader in process density — first to 5nm, with Samsung a close 2nd, and are now testing 3nm. Intel has now joined AMD in using TSMC to fab its high-end chips at 7nm and 5nm. Intel has new plans to catch up, according to this estimate (see slide).

TSMC 4nm

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Apple Orders 4nm Chip Production for Next-Generation Macs

Tuesday March 30, 2021 12:35 am PDT by Sami Fathi

Apple has booked the initial production capacity of 4nm chips with long-time supplier TSMC for its next-generation Apple silicon, according to industry sources cited in a new report today from *DigiTimes*.

Apple & TSMC

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> *Apple has already booked the initial capacity of TSMC's N4 for its new-generation Mac series, the sources indicated. Apple has also contracted TSMC to make its next-generation iPhone processor dubbed A15, built using the foundry's N5 Plus or N5P process node, the sources said.*
>
> *TSMC is expected to kick off production for Apple's A15 chip that will power the upcoming iPhone 13 series by the end of May, the sources noted.*

The latest Apple silicon, the M1 chip, is the first of its kind in the industry based on the 5nm process. The A14 Bionic chip in the iPad Air and iPhone 12 lineup is also based on the 5nm process. According to the report, Apple is already looking to the 4nm chip process for its next-generation Apple silicon.

A timeframe for when these new 4nm chips will debut isn't provided, but *DigiTimes* does report that TSMC will move to volume production of the new process in Q4 of 2021, ahead of the previously set 2022 timeframe. Additionally, Apple plans to use an enhanced version of the 5nm process for the A15 chip in the iPhone 13, with production set to get underway by the end of May.

The smaller process reduces the chips' actual footprint and provides better efficiency and performance. Apple's expected to launch multiple new Macs this year with more powerful Apple silicon chips; however, there's no indication that any will be based on the 4nm process.

TSMC $ Apple

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Taiwan Semiconductor asked for 2023 price increase from Apple, tech giant said no: report

Sep 28, 2022 11:23 AM ET | **Taiwan Semiconductor Manufacturing Company Limited (TSM)** | Chris Ciaccia, SA News Editor

Taiwan Semiconductor (NYSE:TSM) is slated to raise prices on its customers starting in 2023, but the company's largest customer, Apple (NASDAQ:AAPL), has reportedly told the global foundry no deal.

According to Chinese news outlet Economic Daily News, Taiwan Semiconductor (TSM) wanted to increase the price of the process for its 3 nm process by 3%, which may be used in the A17 chip in some of Apple's (AAPL) Mac computers and perhaps next year's iPhone. However, the tech giant refused and said no, the news outlet said, citing sources.

In May, it was reported that Taiwan Semiconductor Manufacturing (TSM) had started to tell some of its customers that it will raise its prices between 5% and 9%, starting next year, due to inflation concerns, rising costs and its expansion.

Cupertino, California-based Apple (AAPL) is Taiwan Semiconductor's (TSM) largest customer and some reports have suggested that it accounts for as much as 25% of the global foundry's annual revenue.

25%

Apple

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TSMC new fabs in Arizona will open in 2024

TSMC 3nm

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SemiWiki.com
The Open Forum for Semiconductor Professionals

8-17-22

TSMC's Initial 3nm HVM Yield To Be Better Than Its 5nm

TSMC **N3e** is the HPC version for Intel, AMD, Nvidia, etc... The SoC companies Apple, Mediatek, will use **N3**. Please remember that TSMC sets expectations on the conservative so they don't disappoint. According to my sources N3 for Apple was frozen in December and the N3e process is now frozen with HVM starting in 1H 2023.

- Apple now in production (HVM) with **4nm**

Section

Jeff Drobman

TSMC at VLSI Conf 2021

TSMC Slides

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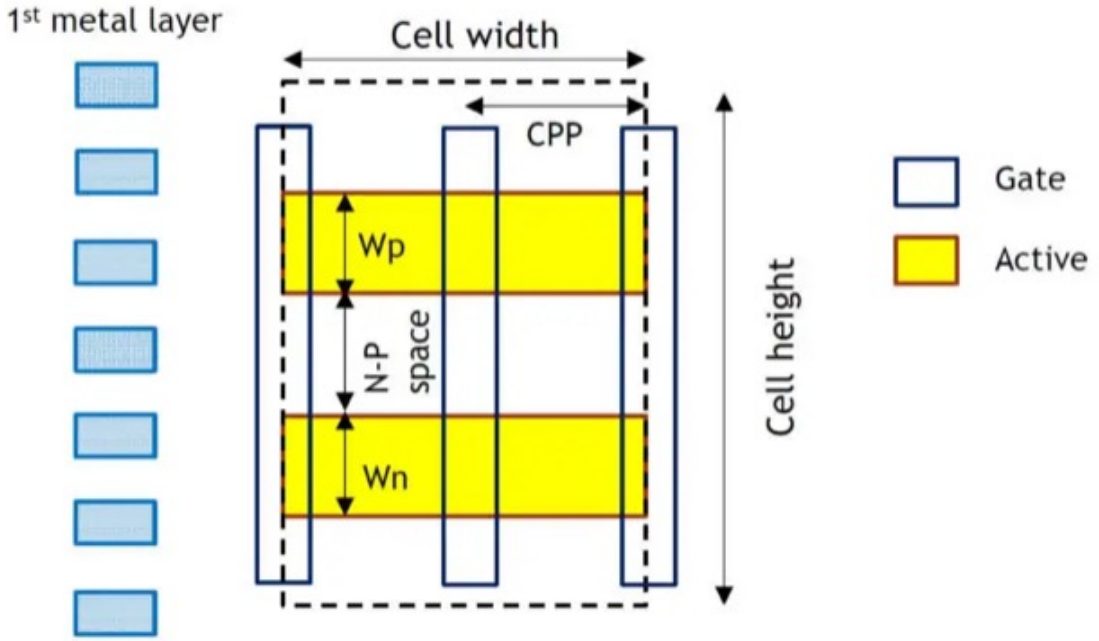
IC Knowledge

VLSI Symposium – TSMC and Imec on Advanced Process and Devices Technology Toward 2nm

by Scotten Jones on 07-02-2021 at 6:00 am
Categories: Events, IC Knowledge, Semiconductor Services, TSMC

CMOS Density Improvement

- Logic standard cell area ~ CPP x Cell height



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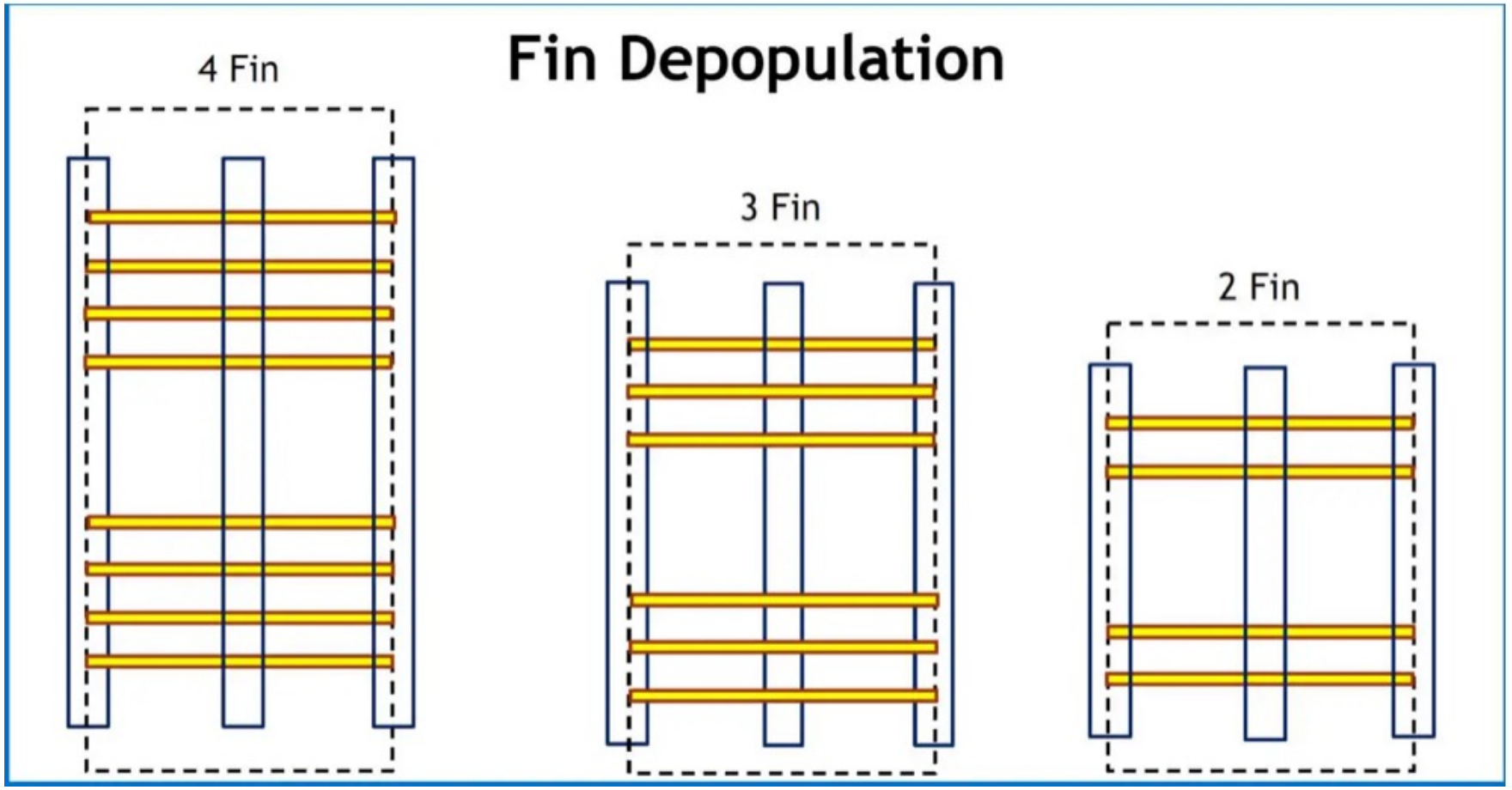

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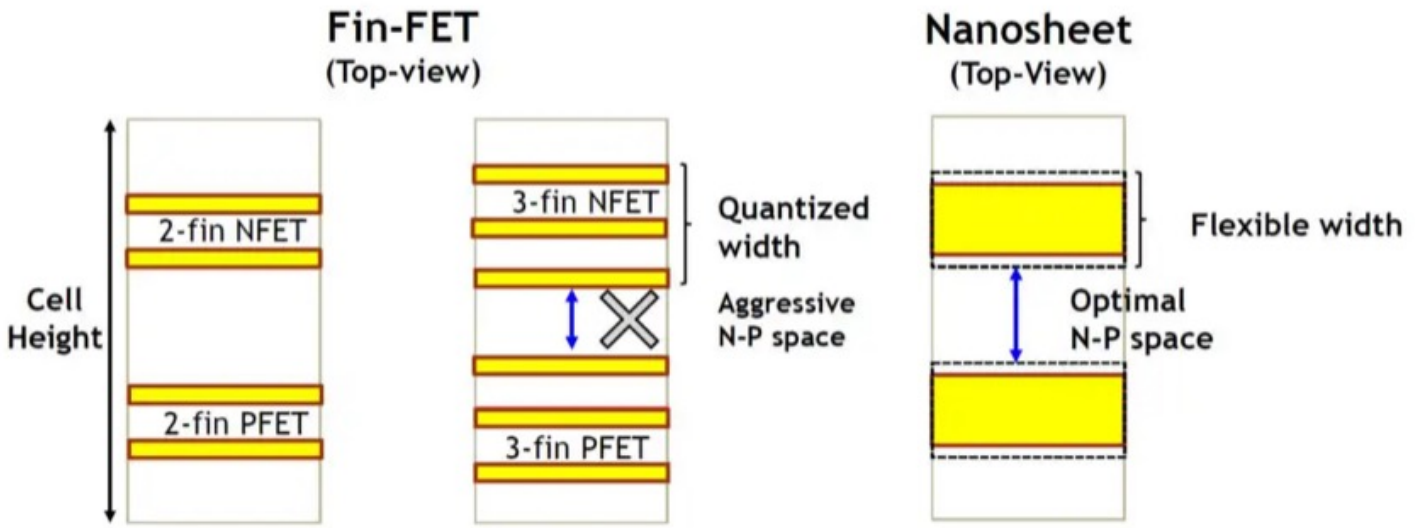
Flexible Sheet Width

- Continuous width adds design flexibility



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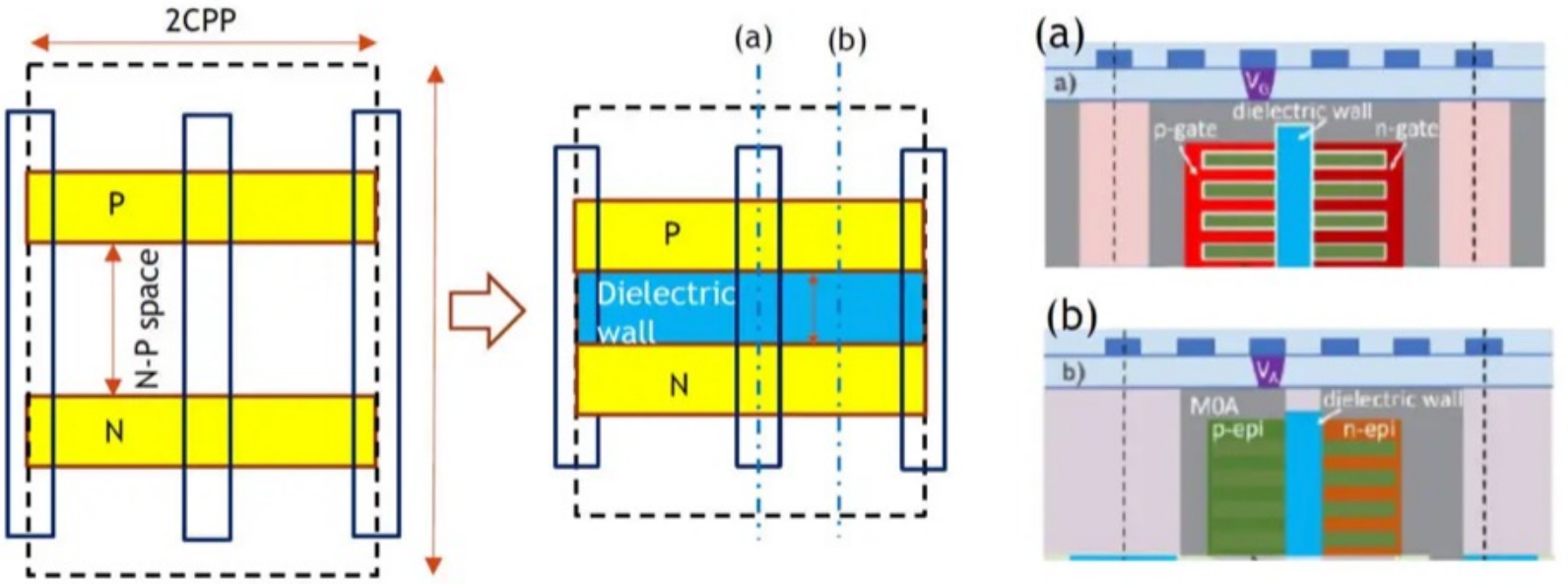
by Scotten Jones on 07-02-2021 at 6:00 am
Categories: Events, IC Knowledge, Semiconductor Services, TSMC

Standard Cell height Scaling: Forksheet

- Dielectric wall between N and P: gate isolation, S/D isolation, end cap ↓



Challenge: Short channel control

P. Weckx et.al., 2019 IEDM (IMEC)

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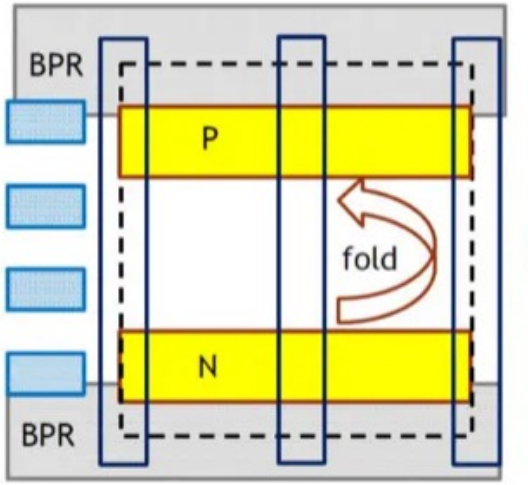
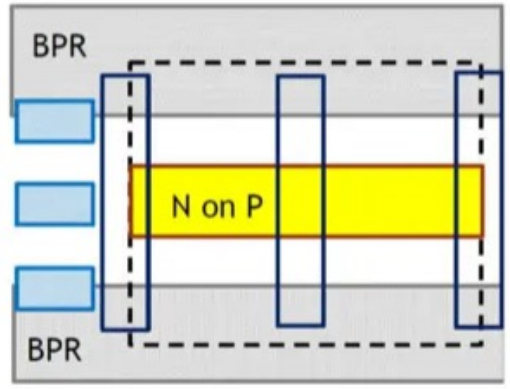
VLSI Symposium – TSMC and Imec on Advanced Process and Devices Technology Toward 2nm

by Scotten Jones on 07-02-2021 at 6:00 am
Categories: Events, IC Knowledge, Semiconductor Services, TSMC

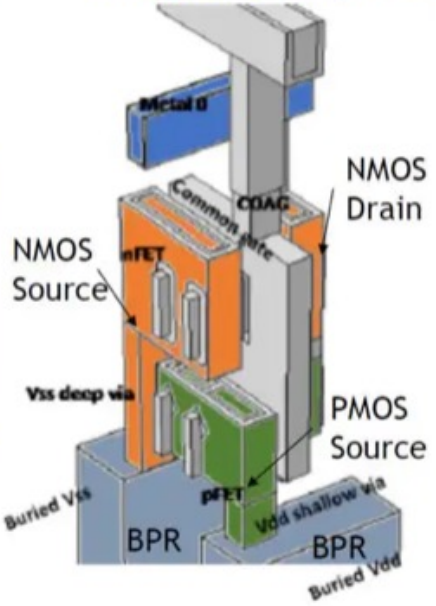
Stacked CMOS

- NMOS and PMOS stacking enables further CH reduction
  - CH limited by signal routing tracks (>=3) and metal pitch





Complementary FET



J. Ryckaert et.al. 2018 VLSI (IMEC)

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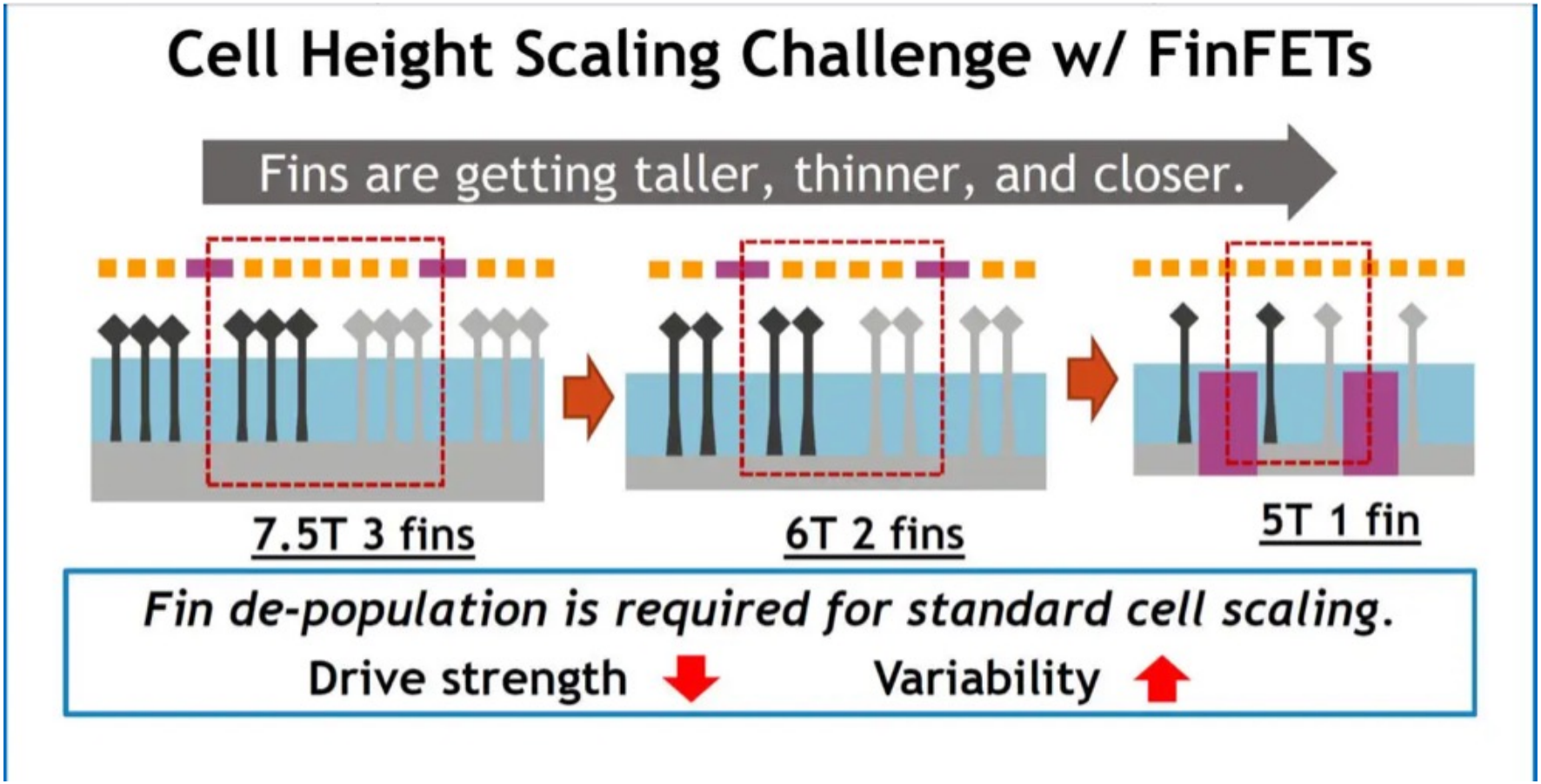

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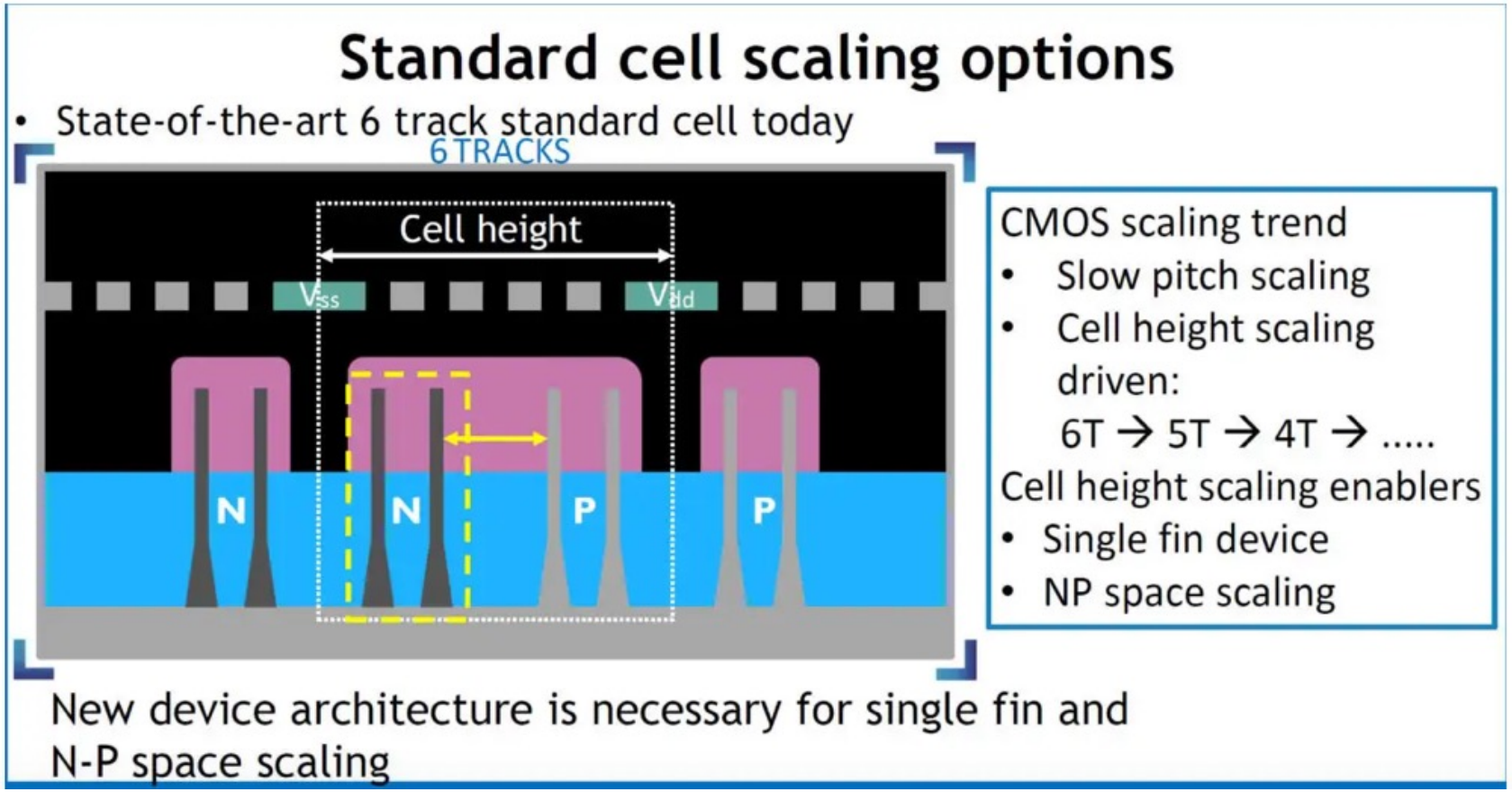

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by Scotten Jones on 07-02-2021 at 6:00 am
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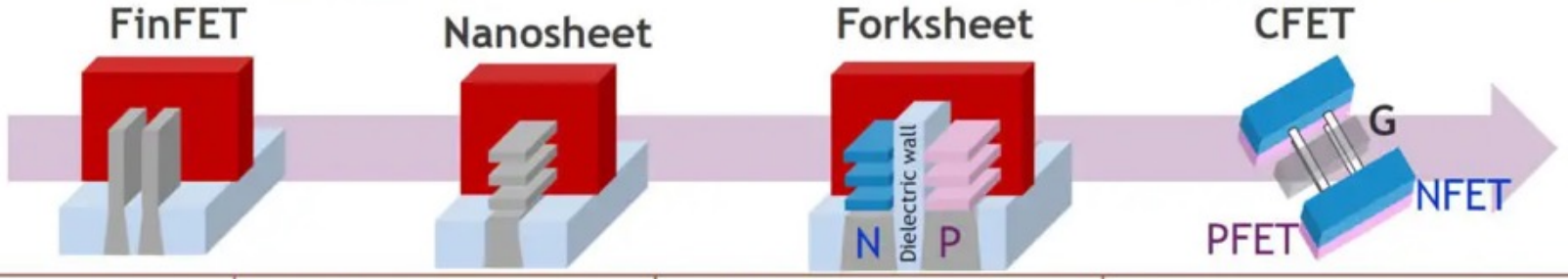
Nanosheet architectures for continuous CMOS scaling

Single Device → *CMOS device architecture*



	Nanosheet	Forksheet	CFET
Wider effective width in single fin	• Stacked nanosheet ch.	• Stacked nanosheet ch. • Small N-P → Wider NS	• Stacked nanosheet ch. • Stacked N&P → Wider NS
N-P space scaling		• Dielectric wall	• Stacked N&P

Nanosheet architectures enable wider effective width and small N-P space

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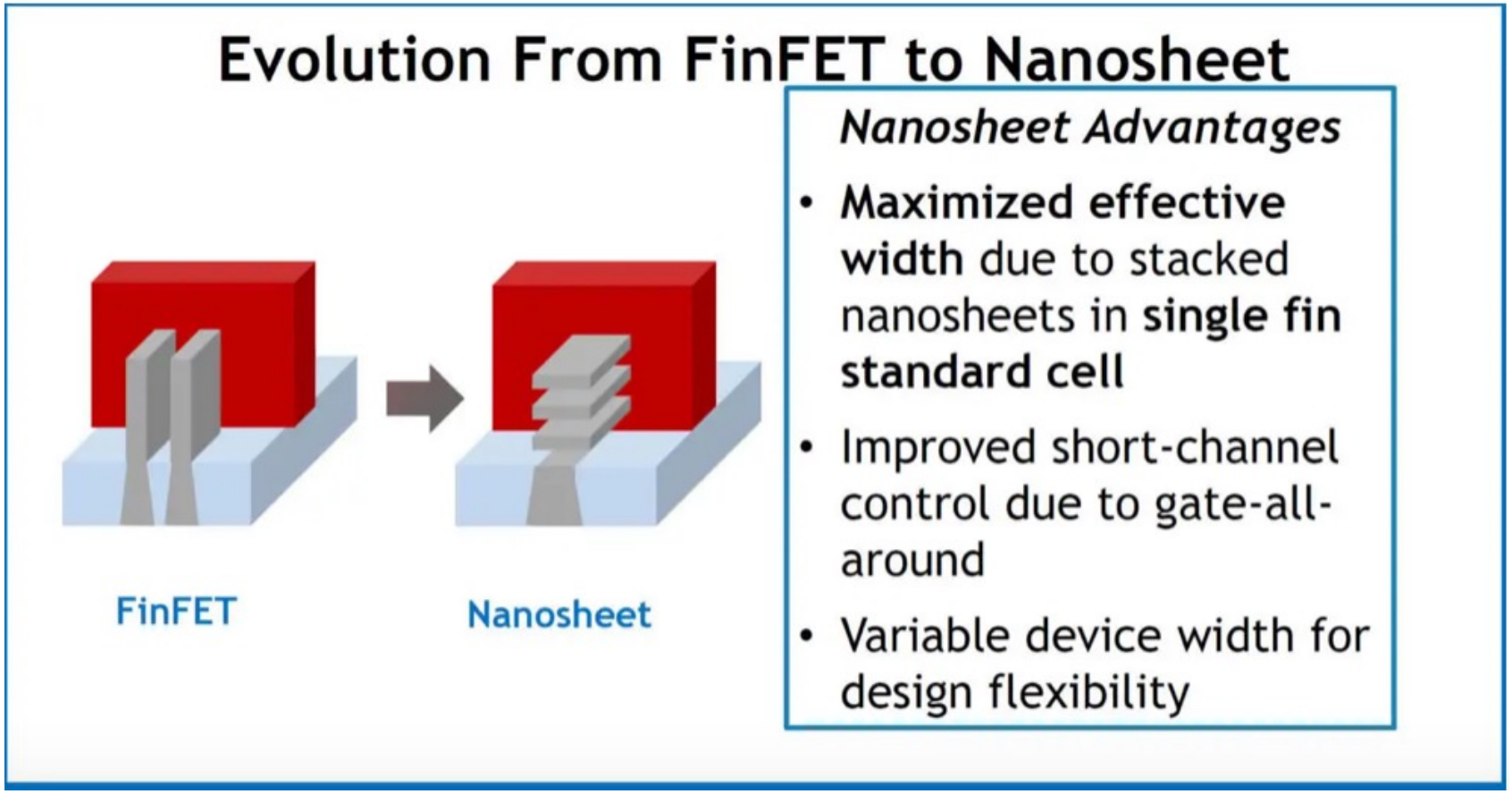

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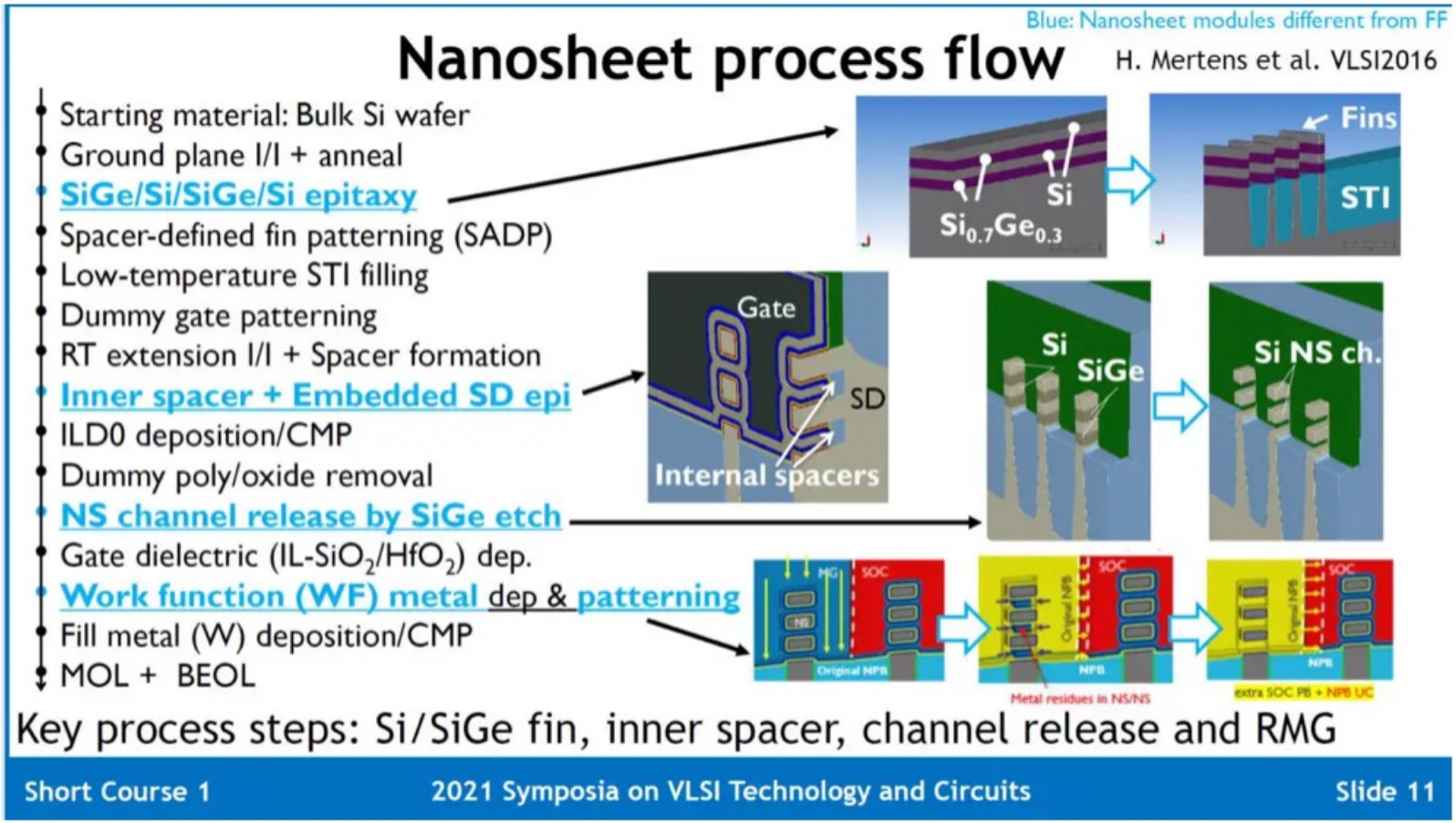

Figure 10. HNS Process Flow.

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by Scotten Jones on 07-02-2021 at 6:00 am
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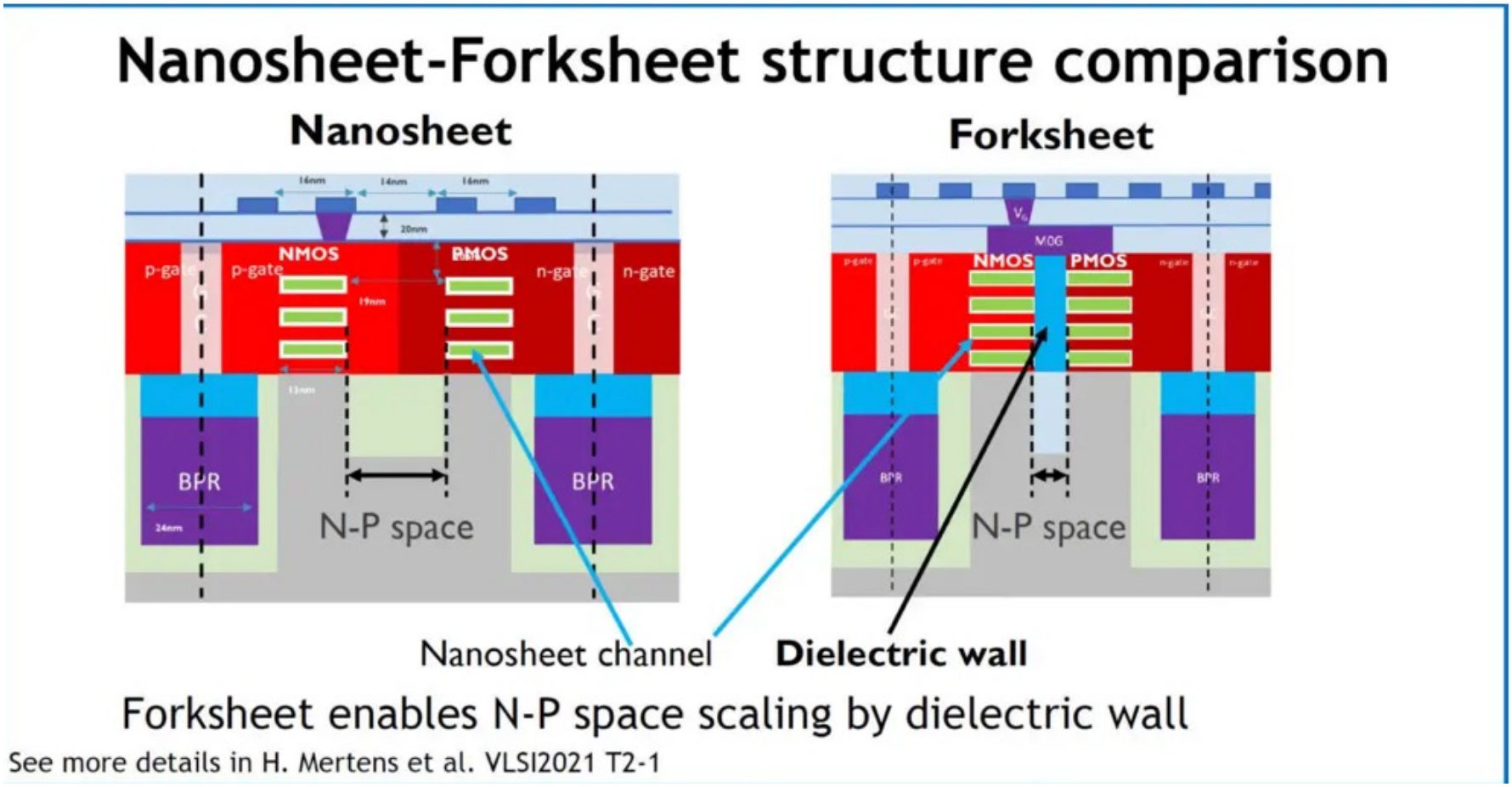

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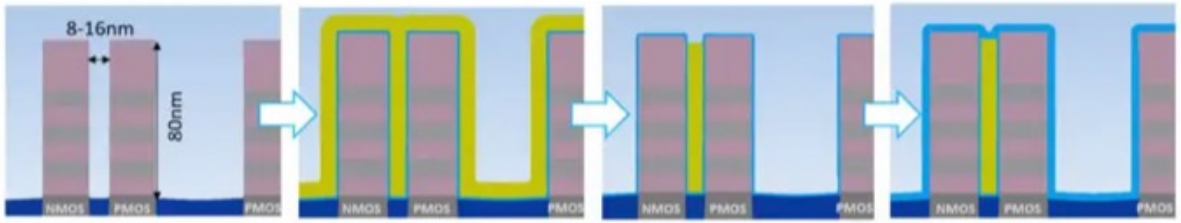
by Scotten Jones on 07-02-2021 at 6:00 am
Categories: Events, IC Knowledge, Semiconductor Services, TSMC

Forksheet process flow

Light Blue: New modules in FS
Blue: Modified modules from NS

- Nanosheet STI
- **Dielectric wall formation**
- Gate patterning
- Spacer and fin recess
- **Inner spacer**
- **Source/drain epitaxy**
- ILD0 CMP
- Dummy poly/oxide removal
- NS channel release by SiGe etch
- **RMG**
- MOL + BEOL



See more details in H. Mertens et al. VLSI2021 T2-1

Forksheet flow is similar as nanosheet flow. Dielectric wall formation and modified inner spacer/SD epi/RMG are key process steps.

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by Scotten Jones on 07-02-2021 at 6:00 am
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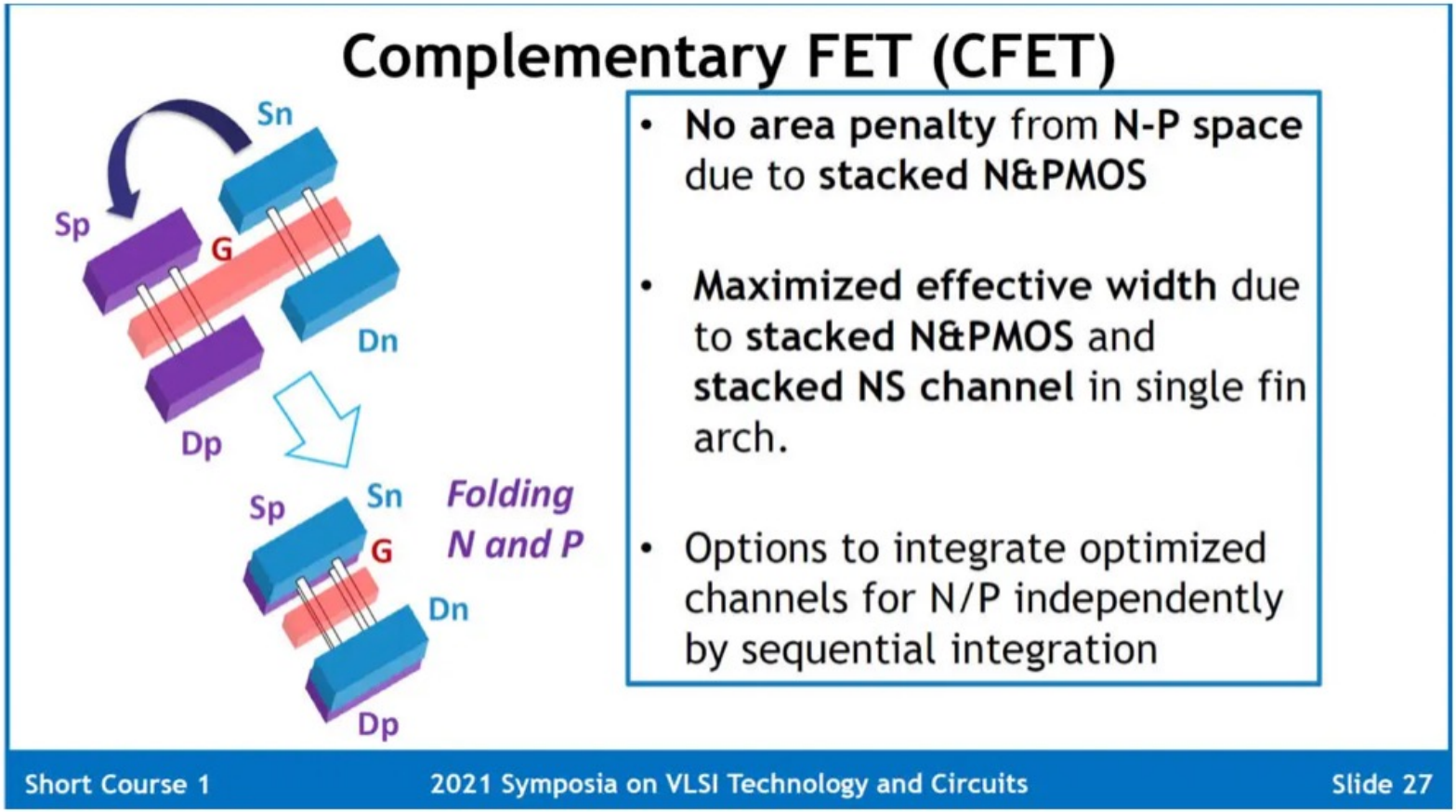

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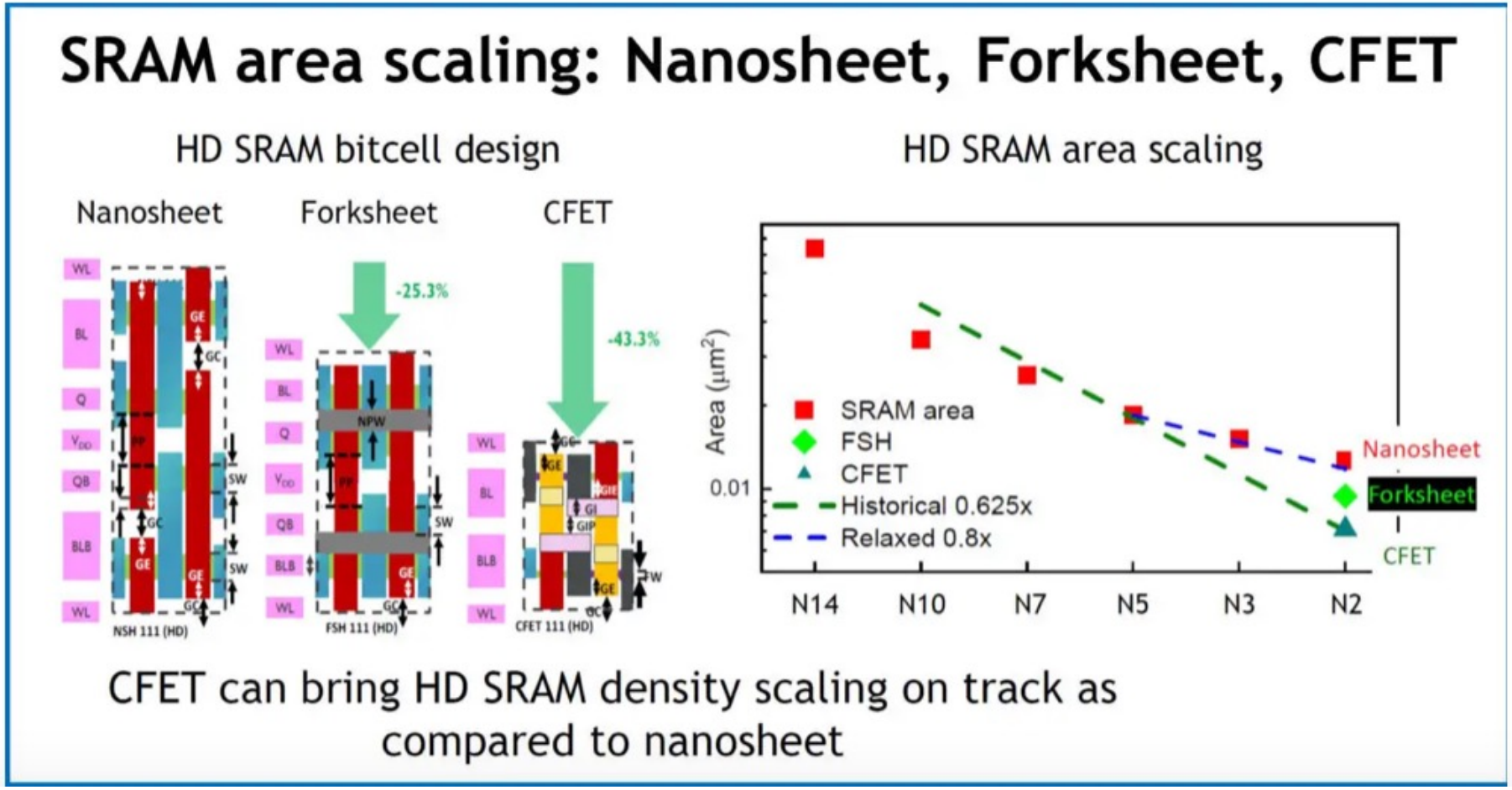

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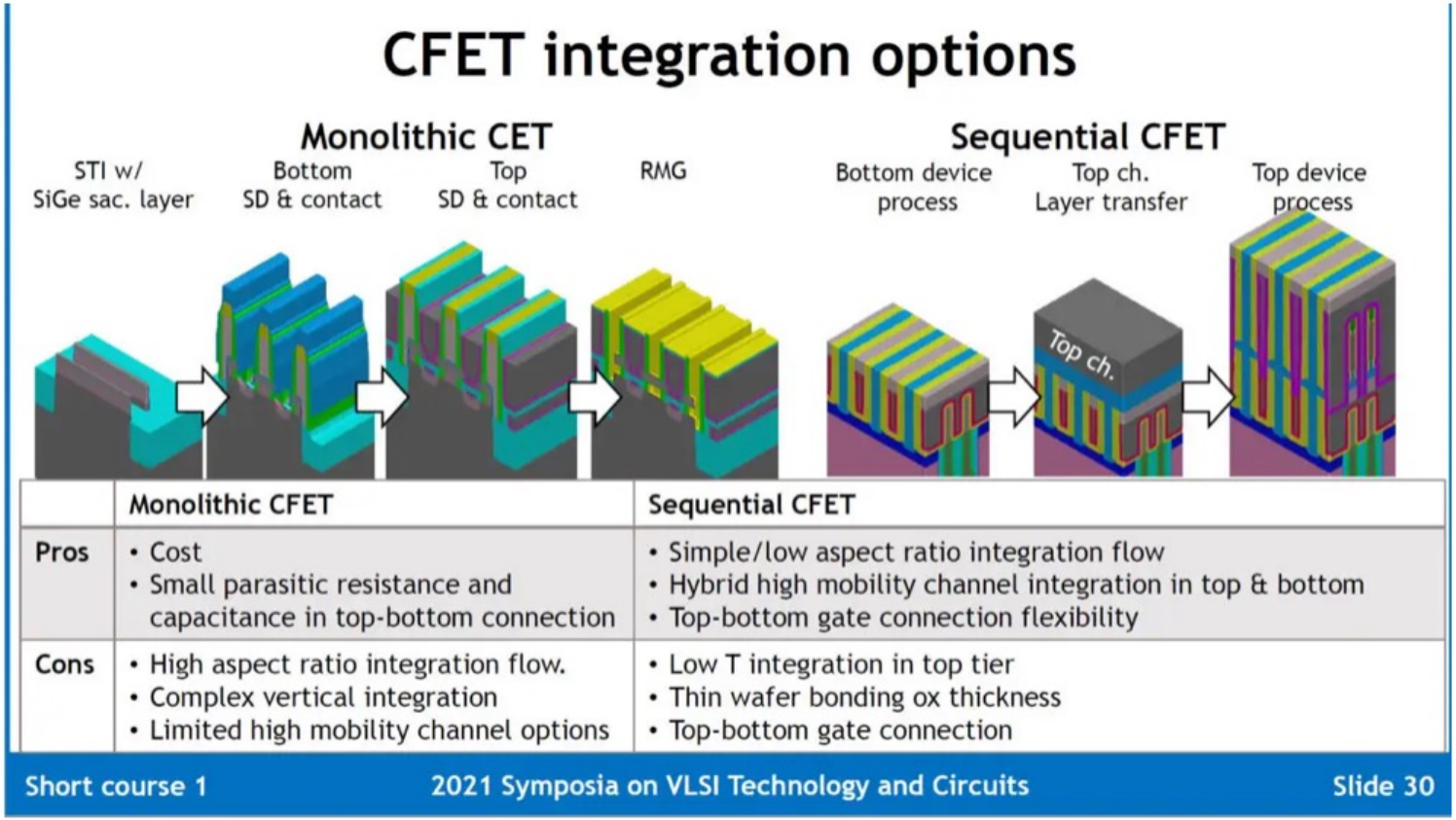

Figure 15. CFET Fabrication Options.

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TSMC at VLSI Conf 2022

TSMC at VLSI Conf ‘22

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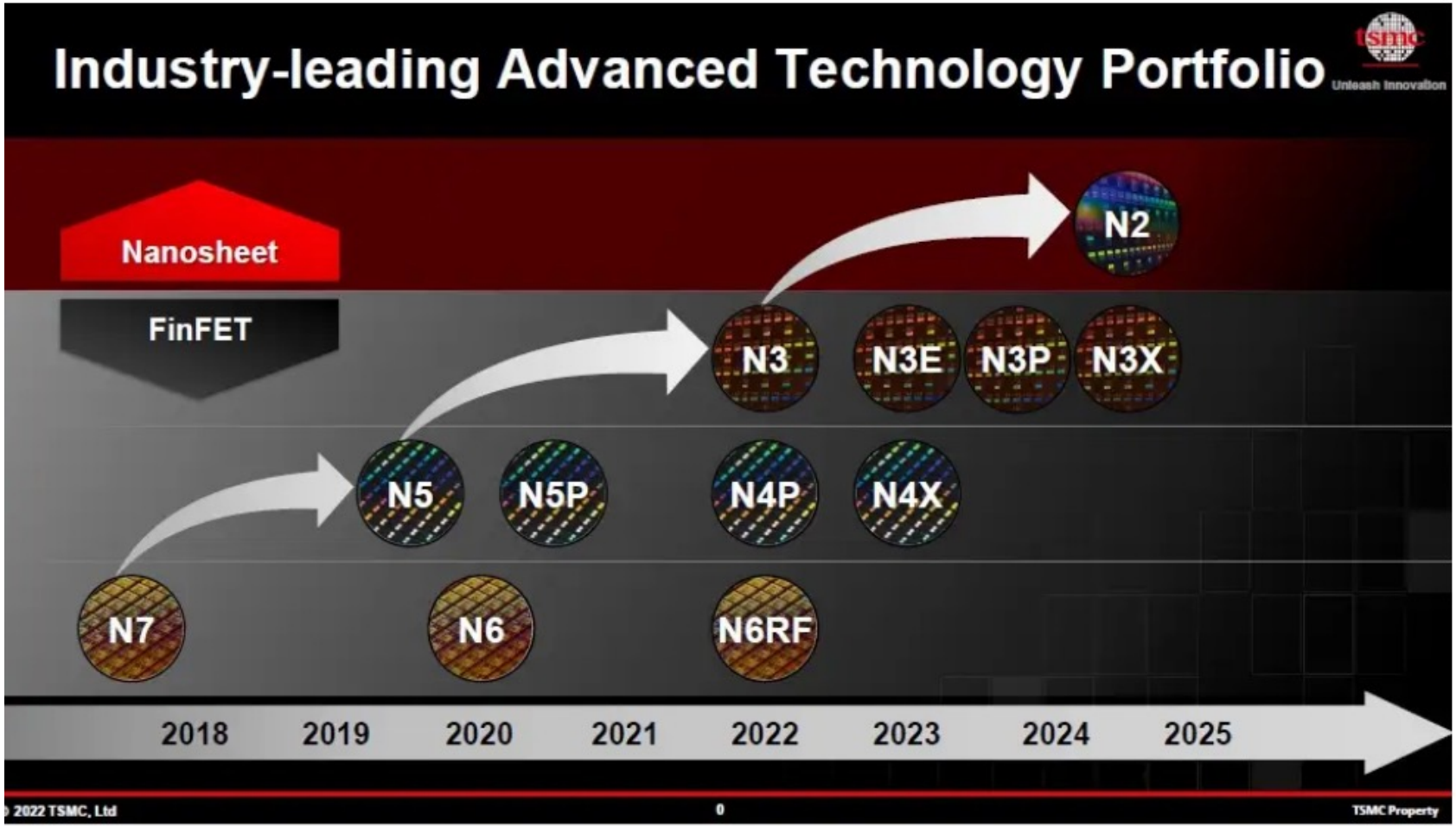

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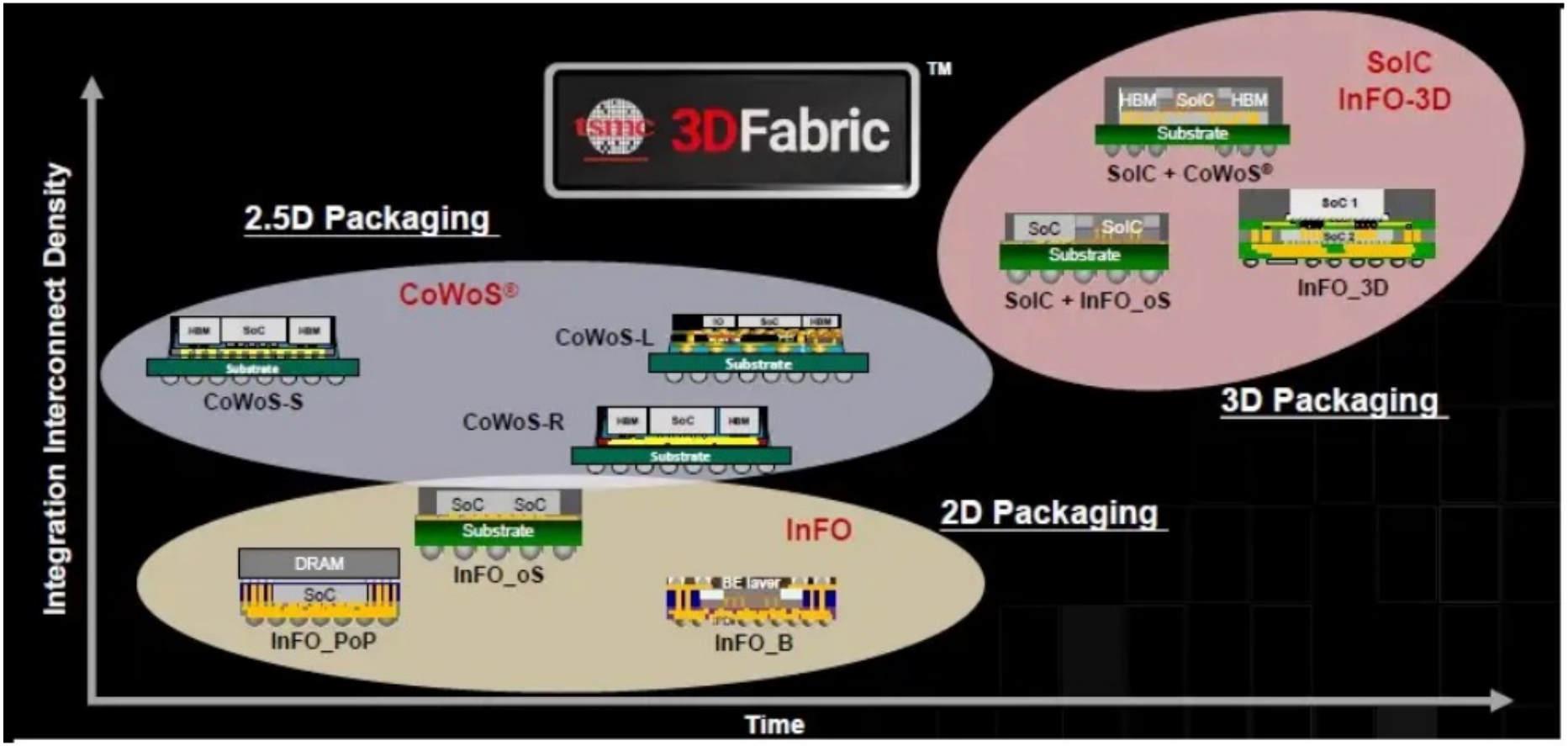

TSMC has merged their 2.5D and 3D packaging offerings into a single brand – “3D Fabric”. The expectations are that there will be future customers that pursue both options to provide dense, heterogeneous integration of system-level functionality – e.g., both “front-end” 3D vertical assembly, combined with “back-end” 2.5D integration.

TSMC at VLSI Conf '22

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N5/N4

- in the 3rd year of production, with over 2M wafers shipped, 150 NTOs by year-end 2022
- mobile customers were the first, followed by HPC products
- roadmap includes ongoing N4 process enhancements
- N4P foundation IP is ready, interface IP available in 3Q2022 (to the v1.0 PDK)
- there is an N5HPC variant (not shown in the figure above, ~8% perf improvement, HVM in 2H22)

Node (compared to N5)	N5	N5P	N4P	N4X
Performance	1X	1.05X	1.11X	1.15X
Density	1X	1X	1.06X	1.06X

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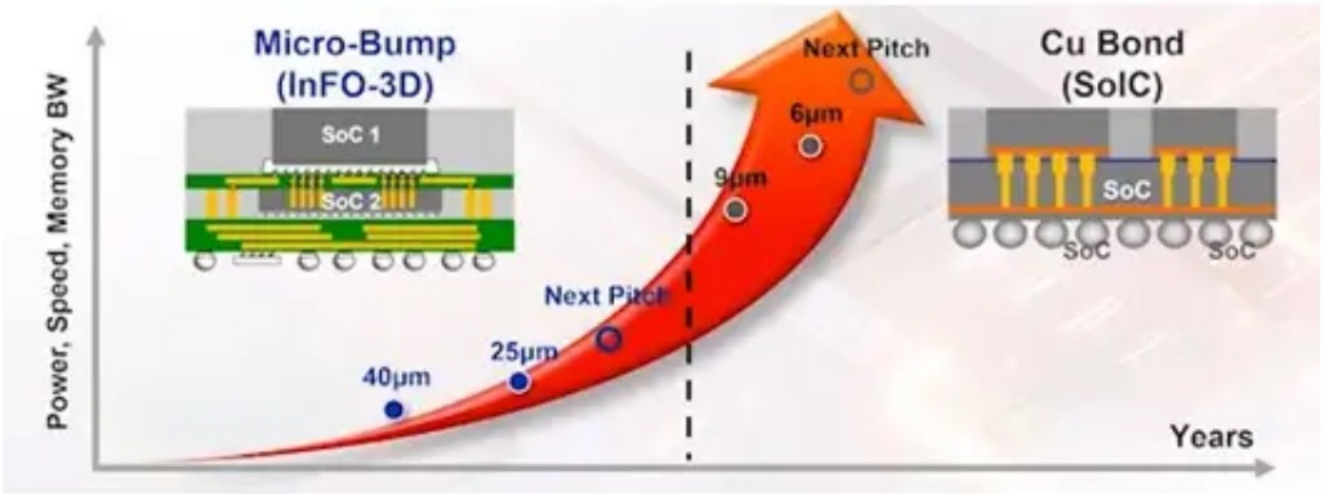
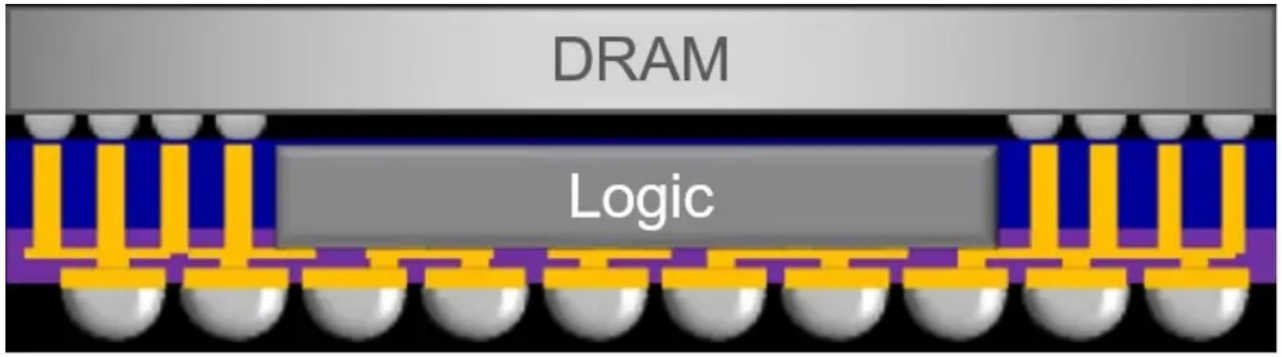
3D packaging



As shown below, InFO_PoP denotes a package-on-package configuration, and is focused on integration of a DRAM package with a base logic die. The bumps on the DRAM top die utilize through-InFO vias (TIV) to reach the redistribution layers.



Foundries

DR JEFF SOFTWARE
INDIE APP DEVELOPER
Jeff Drobman

Samsung

Founded 1938

Samsung in Texas

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Market Chatter: Samsung to Boost Its Semiconductor Investment in Texas to $44 Billion

$44B

08:19 AM EDT, 04/05/2024 (MT Newswires)

Korean electronics giant **Samsung** is planning to increase its semiconductor investment in **Texas** by more than two-fold to **$44 billion**, the Wall Street Journal reported on Friday, citing people familiar with the matter.

The investment will be concentrated in **Taylor, Texas**, where an event to announce the company's increased investment is expected to be held April 15, the report said.

Samsung said in November 2021 that it would invest **$17 billion** to build a semiconductor manufacturing facility in Taylor, Texas. The company said at the time that the facility will manufacture products for application in areas including mobile, 5G, high-performance computing, and artificial intelligence.

Intel vs Samsung

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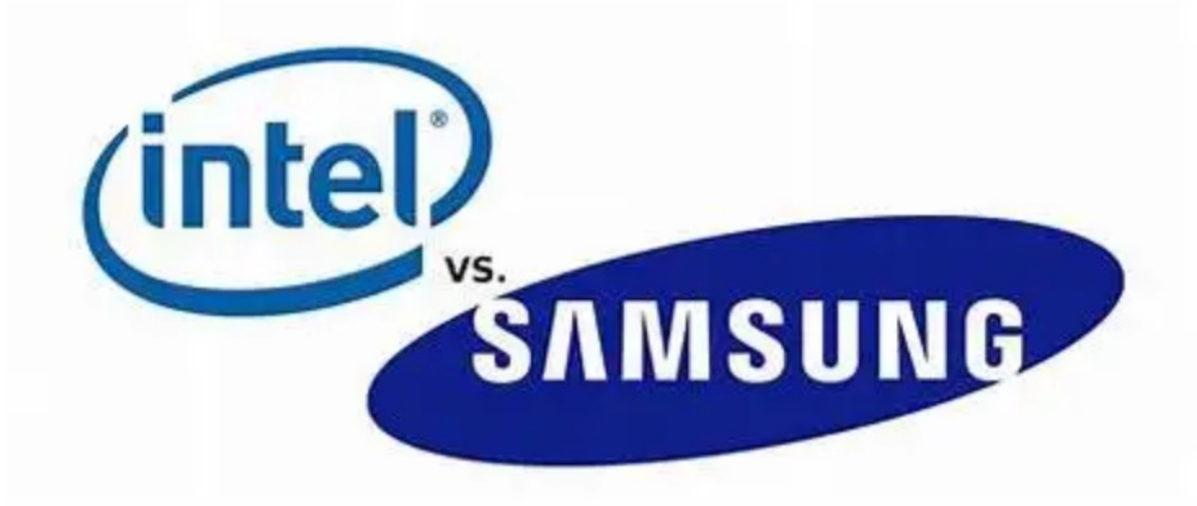
FOUNDRIES

How Intel will Beat Samsung

by Daniel Nenni on 03-09-2022 at 6:00 am
Categories: Foundries
7 Comments



Now that Intel is back in the foundry business, and with the Tower Semiconductor acquisition they are definitely back in the foundry business, Samsung will be the biggest foundry loser here.

You can break the IDM foundry business into two parts: First, and foremost, the NOT TSMC Business. Second is the the Better PPA (Power/Performance, Area) Business.

Samsung 12” Wafers

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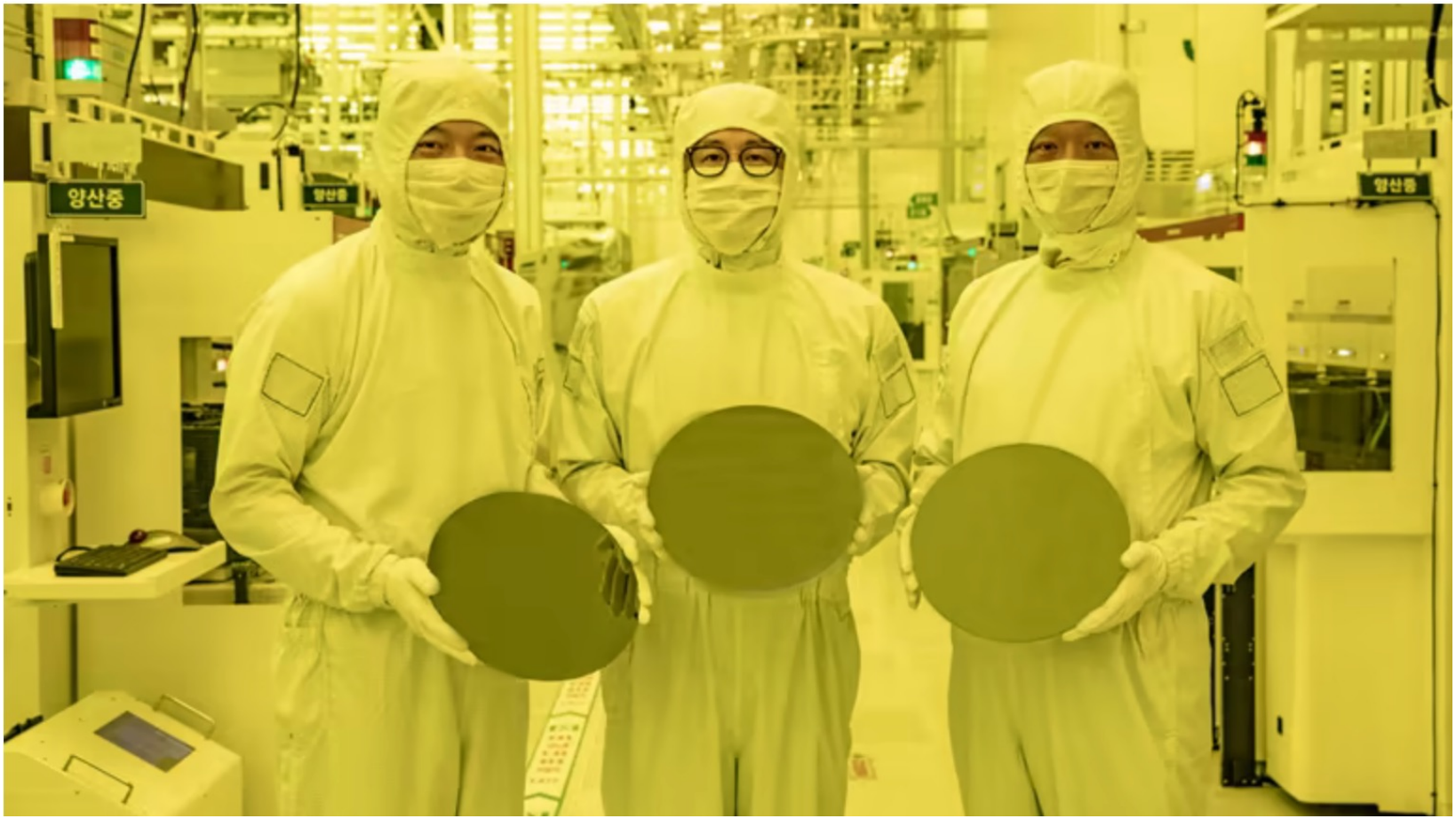

Chip Fabs

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Samsung in Texas

THE VERGE

Samsung is building a new $17 billion advanced chip plant in Texas

Creating 1,800 jobs in the city of Taylor

By Mitchell Clark and Jon Porter | Updated Nov 23, 2021, 6:15pm EST

Samsung Austin Semiconductor — The new plant will be even larger than this | Image: Samsung

Chip Fabs

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THE VERGE

Samsung in Texas

Kinam Kim, the vice chairman and CEO of Samsung Electronics Device Solutions Division says in a statement that "With greater manufacturing capacity, we will be able to better serve the needs of our customers and contribute to the stability of the global semiconductor supply chain." He continued, "In addition to our partners in Texas, we are grateful to the Biden Administration for creating an environment that supports companies like Samsung as we work to expand leading-edge semiconductor manufacturing in the U.S. We also thank the administration and Congress for their bipartisan support to swiftly enact federal incentives for domestic chip production and innovation."

In response, the Biden administration is attempting to bolster US chip production, reducing the potential for supply chain disruption and reversing the country's declining share of manufacturing in recent decades. The Senate recently approved $52 billion in subsidies for new chipmaking plants, though the CHIPS Act is yet to pass in the House of Representatives, according to *Bloomberg*.

Samsung 3nm

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July 2021

Samsung 3nm GAA HVM in 2024?

Samsung Foundry 3nm Gate All Around Process Node, 3GAE, Delayed to 2024

Samsung Foundry 3nm Gate All Around Process Node, 3GAE, Delayed to 2024! This would arrive in a similar time frame to TSMC's denser 2nm GAA technology.Samsung and Intel continue to slip further behind TSMC in leading edge technology. Will they ever be able to catch up?

Samsung Processes

Jeff Drobman

Logic

IC Knowledge

Samsung Keynote at IEDM
by Scotten Jones on 01-27-2022 at 6:00 am

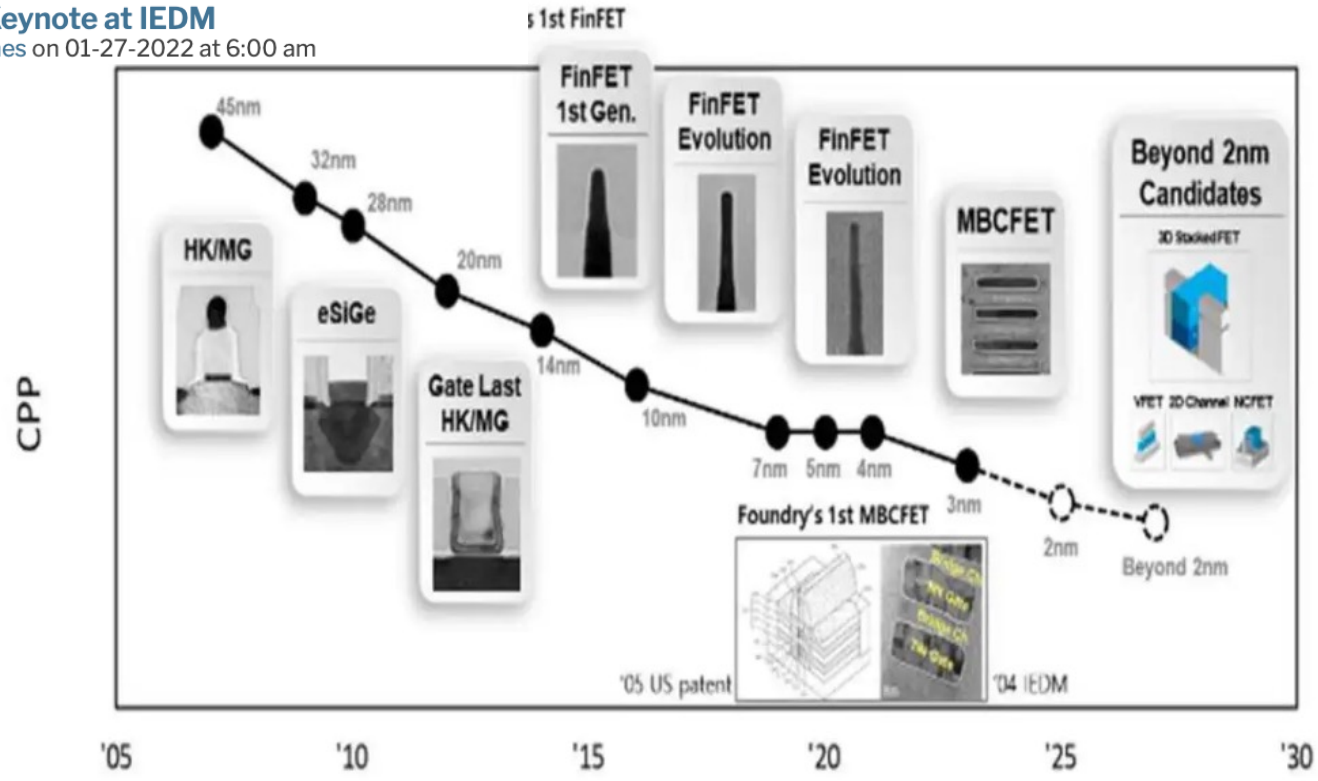

Figure 1. Logic Roadmap.

n figure 1 we can see how the contacted poly pitch (CPP) of logic processes has caled over time. In the planar era we saw high-k metal gate (HKMG) introduced by ntel at 45nm and by the foundries at 28nm as well as innovations like embedded

Samsung DRAM Processes

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IC Knowledge — DRAM

Samsung Keynote at IEDM
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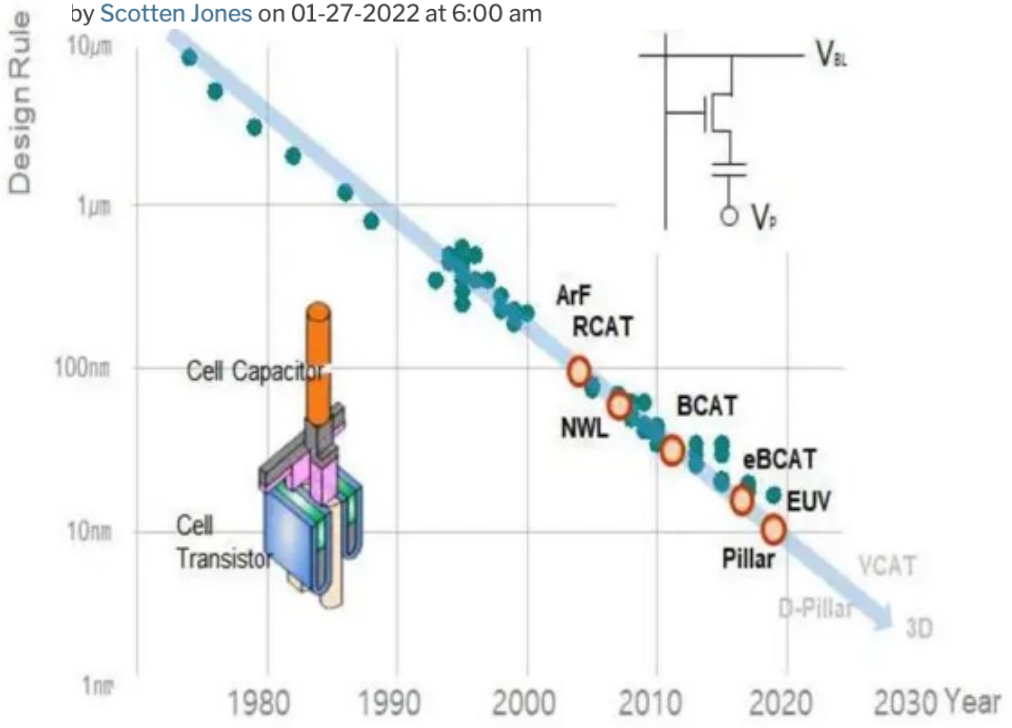

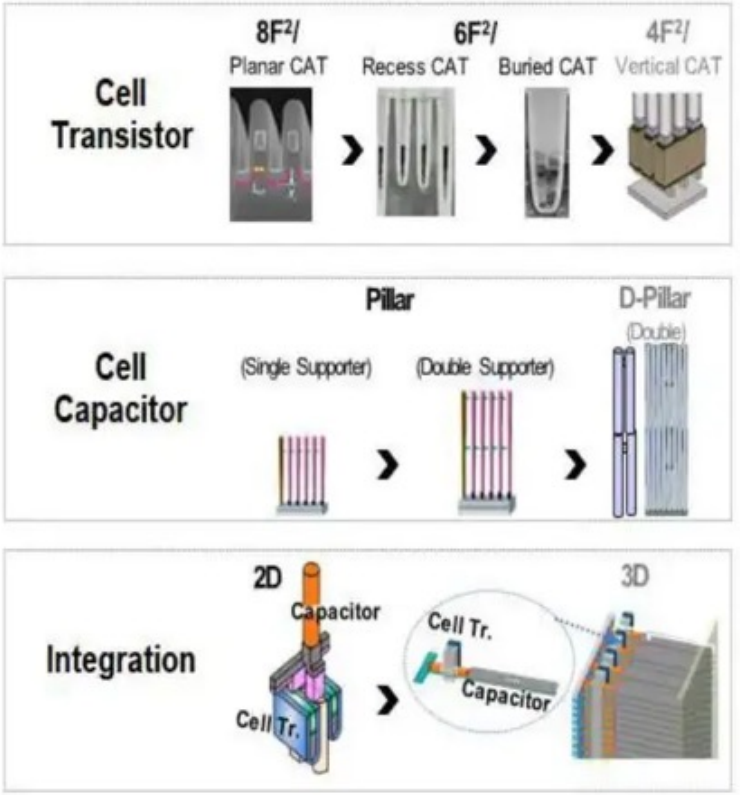

Figure 2 DRAM Roadmap

With EUV already ramping up in DRAM, the next challenges are shrinking the memory cell. Samsung is anticipating staking two layers of capacitors soon. A switch

Samsung NAND Processes

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IC Knowledge

NAND (Flash)

· NAND.

Samsung Keynote at IEDM

by Scotten Jones on 01-27-2022 at 6:00 am

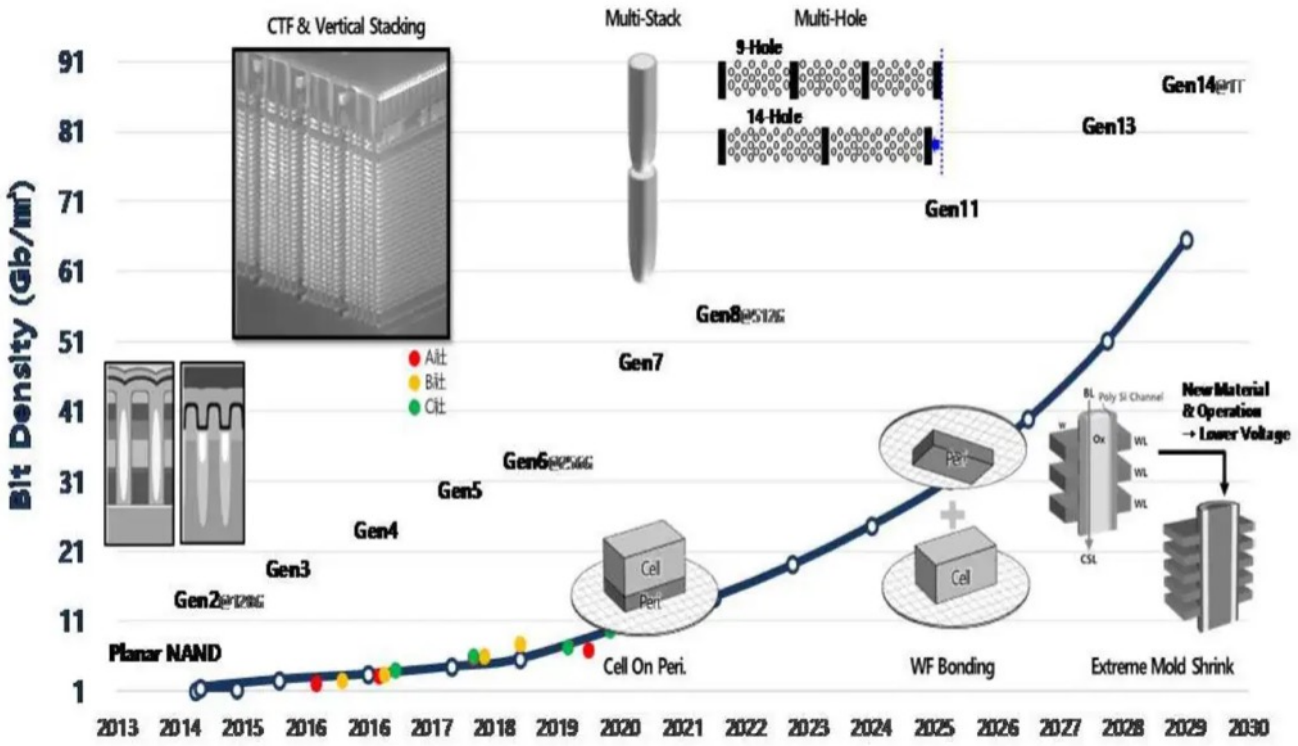

Figure 3 NAND Roadmap

Samsung's latest 3D NAND is a 176-layer process that uses string stacking for the first time (first time string stacking for them, others have been string stacking for multiple generations) and peripheral under the array for the first time (once again the

SemiWiki.com

Via Apple

Fabless: The Transformation of the Semiconductor Industry

Samsung entered the foundry business with Apple 15+ years ago. The first Apple ASIC (iPod) was actually done by fabless ASIC vendor eSilicon and the volumes were drastically underestimated so eSilicon profited greatly. In 2006 Steve Jobs went to Intel CEO Paul Otellini and pitched the iPhone in hopes of getting a manufacturing agreement. Paul did not share Steve's vision and passed on the deal:

"*We ended up not winning it or passing on it, depending on how you want to view it. And the world would have been a lot different if we'd done it. The thing you have to remember is that this was before the iPhone was introduced and no one knew what the iPhone would do. At the end of the day, there was a chip that they were interested in that they wanted to pay a certain price for and not a nickel more and that price was below our forecasted cost. I couldn't see it. It wasn't one of these things you can make up on volume. And in hindsight, the forecasted cost was wrong and the volume was 100x what anyone thought.*"

As a result, not only did Intel miss the mobile market, they missed the opportunity of being a world class foundry like TSMC is today.

SemiWiki.com

Via Apple

Apple then went to Samsung which produced the first A4 SoC for the iPhone 4 using the Samsung 45nm process. The A5 SoC was also 45nm. Back then we named processes different so it was not unusual to reuse a process so all was well and the iPhone dynasty had begun. The A6 was Samsung 32nm and the A7 was Samsung 28nm.

Unfortunately, Samsung showed their true IDM colors by competing directly with Apple and even borrowed some Apple IP. The result was Apple filing more than 50 legal actions around the world which would ultimately be settled for billions of dollars in Apple's favor.

For the A8 (iPhone 6) Apple turned to TSMC 20nm. The iPhone 6 was one of the better smartphones (I had one). Unfortunately, when Apple turned to FinFETs TSMC could not supply enough chips so they also used Samsung 14nm for the A9. Apple was back to TSMC for the A9x and there on after.

SemiWiki.com

Via Apple

Apple absolutely did change the foundry business by writing some really big checks, accounting for 20+% of TSMCs annual revenue, but also for the yearly process cadence. Rather than taking big risky steps TSMC did yearly half nodes matched with the yearly fall iProducts launch. This allowed them to perfect double patterning before adding FinFETs, introduce partial EUV before going to full EUV, and many other process innovations. It's called yield learning for a reason.

Now Samsung and Intel both follow the half node process methodology and you can thank Apple for that, absolutely.

Which brings us back to the recent Samsung missteps. Samsung did VERY well at 14nm getting a piece of the Apple business and many other customers including Qualcomm. Globalfoundries also licensed Samsung 14nm for their Malta fab and has done quite well with it so Samsung 14nm customers are far reaching. Unfortunately, 10nm was not so kind to Samsung with single digit yields at launch time. Samsung was forced to ship good die instead of wafers causing Qualcomm and others to miss market windows and customer commitments.

SemiWiki.com

Via Apple

Samsung did a much better job at 7nm but now we are hearing about a serious unreported yield problem at 5nm. In fact, there is a formal investigation inside Samsung:

"The company's management suspects a forgery of the report on the release of microcircuits by the Samsung Semiconductor Foundry division. Information about the production of 5-, 4- and 3-nm products is now being verified..."

Foundries

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IBM

Founded 1911

IBM $20B

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10-6-22

New Nodes: IBM 2nm

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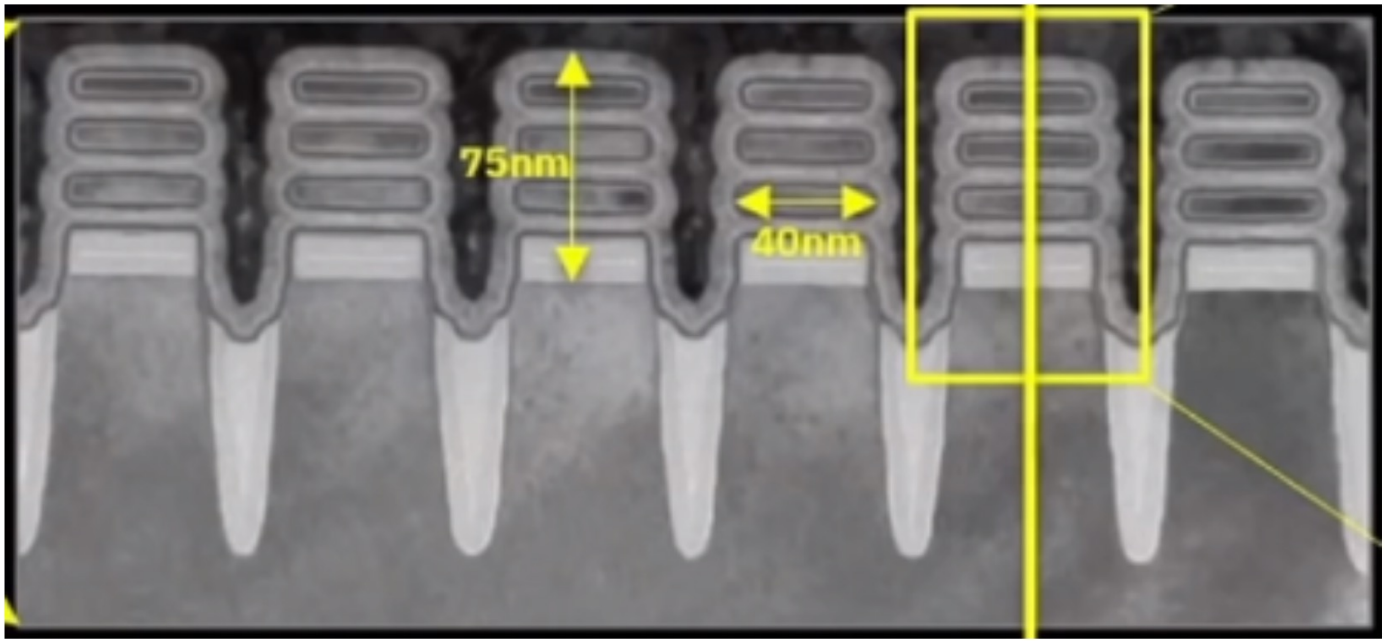

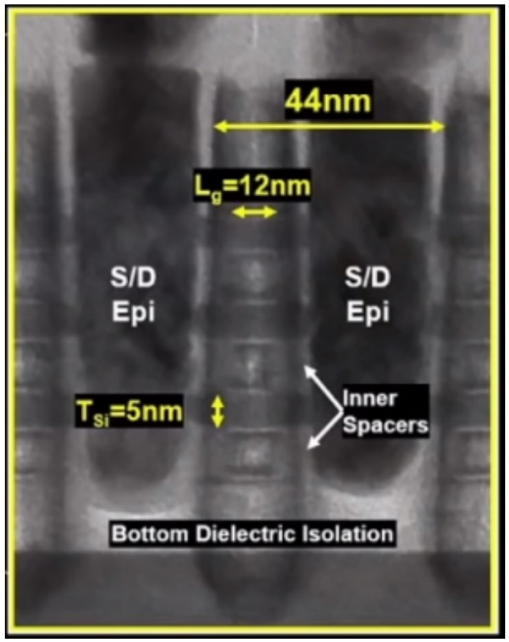

Images of IBMs 2nm Chip architecture

New Processes

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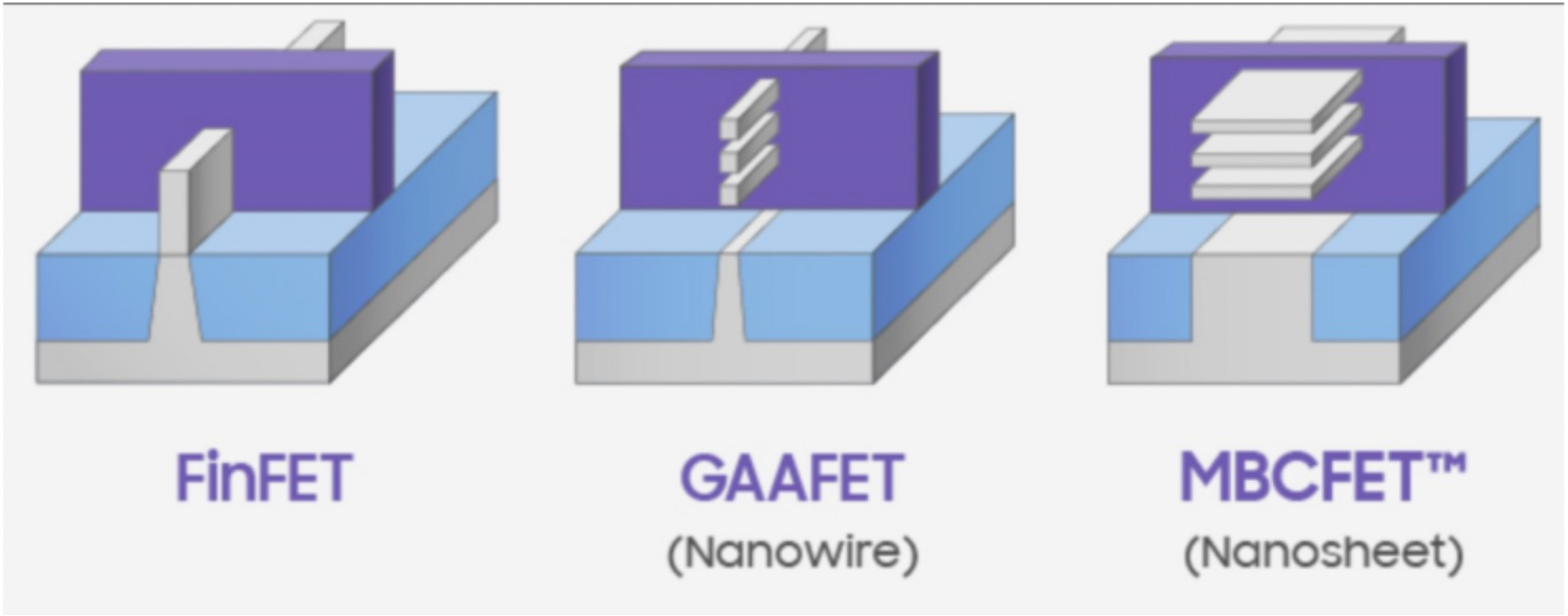

2-3-5-7 nm Comps

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Peak Quoted Transistor Densities (MTr/mm2)				
AnandTech	IBM	TSMC	Intel	Samsung
22nm			16.50	
16nm/14nm		28.88	44.67	33.32
10nm		52.51	100.76	51.82
7nm		91.20	237.18*	95.08
5nm		171.30		
3nm		292.21*		
2nm	333.33			

Data from Wikichip, Different Fabs may have different counting methodologies
*** Estimated Logic Density**

Wikichip

Chips

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China

Process Nodes in China

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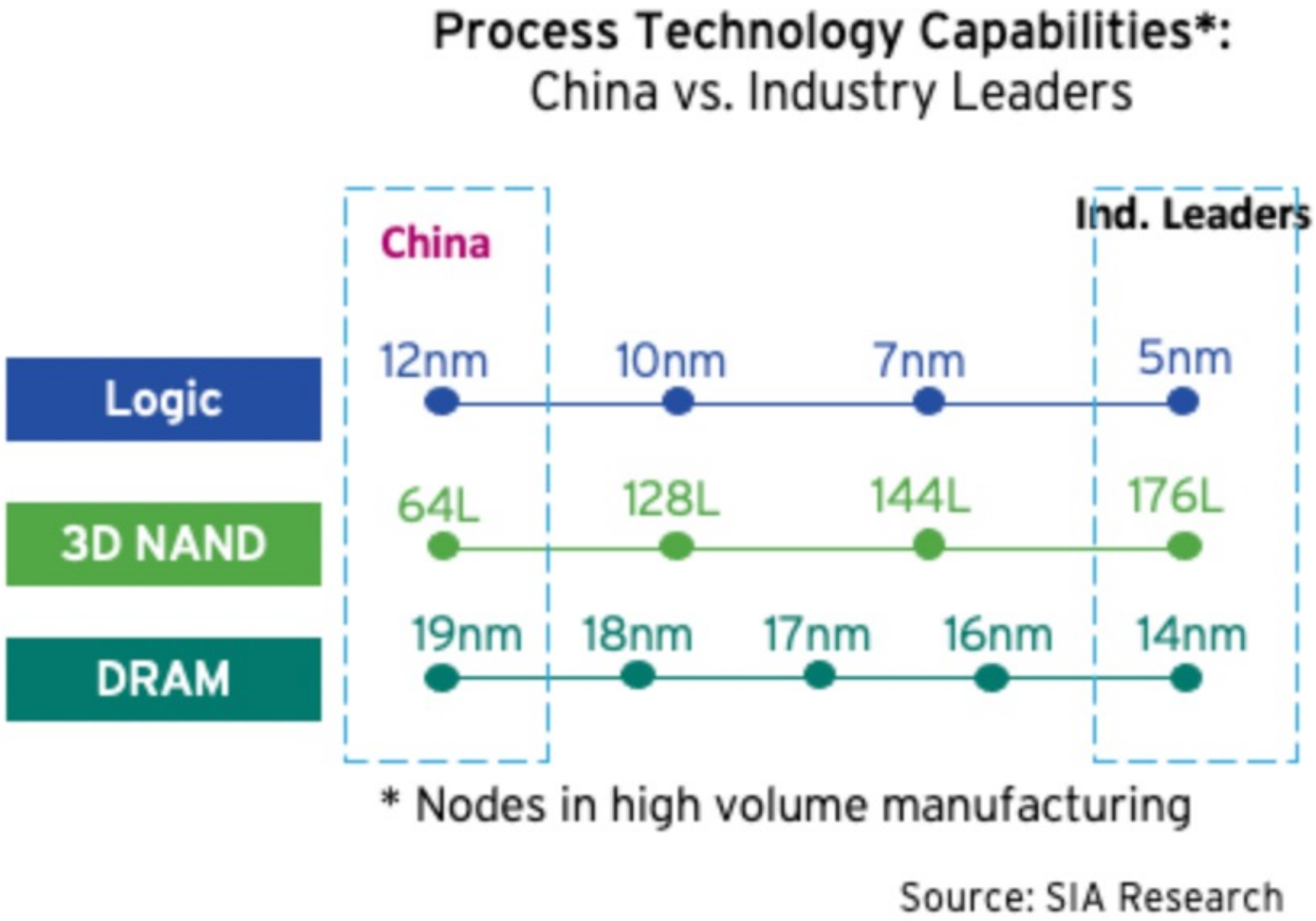

China Chip Segments

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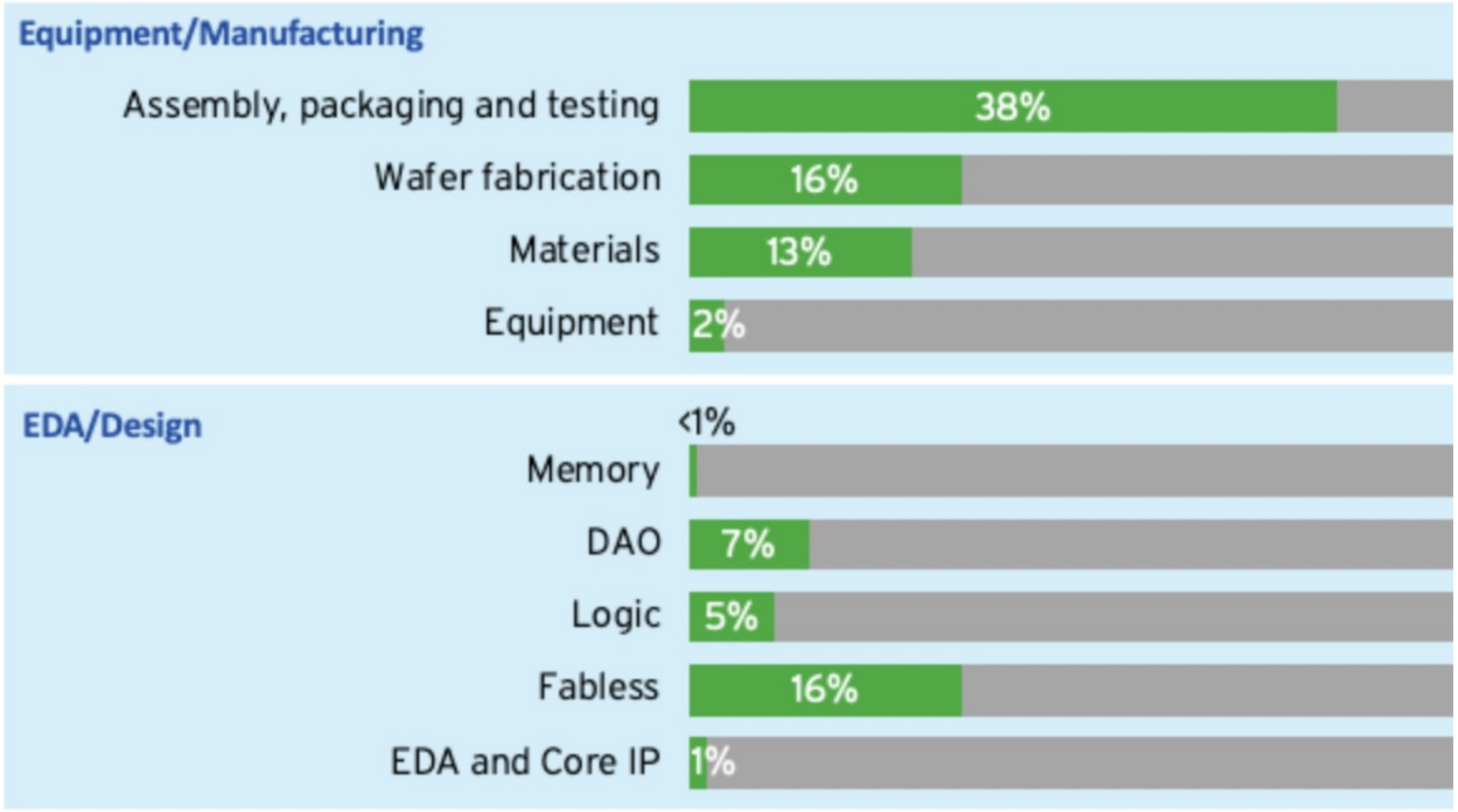
Chinese Share in the Global Semiconductor Supply Chain by Major Segment



Source: BCG x SIA: Strengthening the Global Semiconductor Supply Chain in an Uncertain Era

China Map

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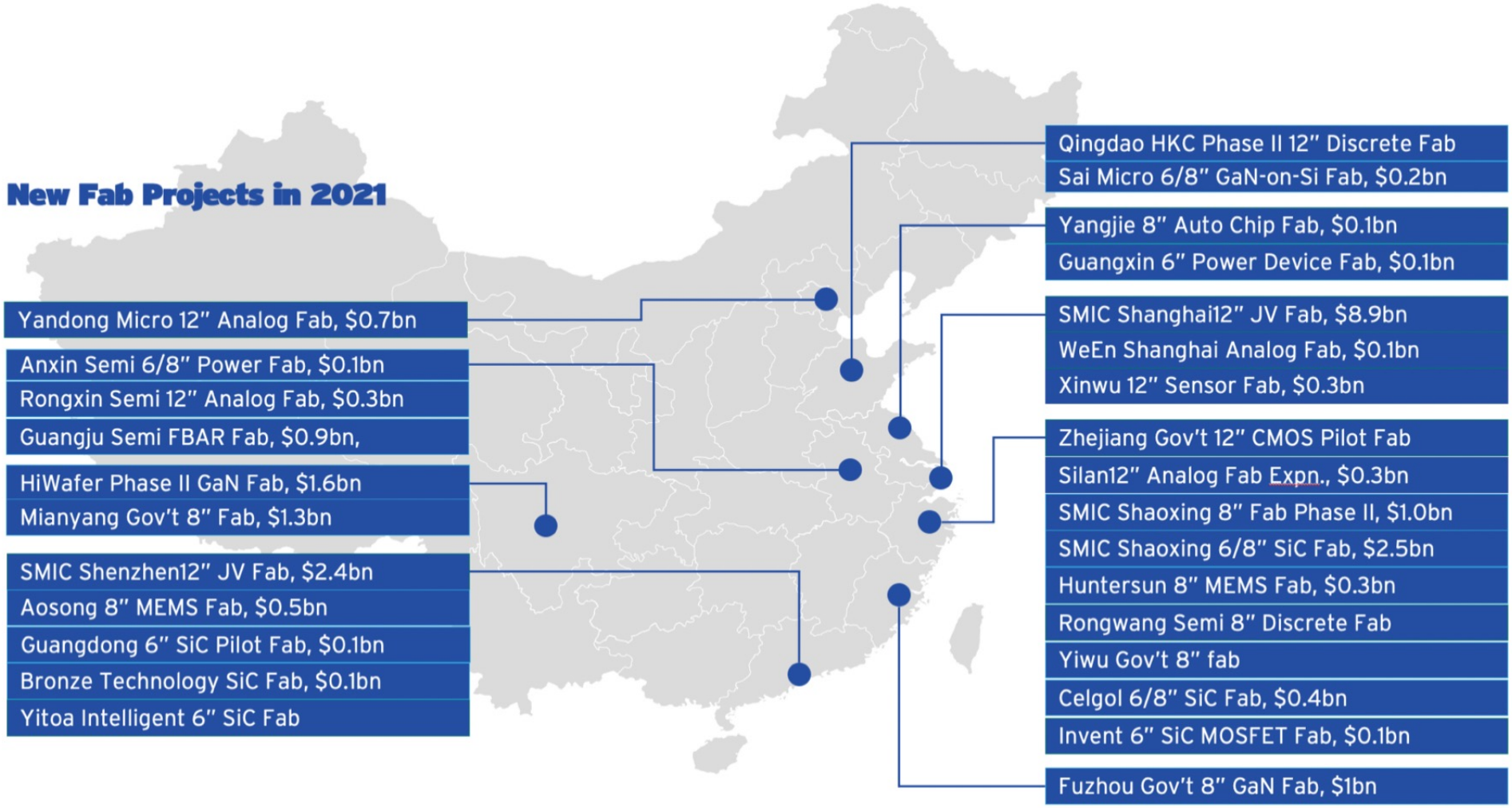
SMIC



Top China Chip Firms

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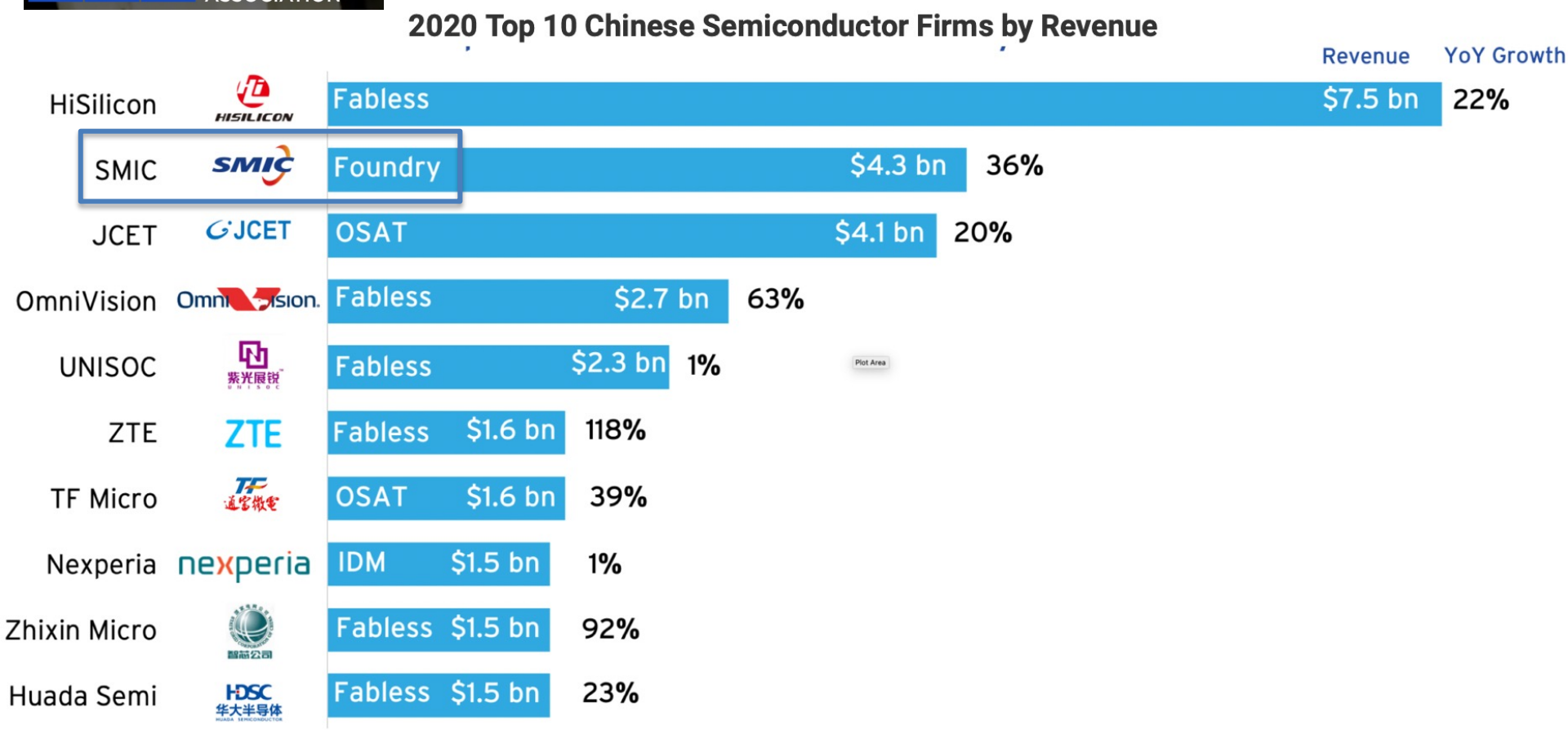

Source: SIA analysis

China OEM's

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Chinese OEMs and Their Commercially Available Chip Products

OEM Vertical	Company	Semiconductor Efforts
Consumer Electronics	mi	• Jun. 2021, recruiting new chip design team • As of Aug. 2021, Xiaomi's VC fund invested in over 60 semiconductor companies
	oppo	• Feb 2020, unveiled "Mariana" chip development plan
	vivo	• Aug. 2021, invested in power semiconductor company
	huami	• Jul. 2021, launched dual-core RISC-V wearable device processor
Home Appliances	KONKA	• Feb. 2020, developed samples of GaN-based MicroLED chip • May. 2020, started memory ATP project
	Galanz	• Jan. 2021, testing RISC-V home appliance chips in foreign markets
	Midea	• Jan. 2021, incorporated semiconductor subsidiaries
	TCL	• Mar. 2021, incorporated two semiconductor subsidiaries
	CHANGHONG 长虹	• Aug. 2020, teams up with HiSilicon on 5G chip development
Internet Cloud Service	Alibaba Group 阿里巴巴集团	• May 2021, launched Xuantie 907 RISC-V processor • Oct. 2021, unveiled 5nm Yitian 710
	Baidu 百度	• Jun. 2021, incorporated chip subsidiary • Aug. 2021, 2nd generation XPU
	ByteDance 字节跳动	• Mar. 2021, developing AI and server chips in-house
	Tencent	• Jul. 2021, developing special purpose processors in-house
	美团 Meituan	• Jul. 2021, set up chip subsidiaries • Aug. 2021, invested in chip IDM
Telecom and Network Equipment	HUAWEI	• As of Aug. 2021, Hubble Technology invested in 44 companies in semiconductor supply chain
	H3C	• Oct. 2020, launched first switch chip • Apr. 2021, launched first network processor

Source: SIA analysis

China Chip Designers

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Chinese Advanced Logic Chip Tapeouts [6], 2020-2021

Alibaba
- October 2021
- 5nm server CPU
- 7nm could AI chip

Baidu
- August 2021
- 7nm cloud server chip

H3C
- April 2021
- 7nm network accelerator

SiEngine
- November 2021
- 7nm autonomous driving SoC

ZTE
- October 2020
- 5nm 5G base station processor

Iluvatar CorX
- March 2021
- 7nm GPU

Horizon Robotics
- August 2021
- 7nm L4 self-driving processor

Cambricon
- January 2021
- 7nm AI accelerator chip

Source: SIA analysis

Foundries

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Wafer Scale

Wafer Scale

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2019

Cerebras Wafer Scale Integration

400,000 cores!

15kW

Startup Cerebras will describe at Hot Chips the world's largest semiconductor device, a 16nm wafer-sized processor array that aims to unseat Nvidia's GPUs dominance in training neural networks. The whopping 46,225mm2 die consumes 15kW, packs 400,000 cores, and is running in a handful of systems with at least one unnamed customer.

...

The Cerebras device packs 84 tiles in a 7x12 array. Each includes about 4,800 cores geared for AI's sparse linear algebra with 48 KBytes SRAM each, their sole memory source.

The Cerebras device packs 84 tiles in a 7x12 array. Each includes about 4,800 cores geared for AI's sparse linear algebra with 48 KBytes SRAM each.

Cerebras WSE 2

Wafer Scale Engine

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--Cerebras Systems

Cerebras Wafer Scale Engine 2

Shift to 7-nanometer process boosts the second-generation chip's transistor count to a mind boggling 2.6-trillion

Almost from the moment Cerebras Systems announced a computer based on the largest single computer chip ever built, the Silicon Valley startup declared its intentions to build an even heftier processor. Today, the company announced that its next-gen chip, the Wafer Scale Engine 2 (WSE 2), will be available in the 3rd quarter of this year. WSE 2 is just as big physically as its predecessor, but it has enormously increased amounts of, well, everything.

...

As big as possible, meaning the size of an entire wafer of silicon (with the round bits cut off), or 46,225 square millimeters.

	WSE 2	WSE	Nvidia A100
Size	46,255 mm^2	46,255 mm^2	826 mm^2
Transistors	2.6 trillion	1.2 trillion	54.2 billion
Cores	850,000	400,000	7,344
On-chip memory	40 gigabytes	18 GB	40 megabytes
Memory bandwidth	20 petabytes/s	9 PB/s	155 GB/s
Fabric bandwidth	220 petabits/s	100 Pb/s	600 gigabytes/s
Fabrication process	7 nm	16 nm	7 nm

UCLA Wafer Scale

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UCLA Samueli School of Engineering

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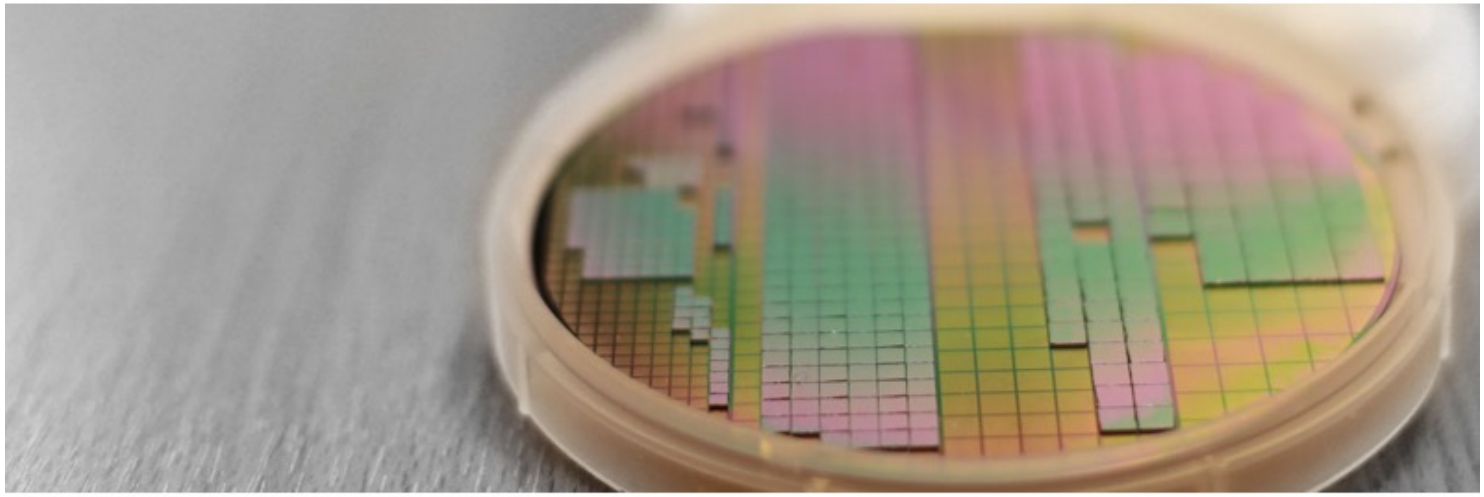
Flextrate

Chiplets?

At Cal State Los Angeles, physiology and neuroscience researcher Selvan Joseph is one such innovator. He's using the Flextrate platform developed at CHIPS to design sensors that can track the physical movements and muscle activity of patients with movement disorders, or those recovering from spinal cord injuries. Flextrate allows him to put these sensors in a small flexible patch that patients can wear unobtrusively on their skin.

"This technology is definitely a game-changer in that you can create devices with more flexibility, pliability and portability," Joseph said. "We can send this device home with our patients and then remote collect data in real time in their day-to-day lives."



Faster Communication

While these platforms have the potential to revolutionize data centers, and consumer and medical electronics, the CHIPS team is also working on ways to make supercomputers and artificial intelligence machines more powerful in the wake of Moore's Law.