Rev 7-14-23

Chips & Wafer Fabs

by
Dr Jeff Drobman
Dr Jeff Software & CSUN

Index

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ISA/SoC Landscape

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CPU & GPU Cores

- MIPS — Focus
- ARM
  - Mobile
    - ❑ **Apple**
    - ❑ Qualcomm
    - ❑ Samsung*
    - ❑ *Google*

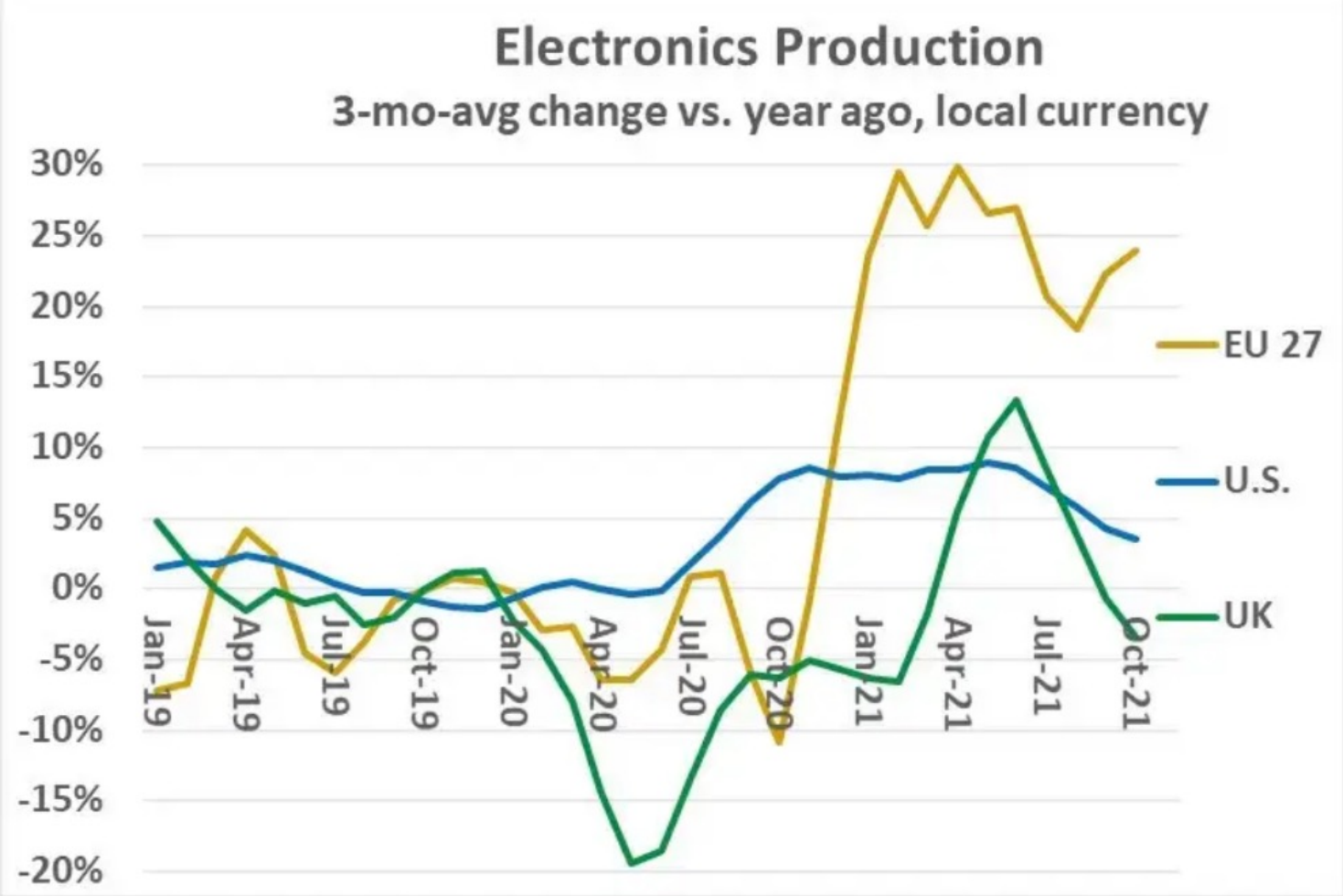
- x86
  - Desktop / Server
    - ❑ Intel*
    - ❑ AMD
- ARM
  - ❑ Apple
  - ❑ *Nvidia*

*has own fab

- iOT
  - ❑ *Amazon*
  - ❑ *Google*
- Cars
  - ❑ *Tesla*

- Foundry (mfr)
  - ❑ TSMC
  - ❑ Samsung
  - ❑ GlobalFoundries (AMD)
  - ❑ Intel (new)

Electronics Industry: US/UK/EU



Electronics Industry: ROW

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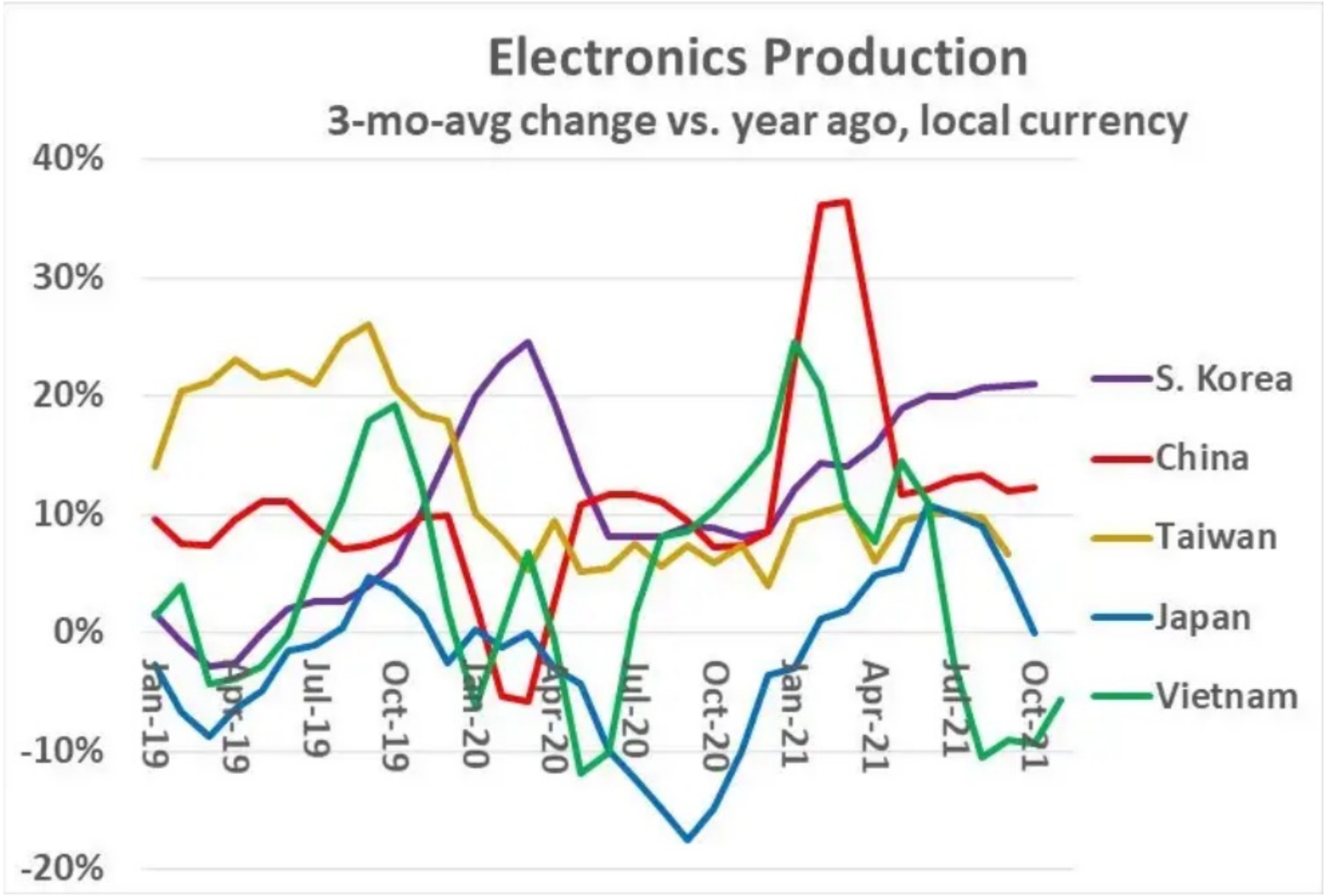

Chips Sales

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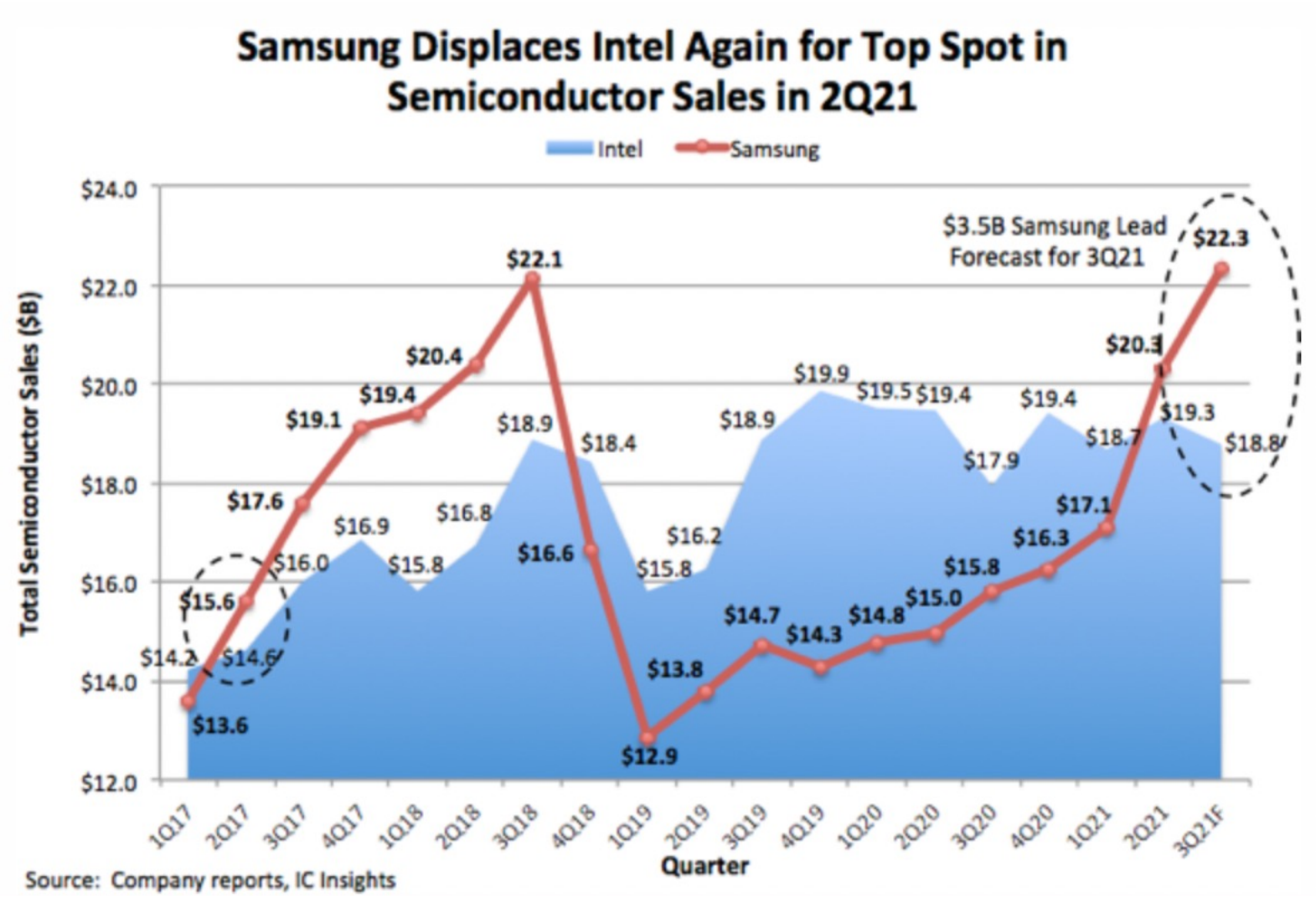

Chips Sales

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2Q21 Top 10 Semiconductor Sales Leaders ($M, Including Foundries)

2Q21 Rank	1Q21 Rank	Company	Headquarters	1Q21 Total IC	1Q21 Total O-S-D	1Q21 Total Semi	2Q21 Total IC	2Q21 Total O-S-D	2Q21 Total Semi	2Q21/1Q21 % Change
1	2	Samsung	South Korea	16,152	920	17,072	19,262	1,035	20,297	19%
2	1	Intel	U.S.	18,676	0	18,676	19,304	0	19,304	3%
3	3	TSMC (1)	Taiwan	12,911	0	12,911	13,315	0	13,315	3%
4	4	SK Hynix	South Korea	7,270	358	7,628	8,762	451	9,213	21%
5	5	Micron	U.S.	6,629	0	6,629	7,681	0	7,681	16%
6	6	Qualcomm (2)	U.S.	6,281	0	6,281	6,472	0	6,472	3%
7	8	Nvidia (2)	U.S.	4,842	0	4,842	5,540	0	5,540	14%
8	7	Broadcom Inc. (2)	U.S.	4,364	485	4,849	4,400	490	4,890	1%
9	10	MediaTek (2)	Taiwan	3,849	0	3,849	4,496	0	4,496	17%
10	9	TI	U.S.	3,793	235	4,028	4,030	269	4,299	7%
—	—	Top-10 Total		84,767	1,998	86,765	93,262	2,245	95,507	10%

(1) Foundry (2) Fabless

Source: Company reports, IC Insights' *Strategic Reviews* database

Top 10 IC Companies

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Table 1: Global Top Ten IC Design Company Revenue Ranking, 1Q22 (Unit: US$1 Million)

1Q22 Rank	1Q21 Rank	Company	1Q22 Revenue	1Q21 Revenue	YoY
1	1	Qualcomm	9,548	6,281	52%
2	2	NVIDIA	7,904	5,173	53%
3	3	Broadcom	6,110	4,849	26%
4	5	AMD	5,887	3,445	71%
5	4	MediaTek	5,007	3,805	32%
6	9	Marvell	1,412	821	72%
7	6	Novatek	1,281	929	38%
8	8	Realtek	1,044	822	27%
9	-	Will Semiconductor	744	815	-9%
10	-	Cirrus Logic	490	294	67%
	7	Xilinx	-	851	-
-	10	Dialog	-	366	-
Total Revenue			39,427	27,342	44%

Notes

1. This top ten ranking only accounts for companies ahead of public financial reporting.
2. Qualcomm revenue only includes QCT; NVDIA excludes OEM/IP revenue; Broadcom revenue only includes semiconductors; Will Semiconductor revenue only includes semiconductor design and sales.
3. NT$:US$ exchange rate: 1Q22 - 28.50:1; 1Q21 - 28.39:1
4. RMB:US$ exchange rate: 1Q22 - 6.336:1; 1Q21 - 6.483:1

Source: TrendForce, Jun. 2022

Top 10 IC Companies

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Leading MPU Suppliers ($B)

2021 Rank	Company	Headquarters	2020	2021	21/20 % Chg	2021 % Marketshare
1	Intel	U.S.	50.6	52.3	3%	50.9%
2	Apple*	U.S.	10.5	13.4	27%	13.0%
3	Qualcomm	U.S.	7.4	9.4	26%	9.1%
4	AMD	U.S.	5.9	9.2	56%	8.9%
5	MediaTek	Taiwan	2.7	4.1	51%	4.0%

*Custom designs for Apple's products that are made by IC foundries.

Source: Company reports, IC Insights

Chips Sales

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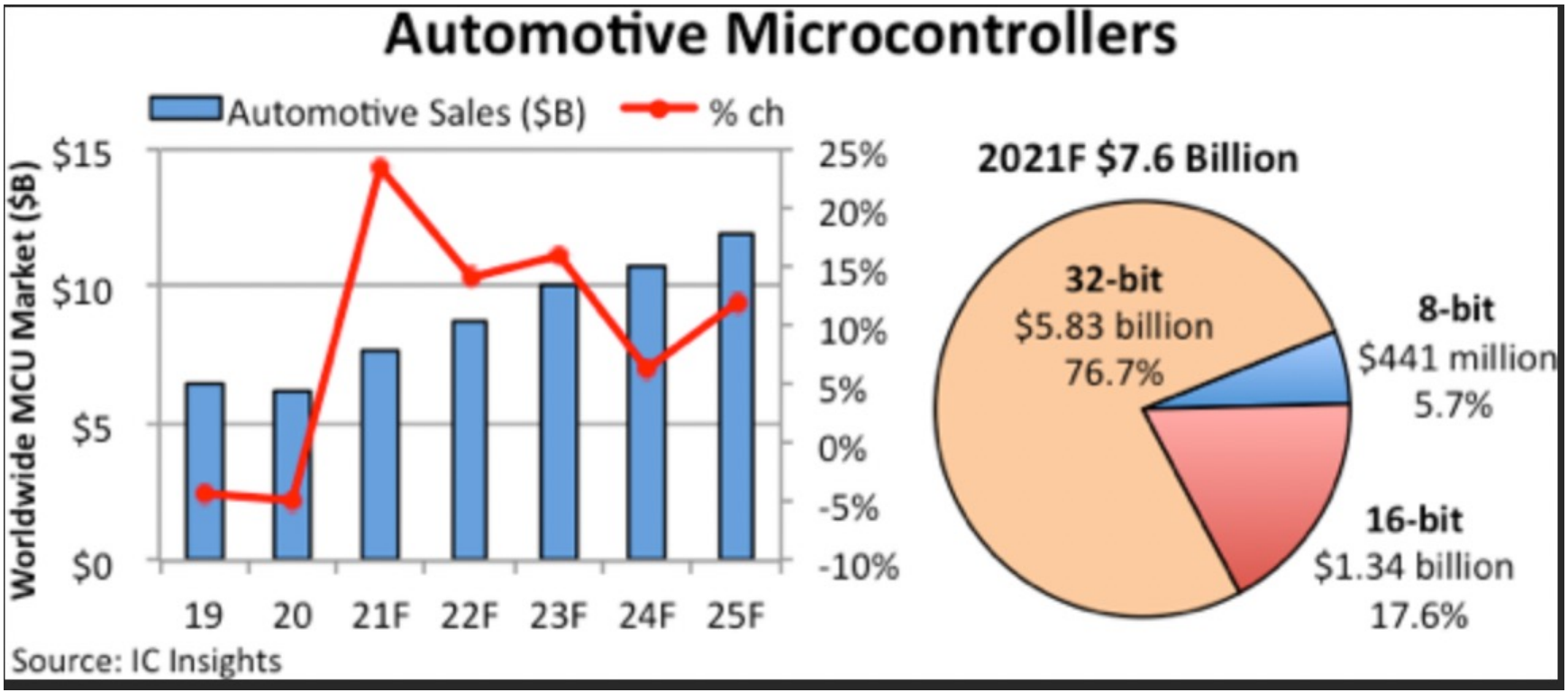

WW Chip Sales

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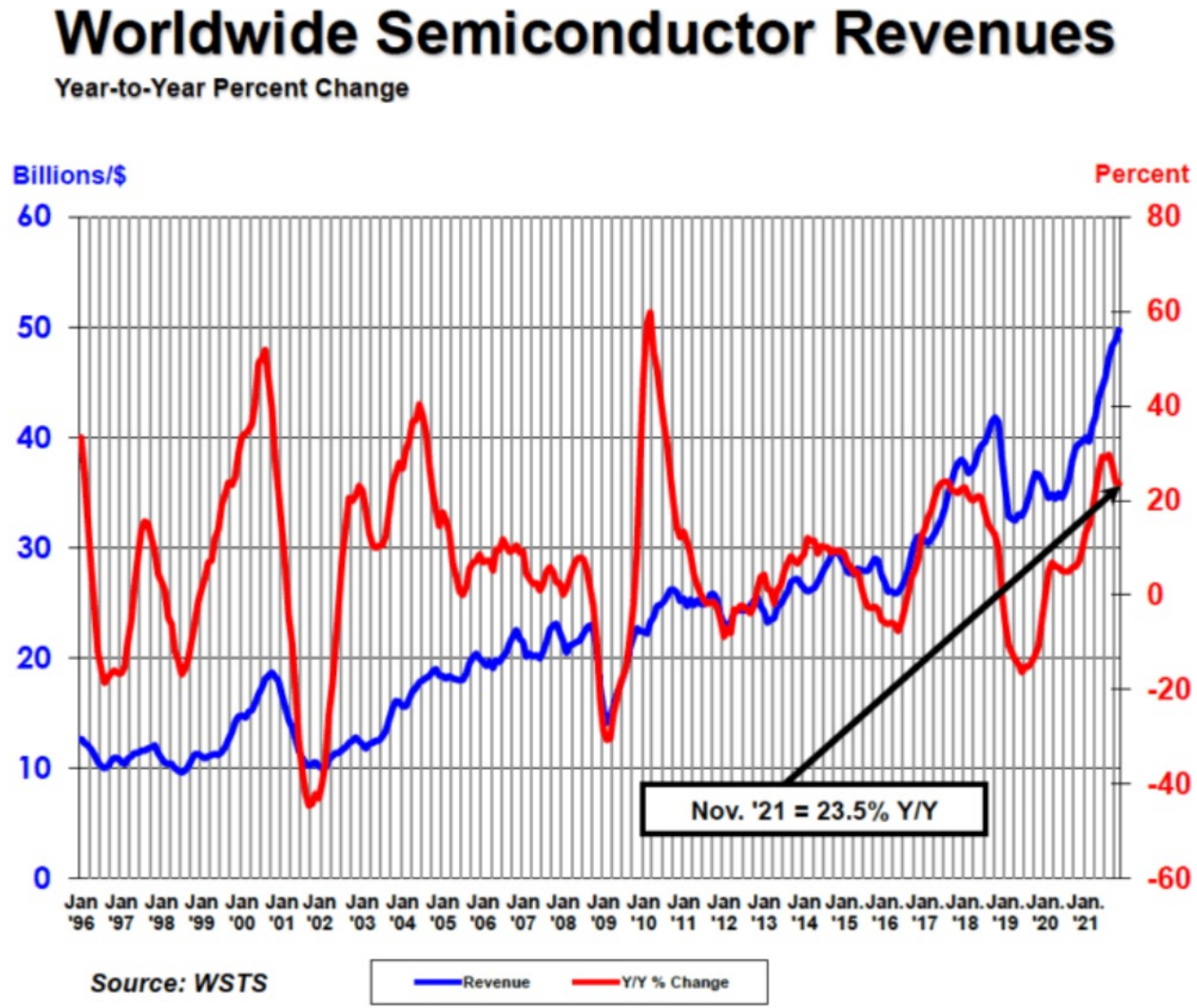
SEMICONDUCTOR INDUSTRY ASSOCIATION



US Chip Industry

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SEMICONDUCTOR INDUSTRY ASSOCIATION

WW Chip Shares

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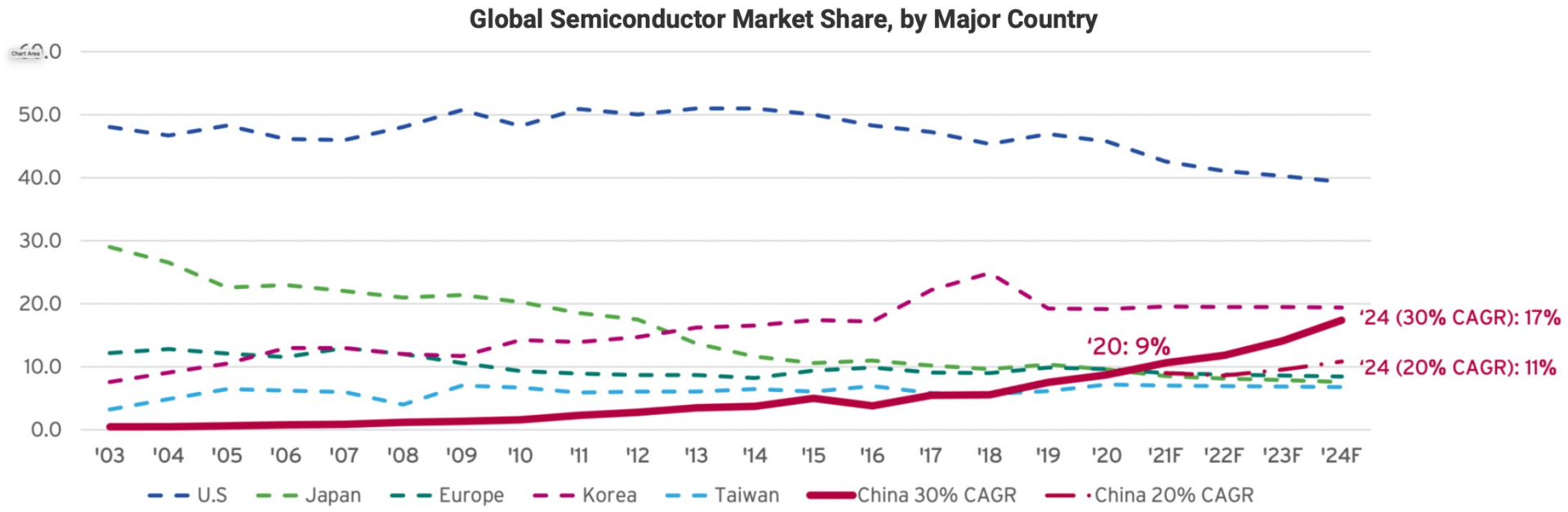
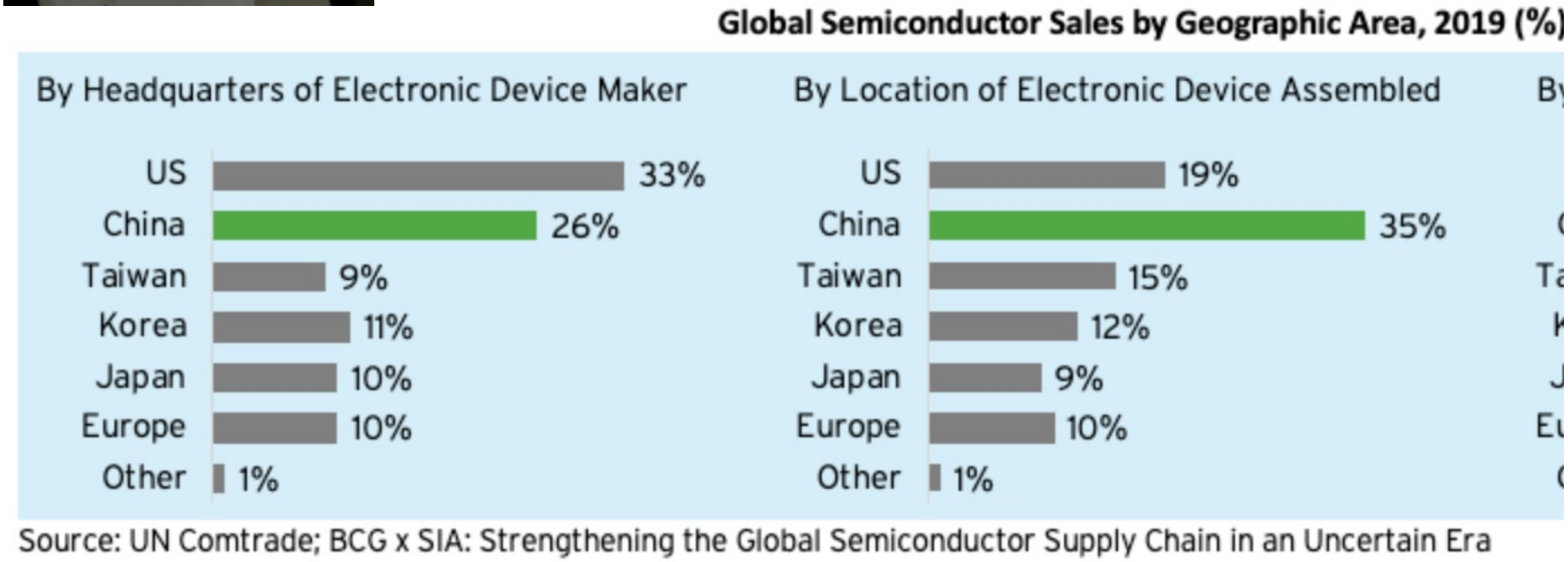


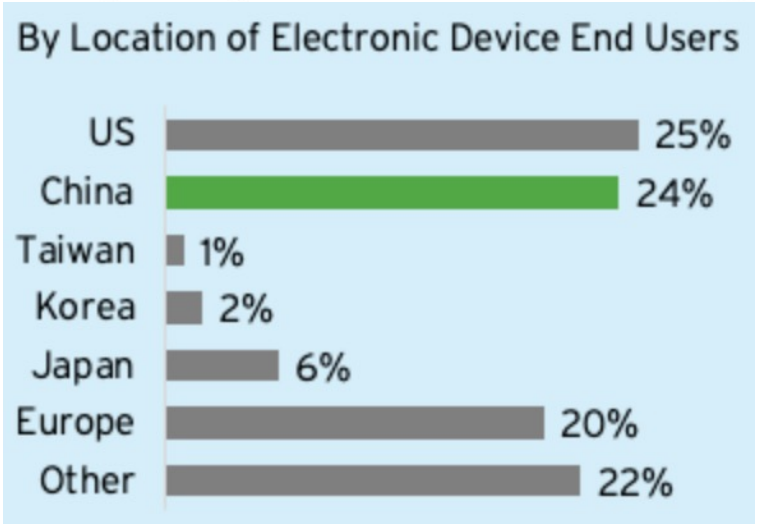
Source: Company financials, SIA analysis, WSTS, Omida

WW Sales by Segment by Area

SEMICONDUCTOR INDUSTRY ASSOCIATION



Source: UN Comtrade; BCG x SIA: Strengthening the Global Semiconductor Supply Chain in an Uncertain Era



SIA Members

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SEMICONDUCTOR INDUSTRY ASSOCIATION

Charter Members

AMD, AMPERE, ANALOG DEVICES, BROADCOM, CIRRUS LOGIC, GlobalFoundries, IBM, intel, LANSDALE Semiconductor Inc., LATTICE SEMICONDUCTOR, Littelfuse, MARVELL, Micron, NVIDIA, onsemi, qorvo, Qualcomm, Rochester Electronics

International Members

ALLEGRO microsystems, arm, infineon, KIOXIA, MEDIATEK, NXP, POLAR semiconductor, SAMSUNG, SK hynix, TOSHIBA, Tower Semiconductor Where Analog and Value Meet, tsmc

IC Technology

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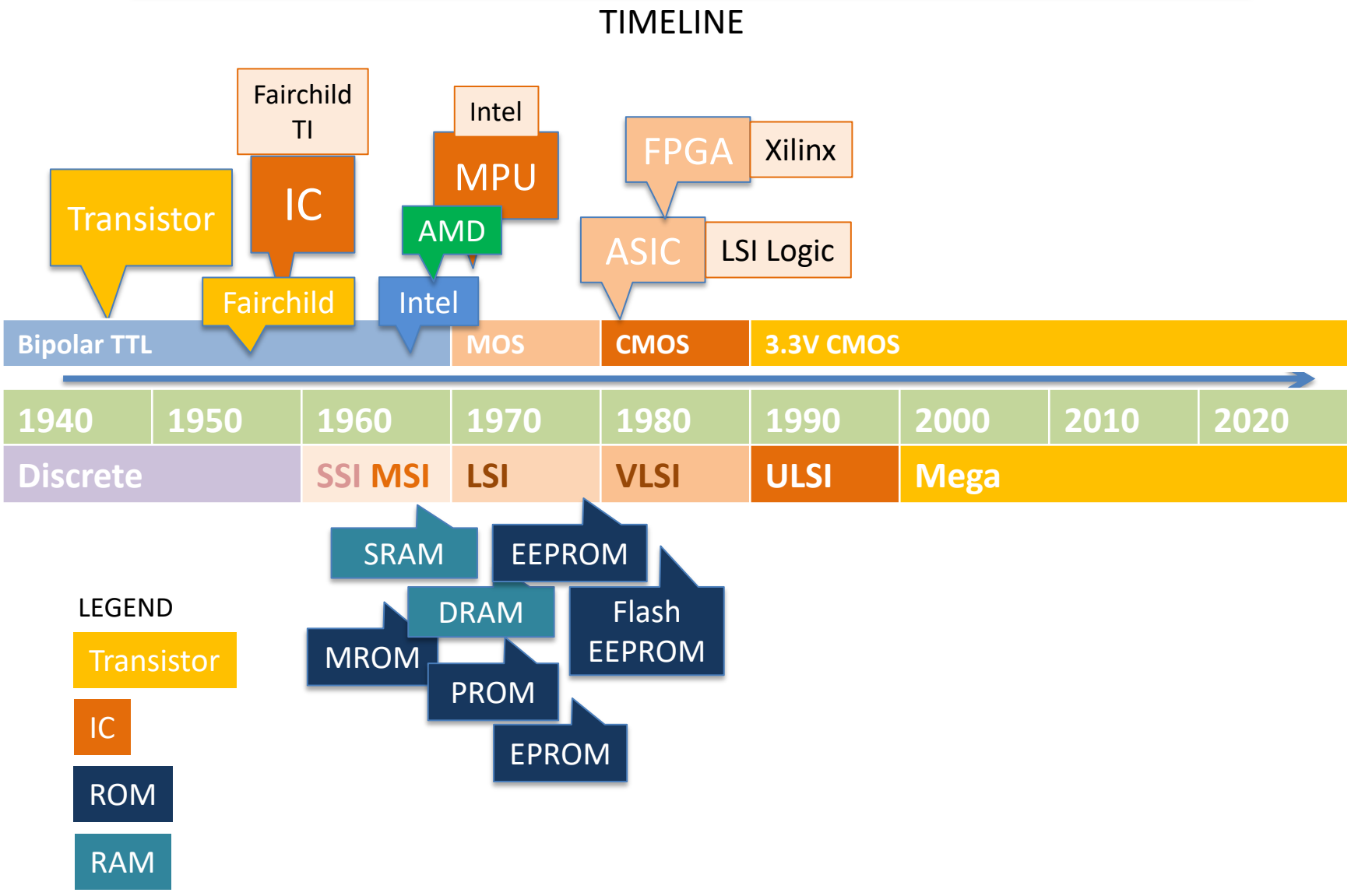

CPU Trends

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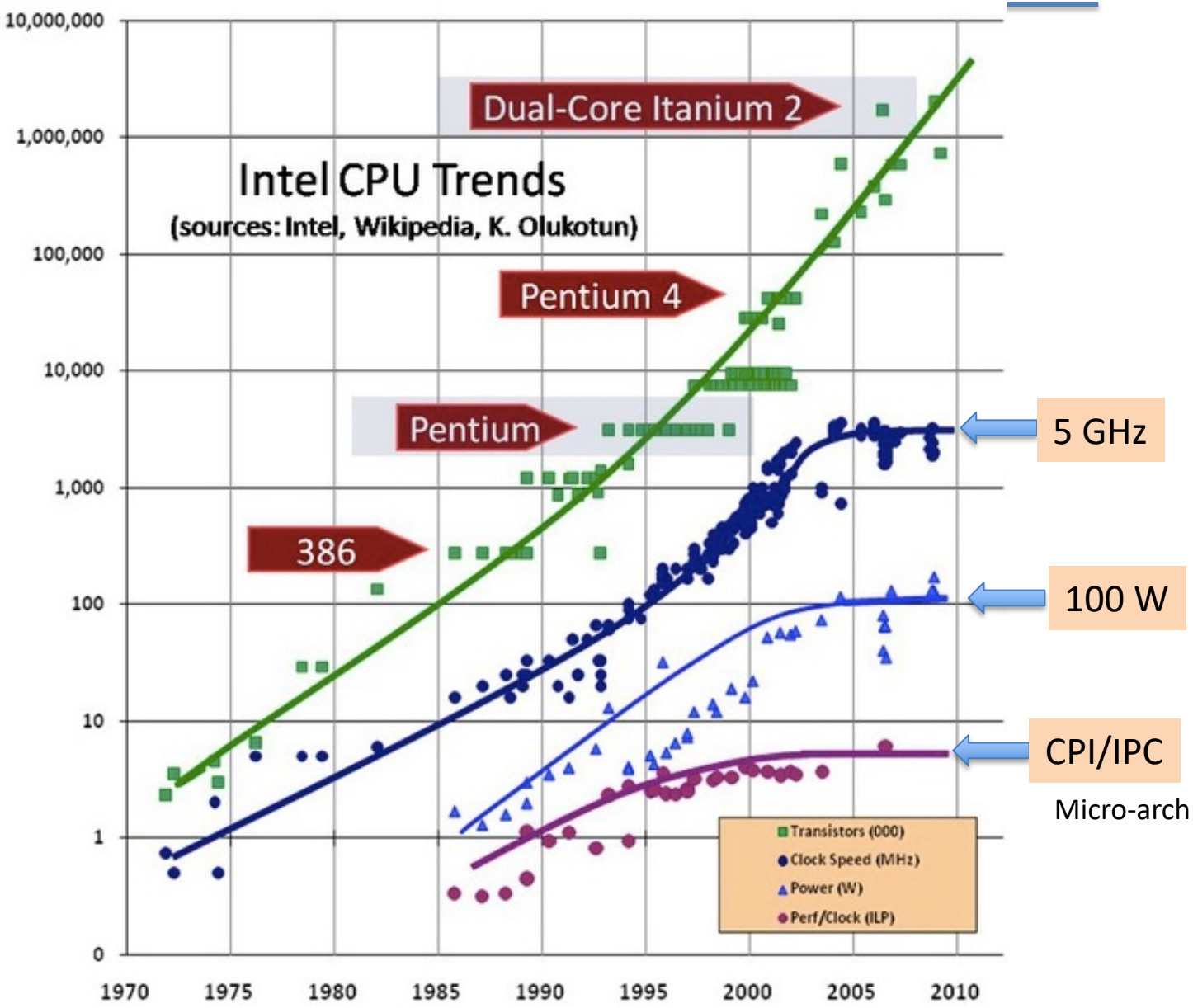
Quora

Steve Baker, Blogger at LetsRunWithIt.com (2013-present)

Answ



Micro-arch

CPU Trends

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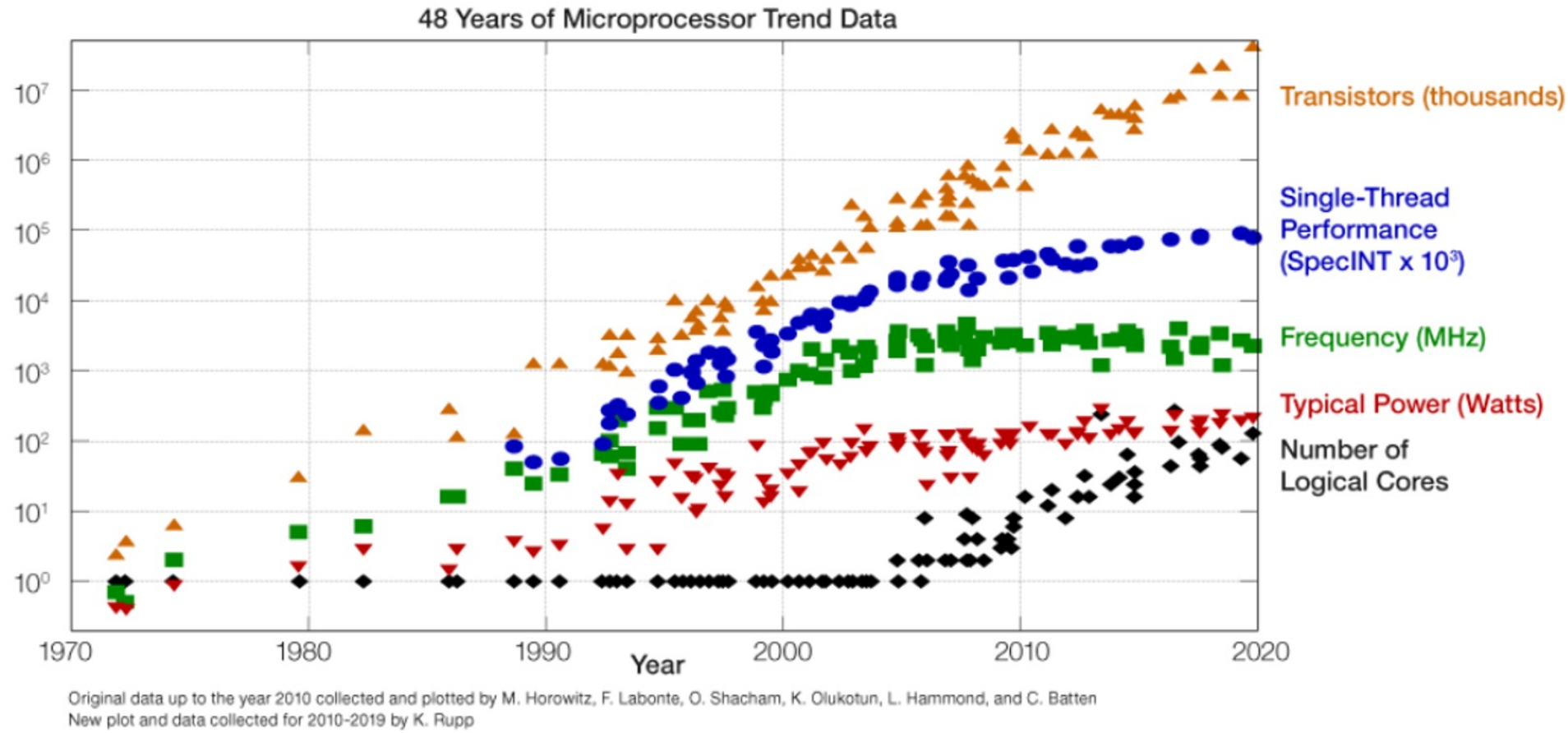

Timeline of CPU Speed

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Multi-Core

MT

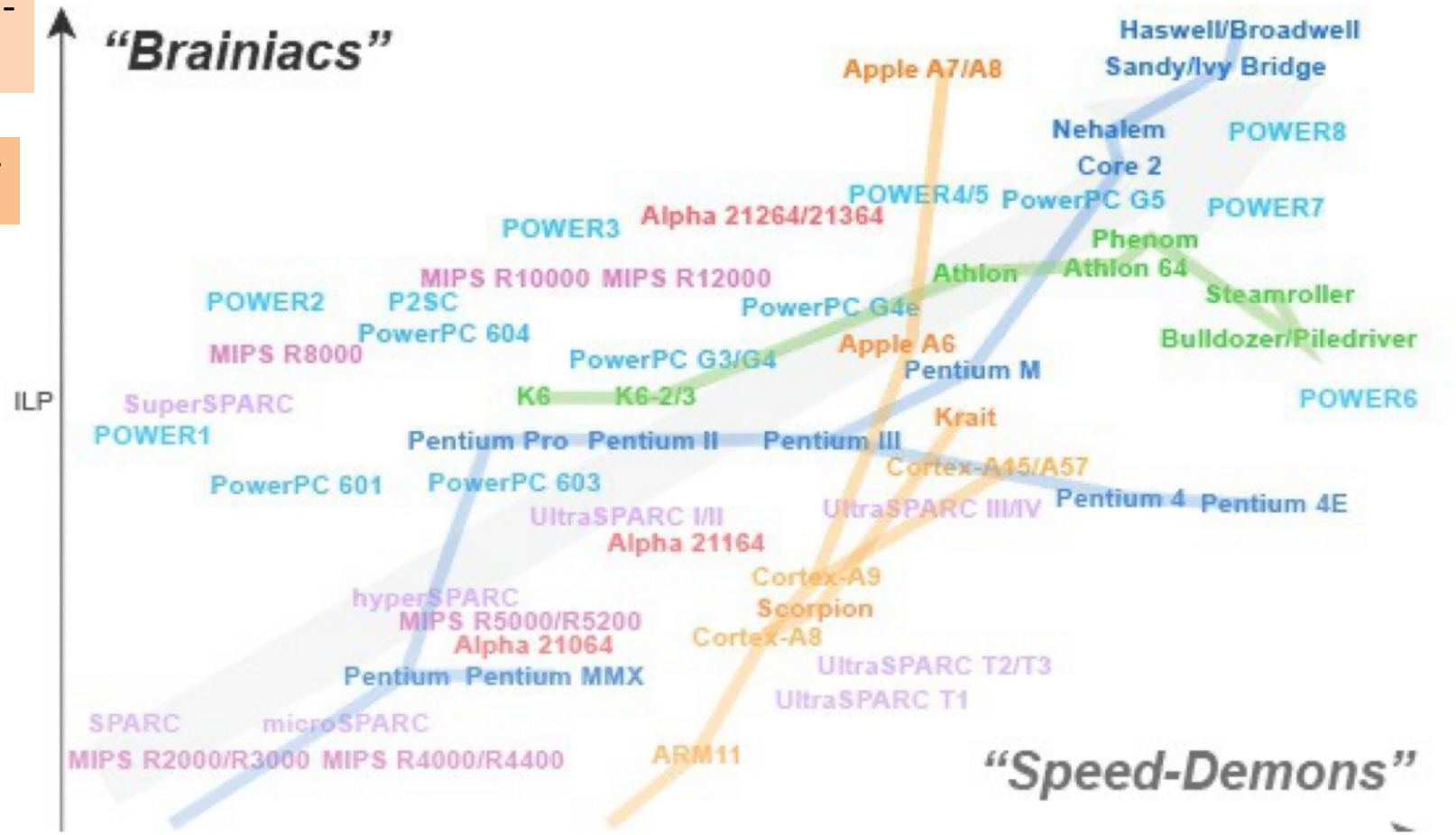

image: CPU Architecture War : Clock Speed v.s. Instruction-Level Parallelism [https://www.linkedin.com/pulse/cpu-architecture-war-clock-speed-vs-instruction-level-hanindhito]

CPU Trends

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Iain McClatchie
design verification on MIPS R8000, helped architect Beast · September 2

In the mid-2000s a bunch of effects simultaneously ended the party.

- Transconductance stopped getting better. Yes, there were still a couple of great tricks that got introduced after that (strained silicon and FinFETs), but the regular improvements ended.
- The delay from transistors finally scaled below the delay from wires, and wires had never been getting better.
- The number of logic stages per clock cycle dropped to about 20 inverter-load-4 delays, and it turns out that getting less than that makes your logic get impractically power hungry really quickly.
- It turned out that people just didn't want CPUs that used more than 100 watts. The business folks realized they were spending more money on the electricity to run the CPU than on the CPU.

Custom SoC's

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Are tech giants, like Tesla, rushing to develop their own semiconductor chips because they do not like having to do things with their hands tied?

Jeff Drobman, Lecturer at California State University, Northridge (2016-present)

Answered just now

Almost all, except Google, license existing CPU and GPU core designs from ARM which are manufactured by TSMC according to their own custom multi-core designs. Apple's SoC's are also based on ARM cores, but were customized by Apple in concert with ARM. Google alone designed their own CPU architecture called Tensor Processing Units.

Apple Event

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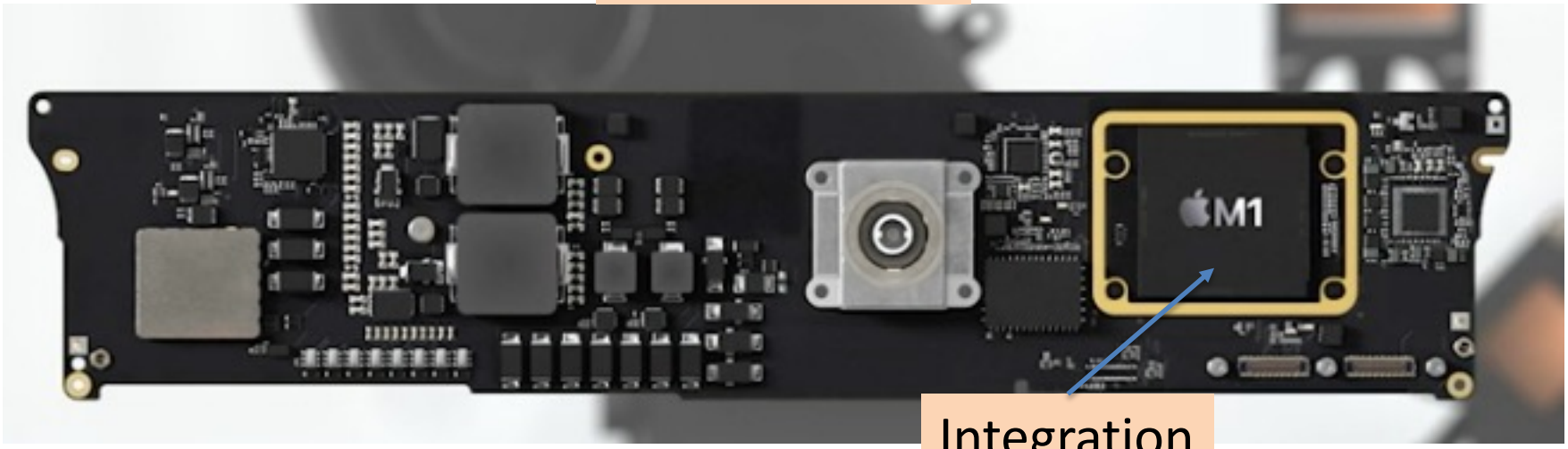
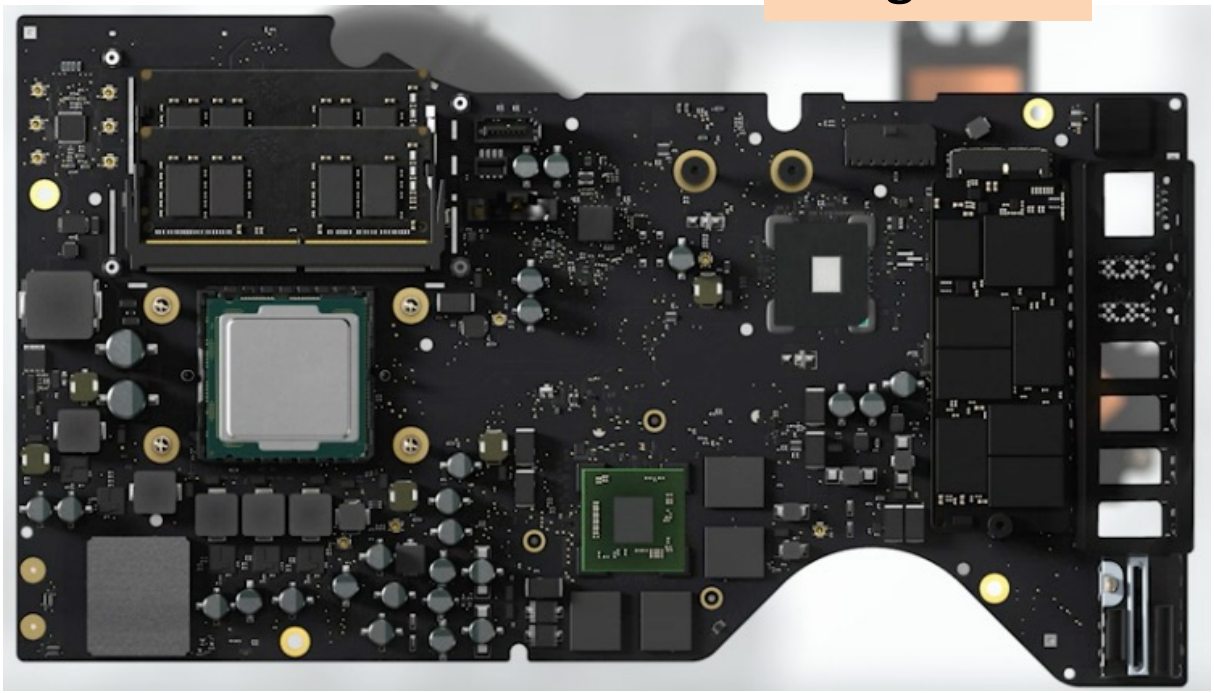
Mac Motherboards



Integration



Tesla SoC

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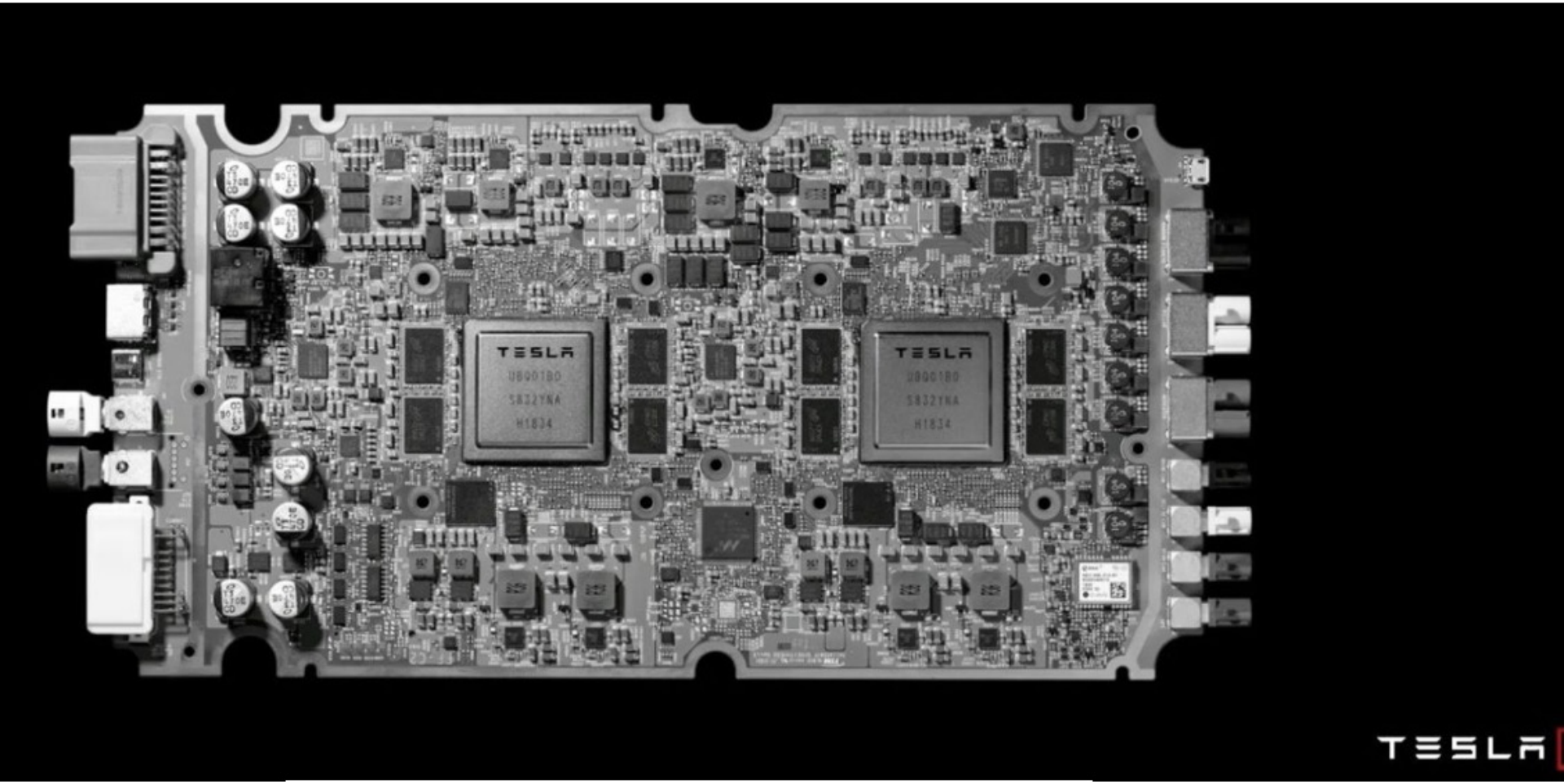

Chips

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Moore's Law

Gordon Moore

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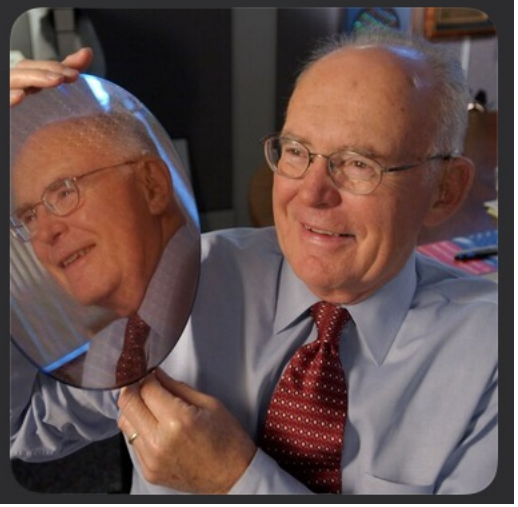
Jan 3, 1929 -- March 24, 2023

News+

Los Angeles Times

Gordon E. Moore, Intel founder and creator of Moore's Law, dies at 94



Gordon Moore

Moore in 1978

Born	Gordon Earle Moore January 3, 1929 Pescadero, California, U.S.[1]
Died	March 24, 2023 (aged 94) Waimea, Hawaii, U.S.
Education	University of California, Berkeley (BS) California Institute of Technology (PhD)

Chips-Moore's Law

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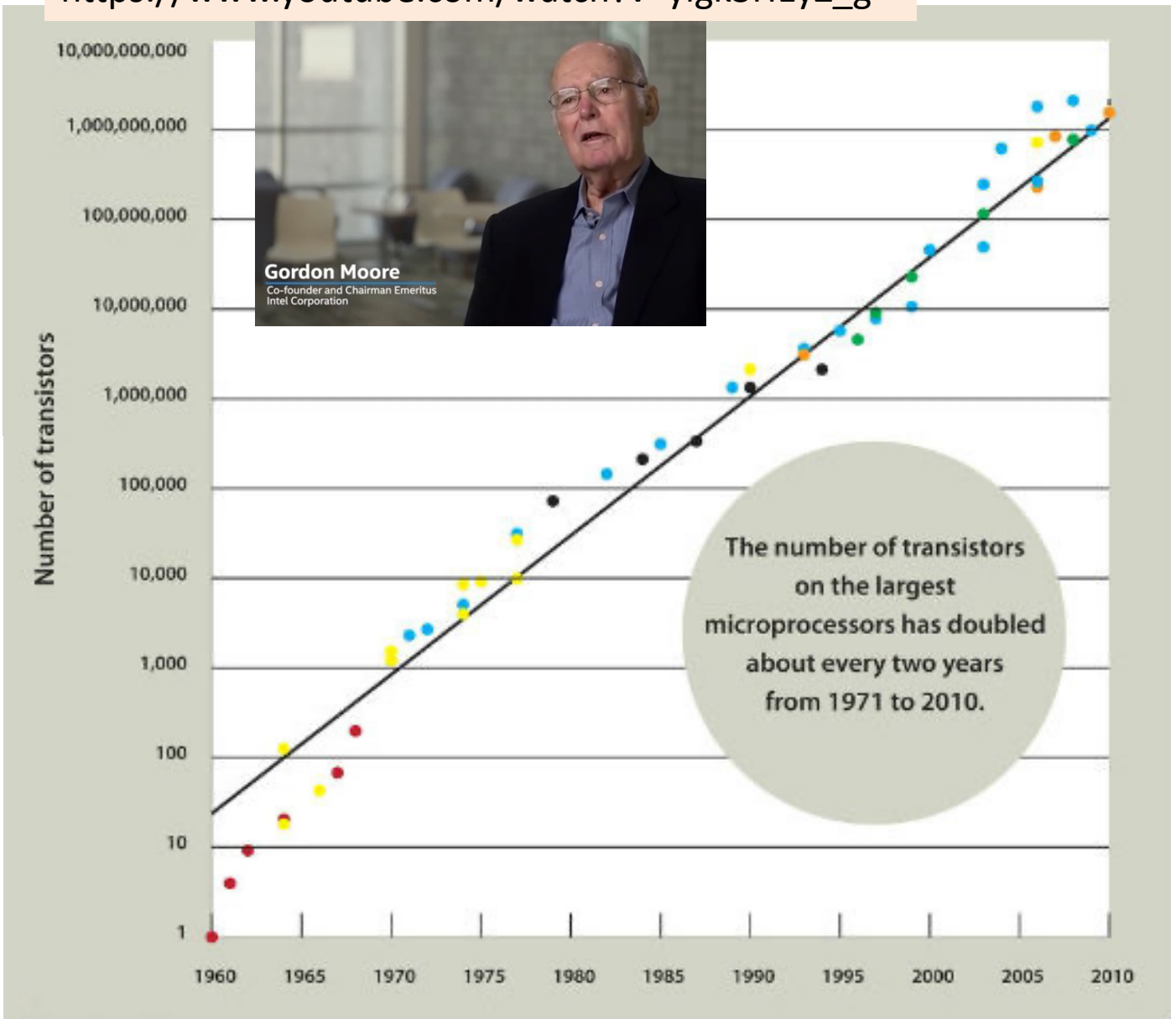
https://www.youtube.com/watch?v=ylgk3HEyZ_g

transistors doubles every 2 years

Plaque to Moore\'s Law at the technology plaza in Mountain View, beneath a model of the Silicon crystal

Dave Laws (2018)



Moore's Law

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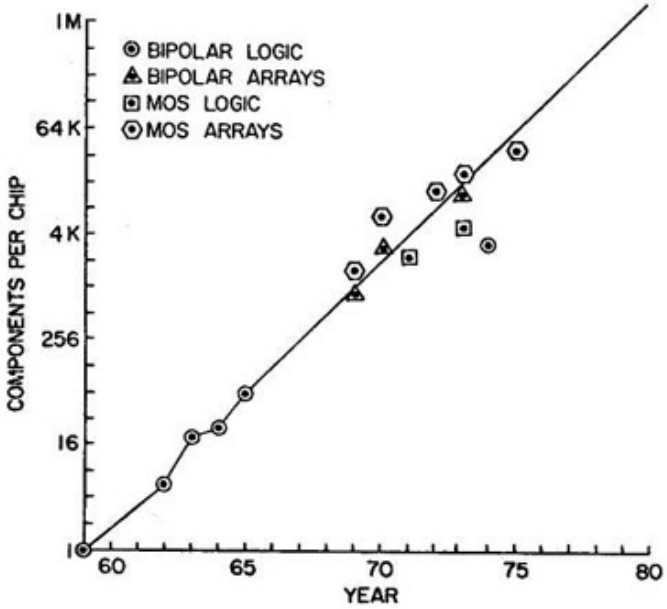
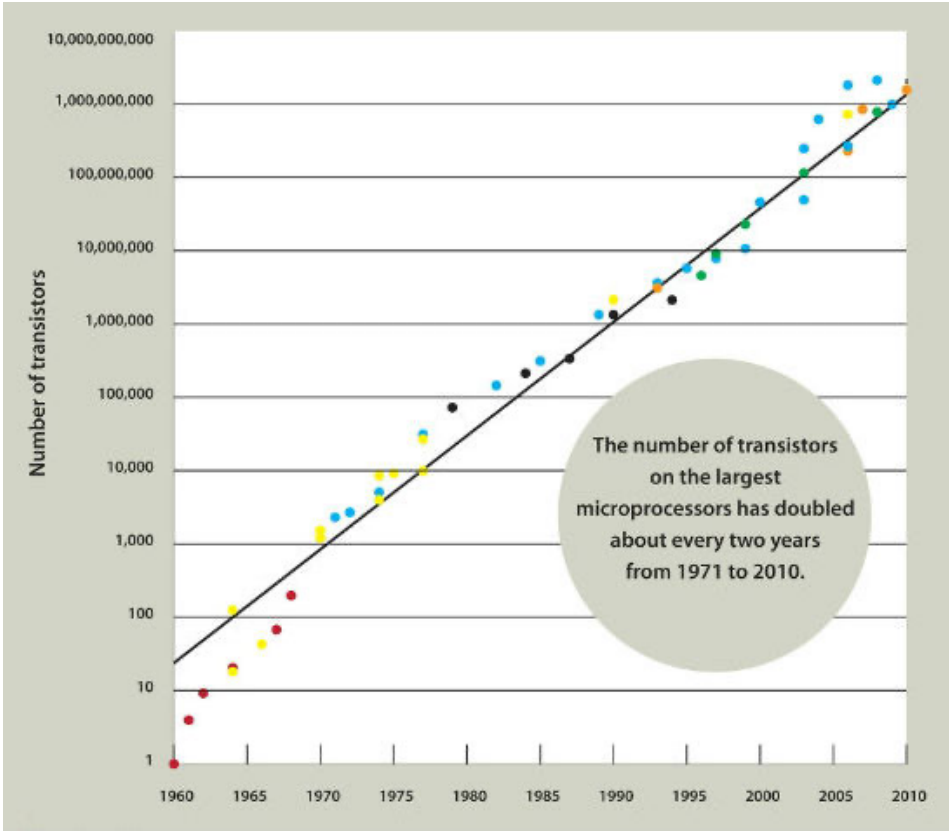
Looking Back

- Original in 1965: # Transistors will double **every year** (12 months)
- Moore revised his prediction in 1975: double **every 2 years** (24 months)
  → THIS IS MOORE'S LAW
- Intel's exec David House added CPU complexity would double **every 18 months**
- History shows # Transistors has doubled every –
  - **2 years** in *logic*
  - **18 months** in DRAM/SRAM





Origin of Moore's Law

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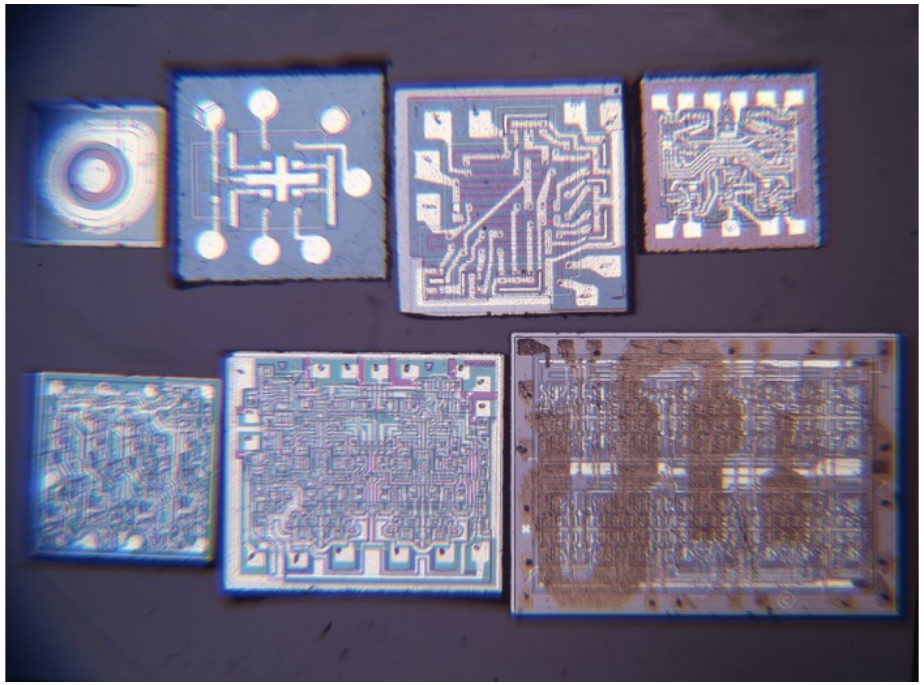

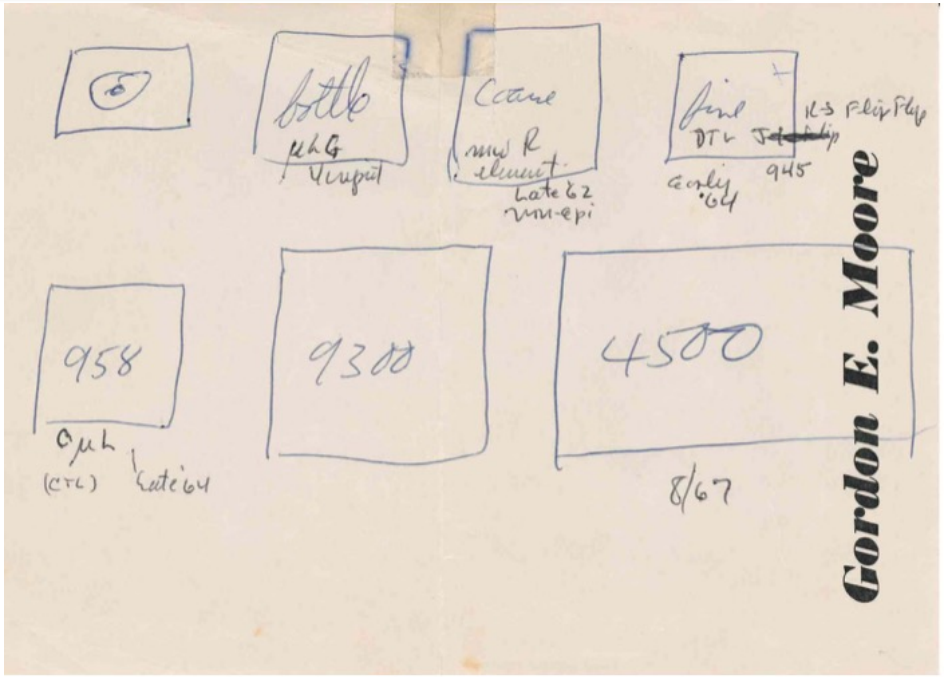

Figure 3. Gordon Moore notes on IC device types. Collection of the Computer History Museum, 102783359.

Year	Device	Function	Transistors	Resistors	Components	LOG_2
1959	2N697	Transistor	1	0	1	0
1962	Type G	RTL 3 - I/P gate	3	4	7	2.8
1963 (late 62)	Type R	RTL D Flip Flop	15	18	33	5.0
1964	945	DTL R-S Flip Flop	13	21	34	5.1
1965 (late 64)	958	RTL Counter	33	25	58	5.9
1966	9300	TTL Shift Register	85	40	125	7.0
1967	4500	DTL 32- Gate Array	200	64	264*	8.0

Figure 4. Table of component count for devices in photograph.

Microprocessor Timeline

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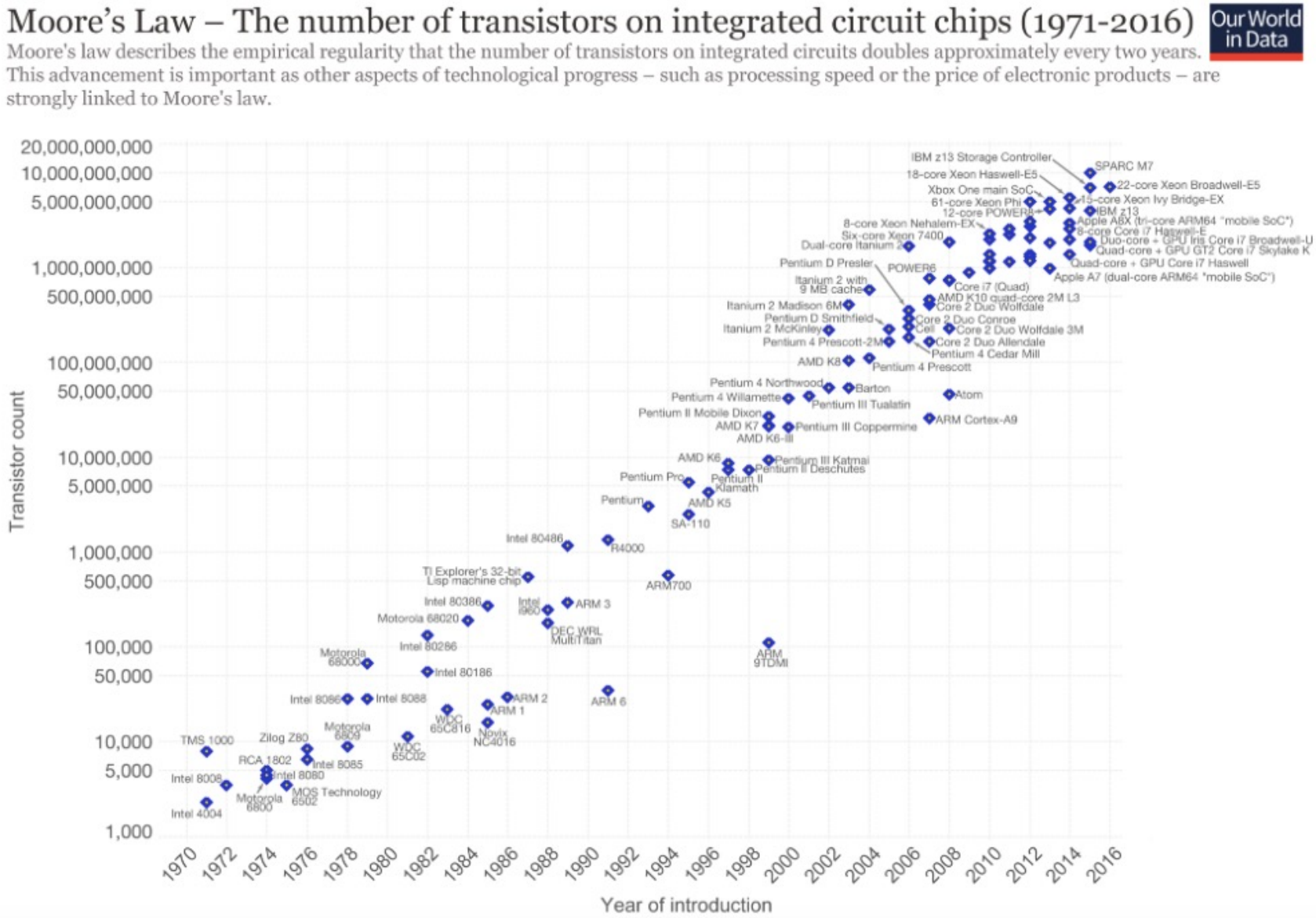

Data source: Wikipedia (https://en.wikipedia.org/wiki/Transistor_count)
The data visualization is available at OurWorldinData.org. There you find more visualizations and research on this topic.

Memory Timeline

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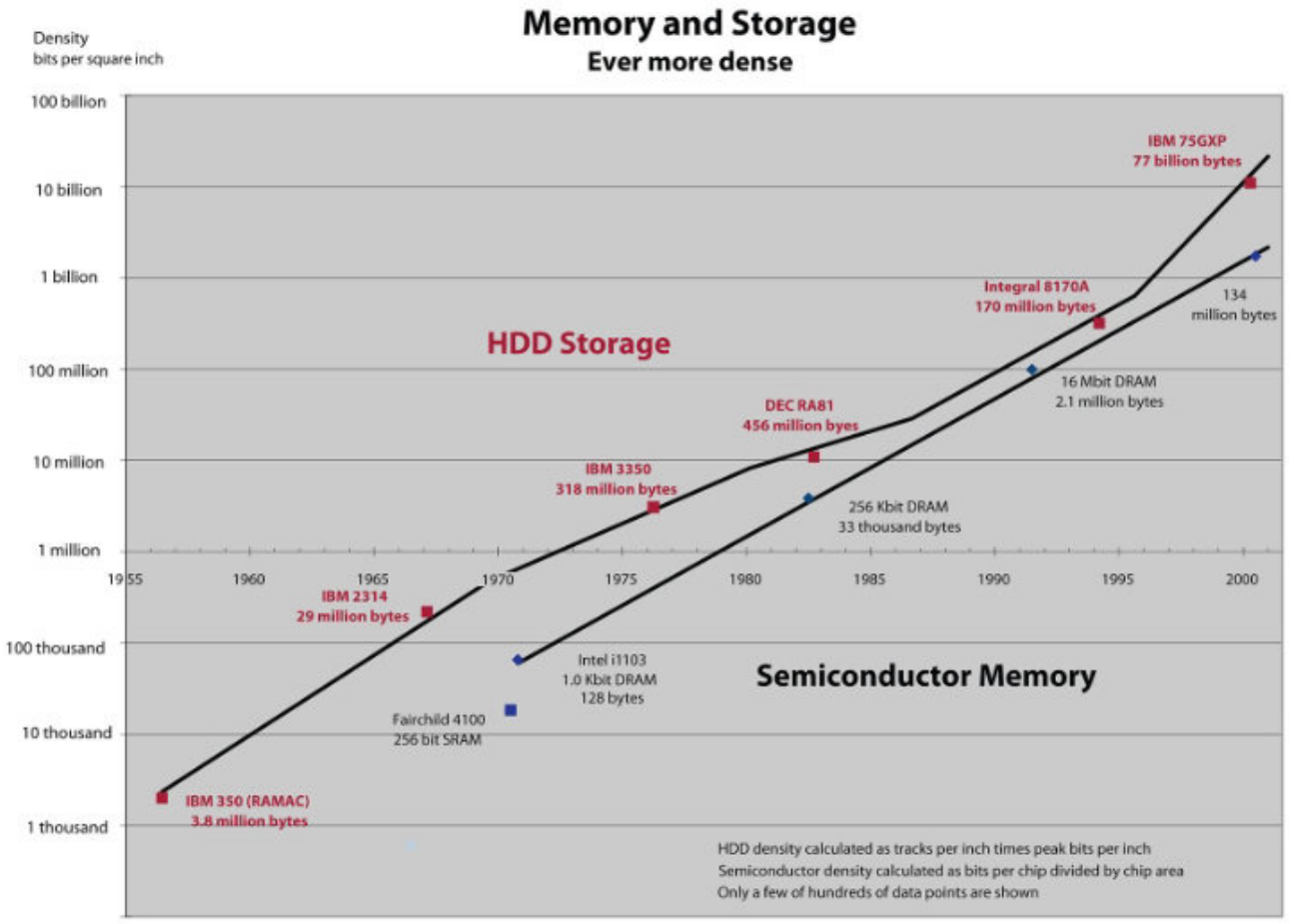

Hard disk storage has become denser at an exponential rate over the last 50 years, just like main memory. The dramatic increase in capacity and speed of both has fueled the increasing power of computers.

Moore's Scale

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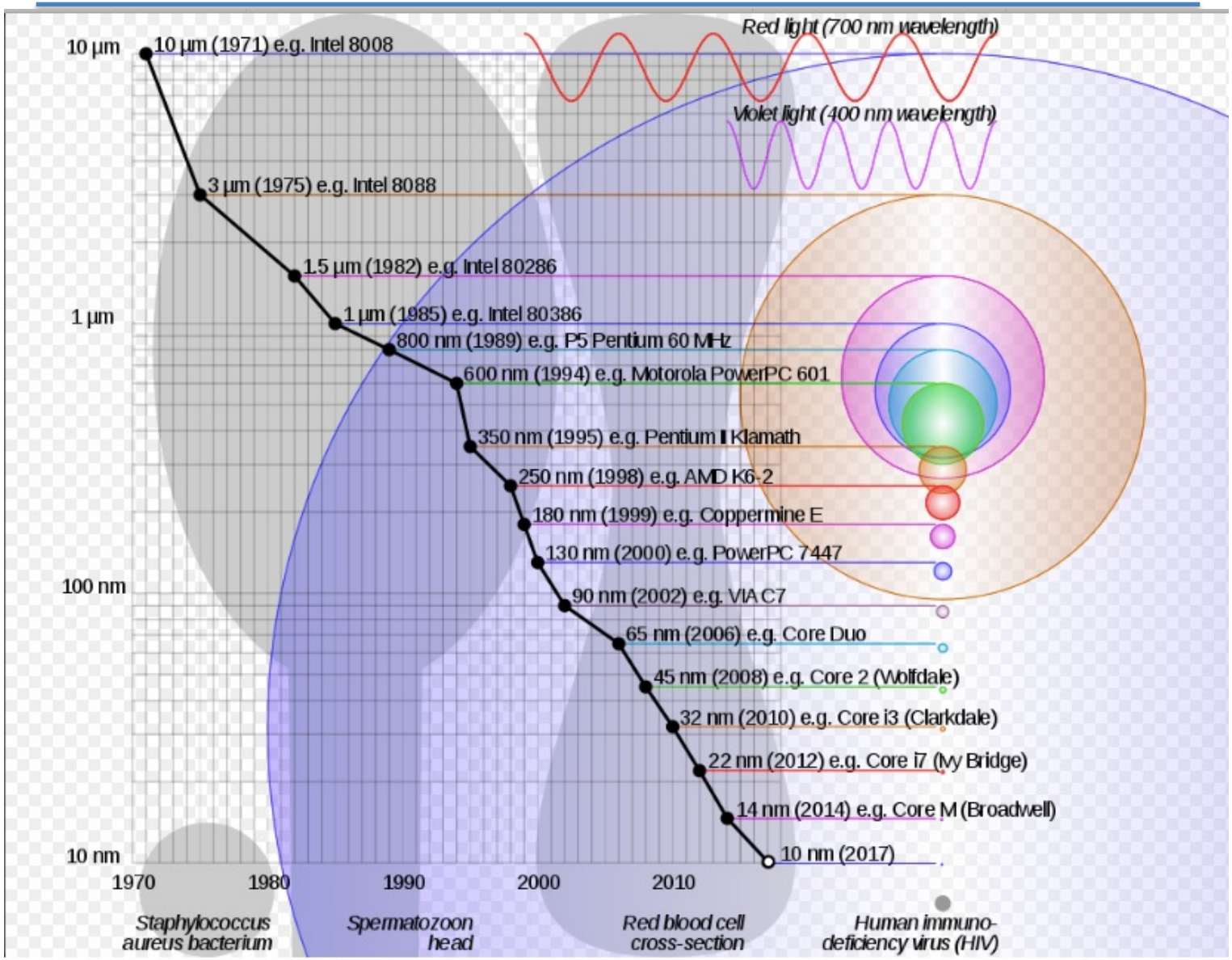

and comparison of sizes of semiconductor manufacturing process nodes with some microscopic objects and

Future of Moore's Law

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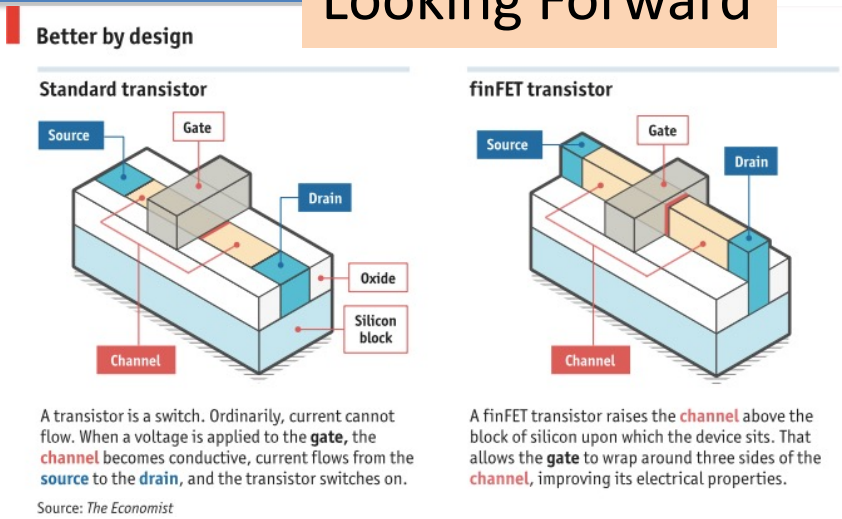
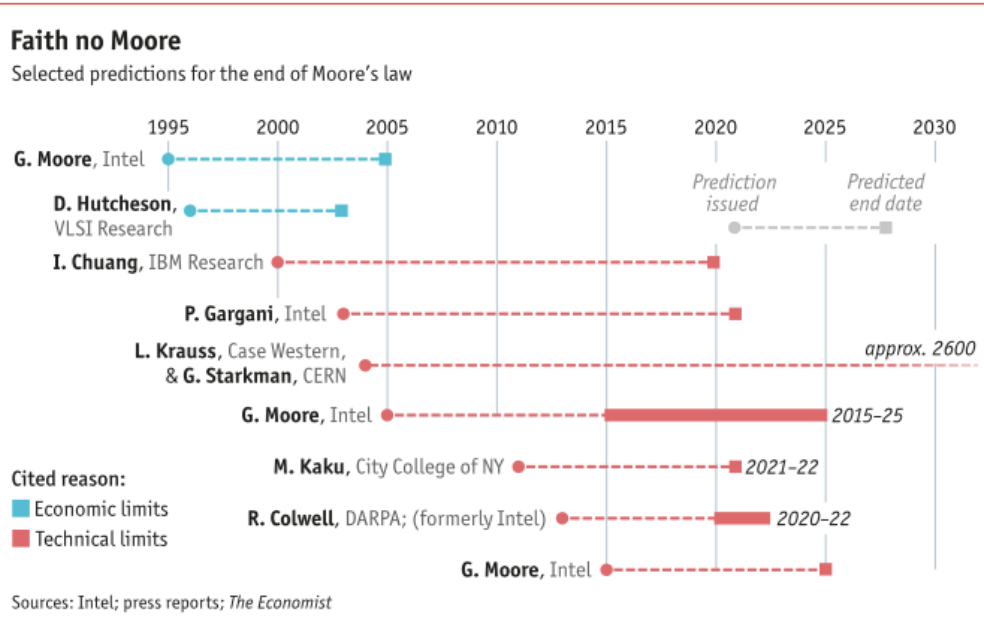
Looking Forward

- Chip design
  - Transistors
    - SiGe
    - FinFET
    - JNT
  - Chip stacks (3D hybrid)
    - Intel/Micron 3D Xpoint
  - 3D
    - NAND Flash (EEPROM)
- Architecture
  - Specialized hardware (GPU, APU, etc.)
  - Reconfigurable hardware (FPGA)
- Thermal/Cooling
  - Microfluidics (liquid cooling)
- Something completely diffferent
  - Molecular computing
  - Quantum computing

"As Moore's Law slows, we are being forced to make tough choices between Power, Performance and Cost." (ARM)



New sorts of transistors can eke out a few more iterations of Moore's law, but they will get increasingly expensive



TSMC on Moore's Law

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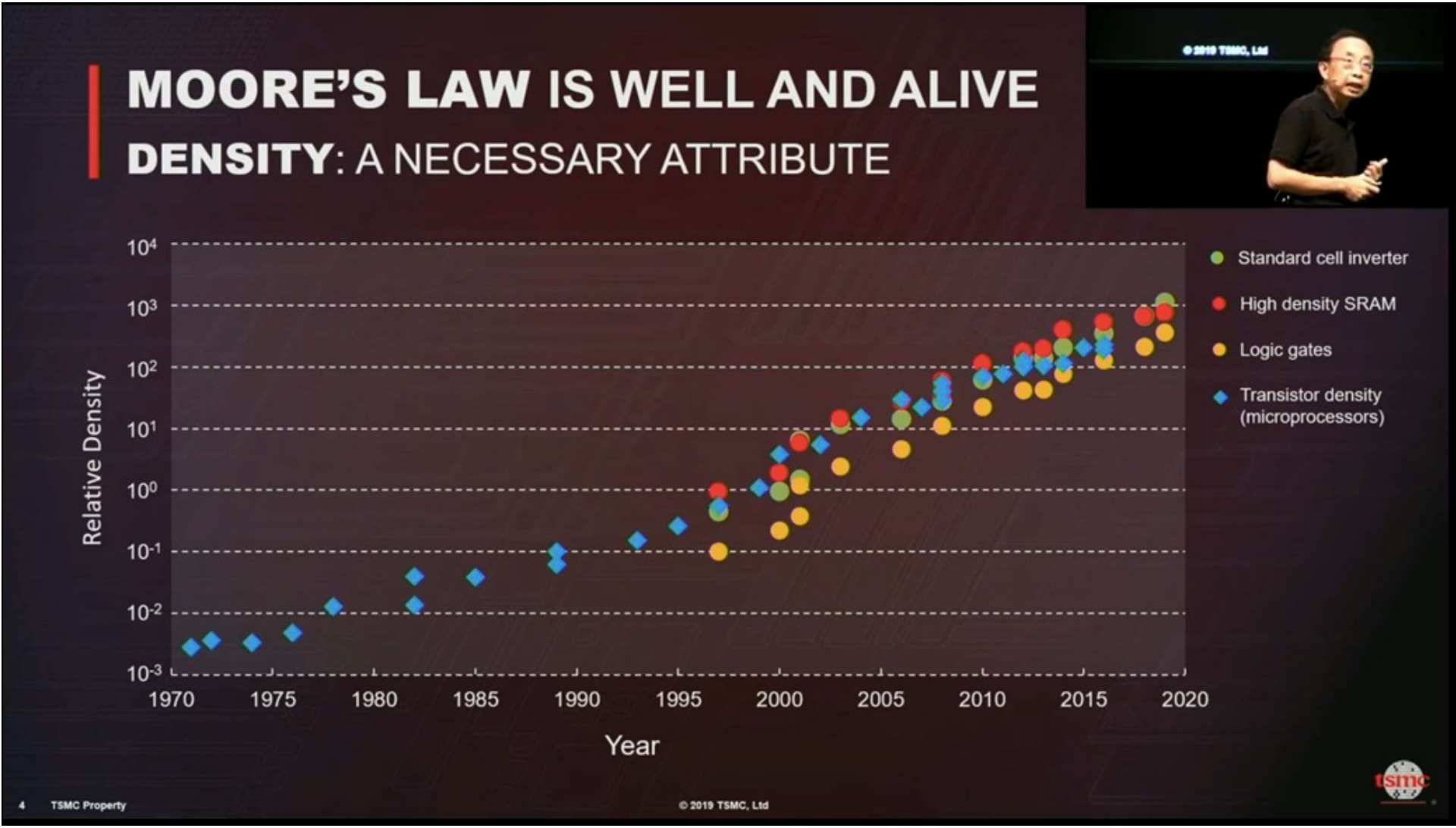

Moore’s Law 1985

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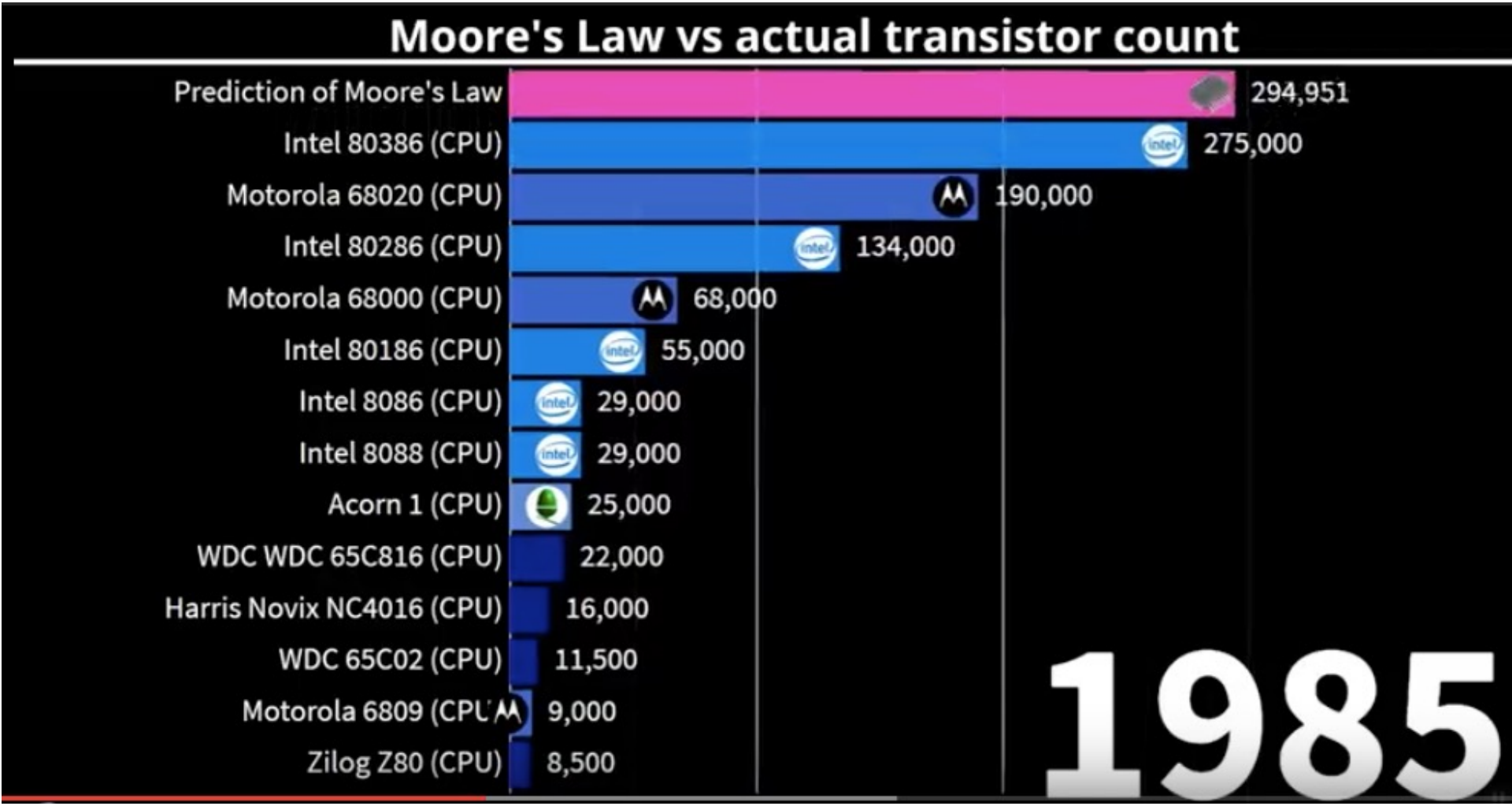

Moore’s Law 1995

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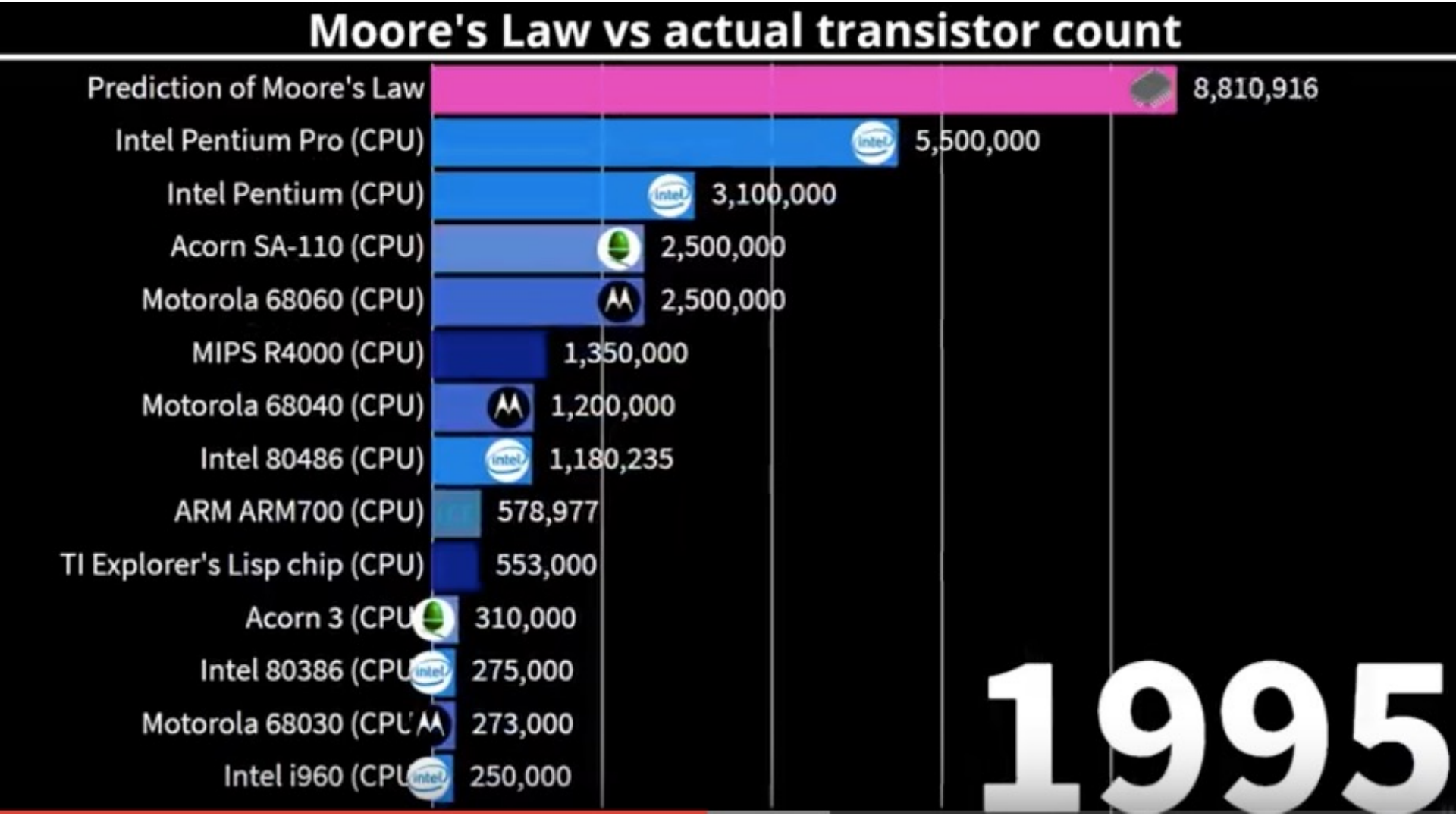

Moore’s Law 2000

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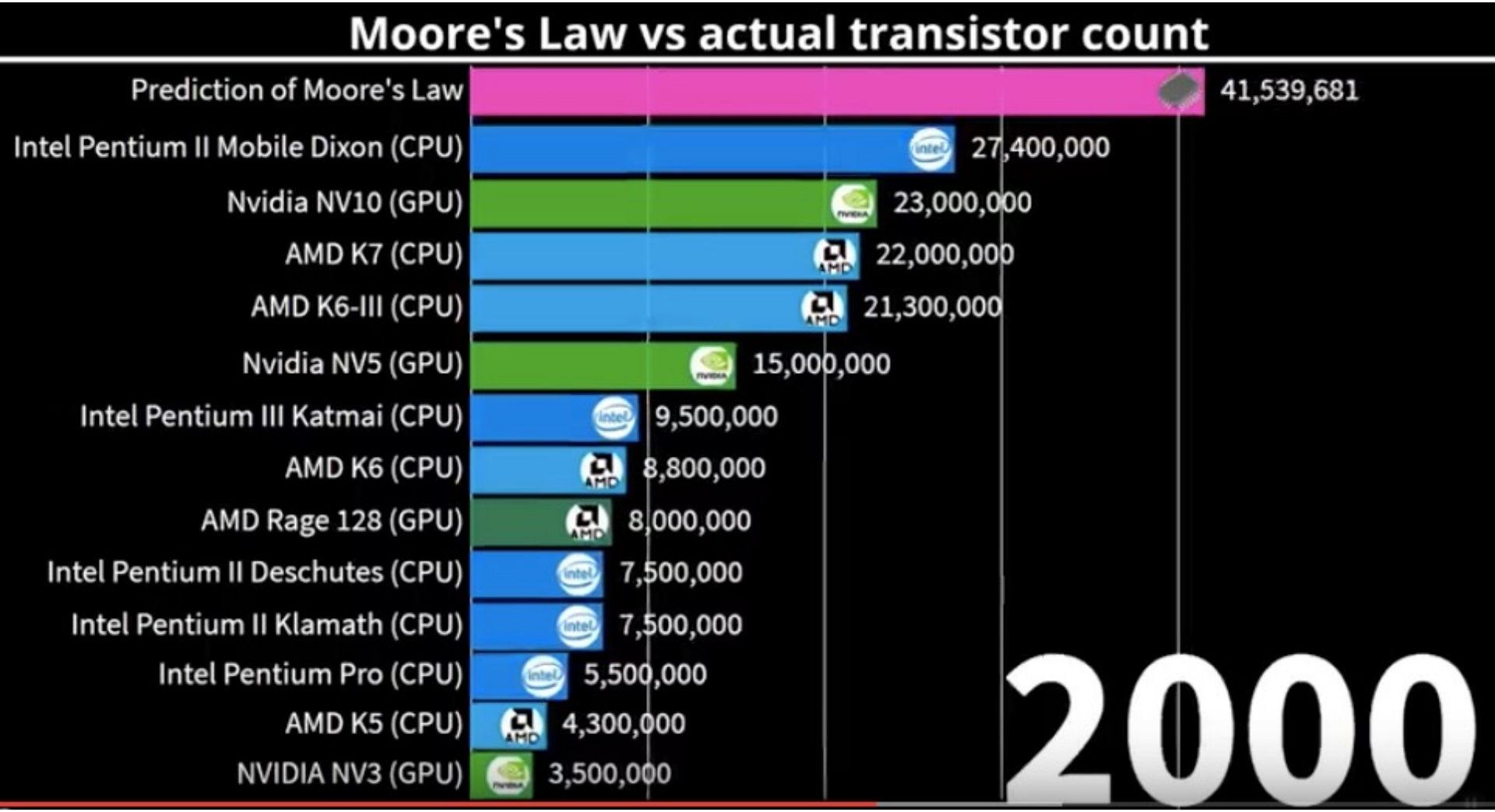

Moore’s Law 2005

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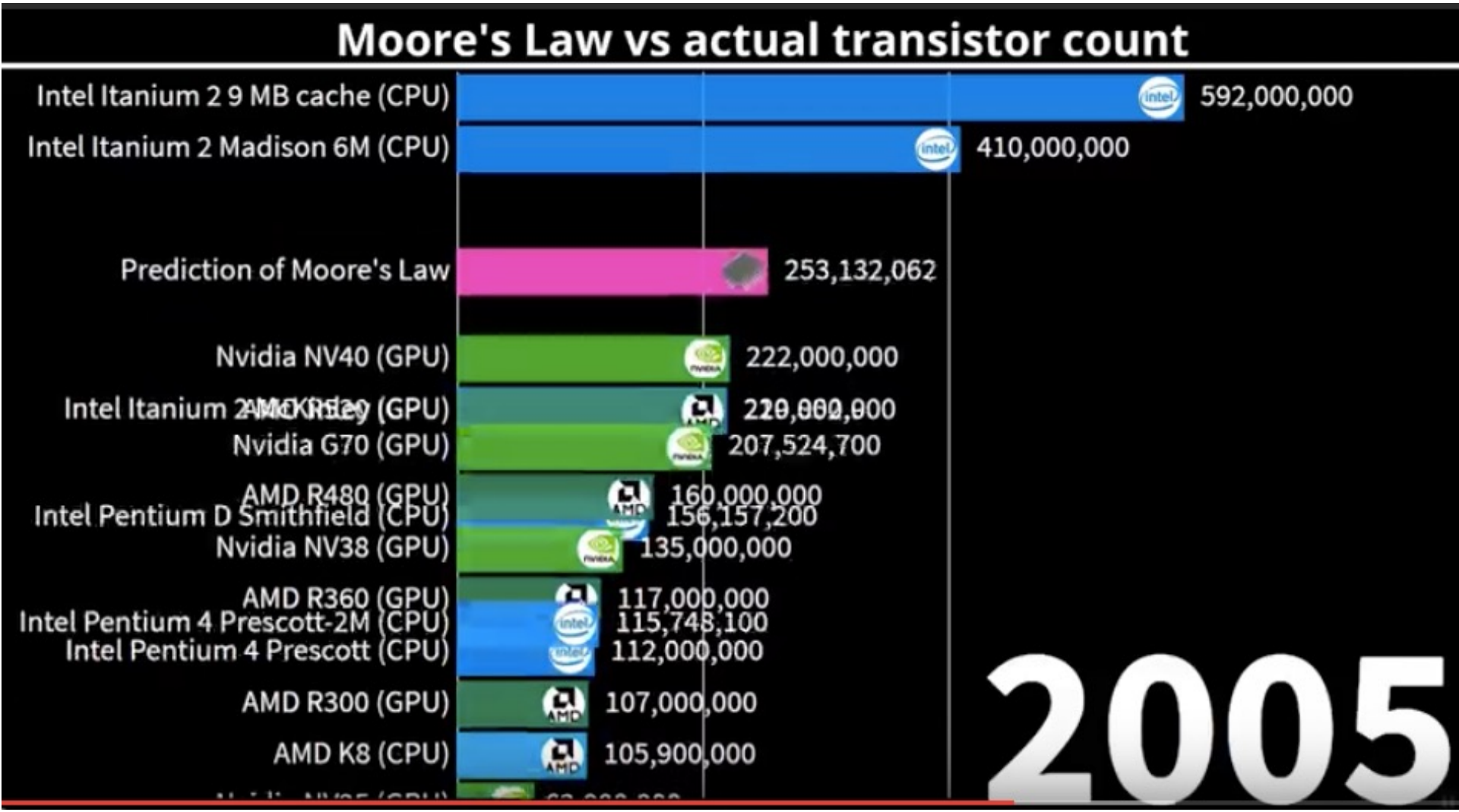

Moore’s Law 2010

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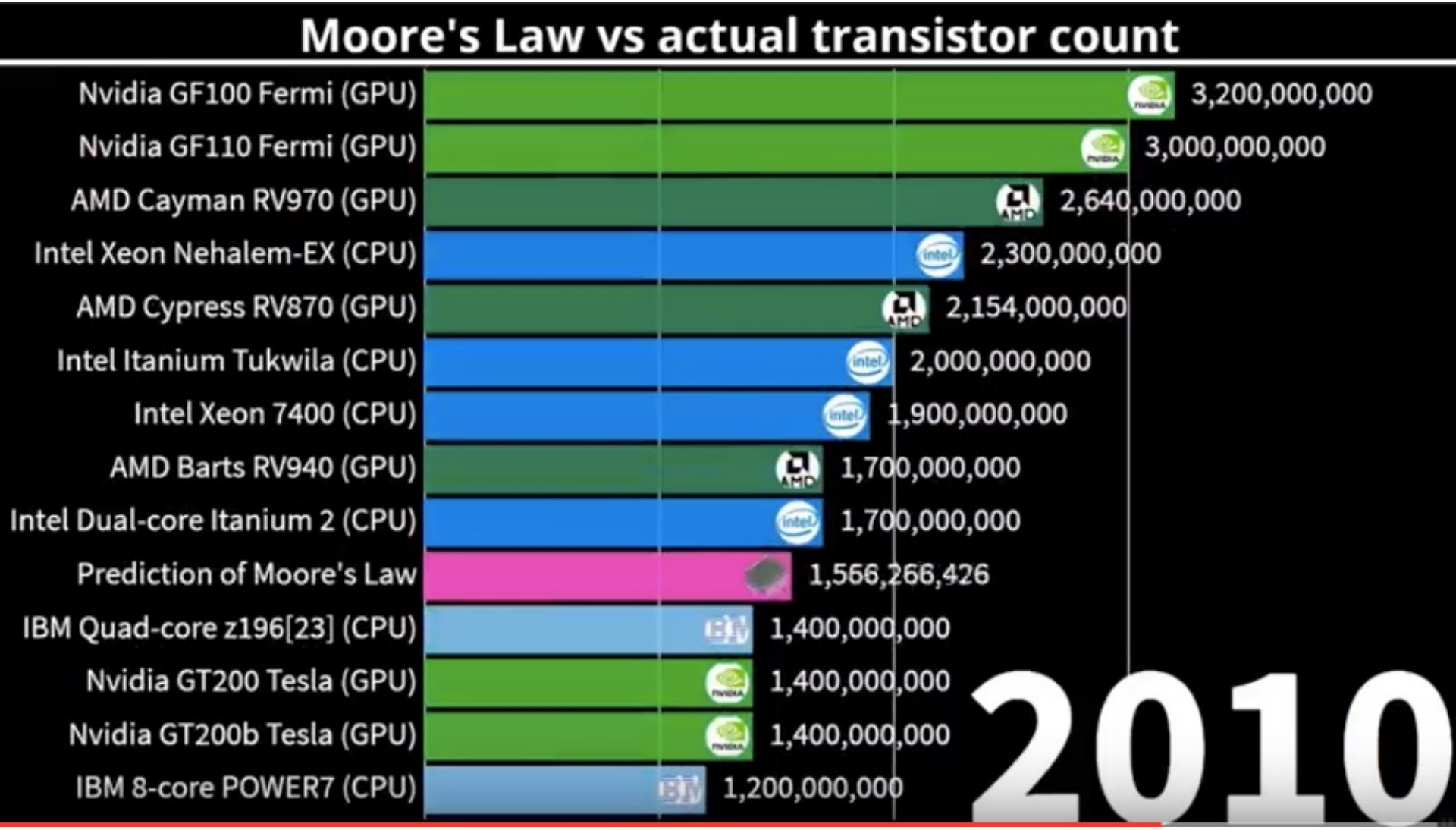

Moore's Law 2015

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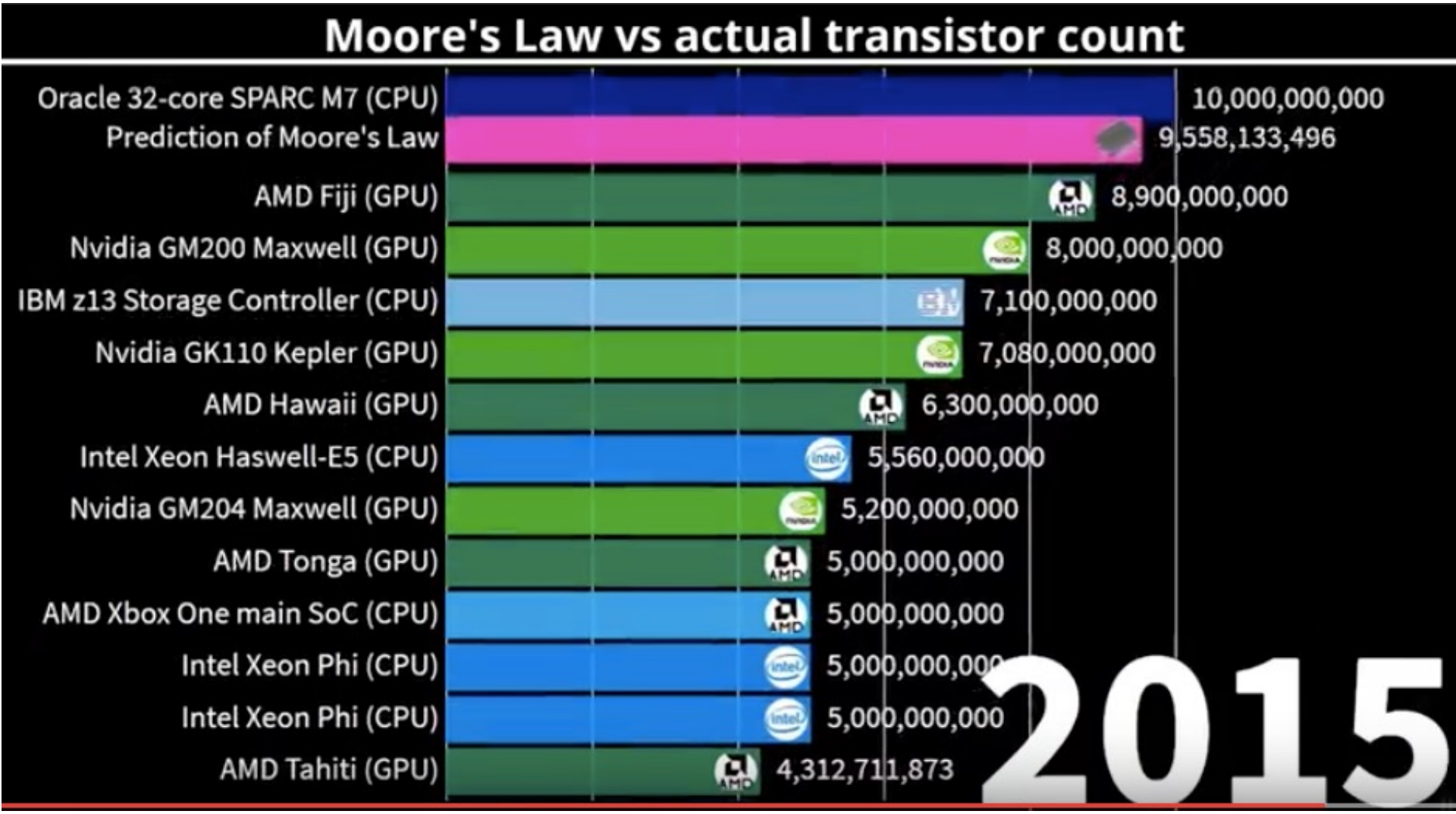

Moore’s Law 2018

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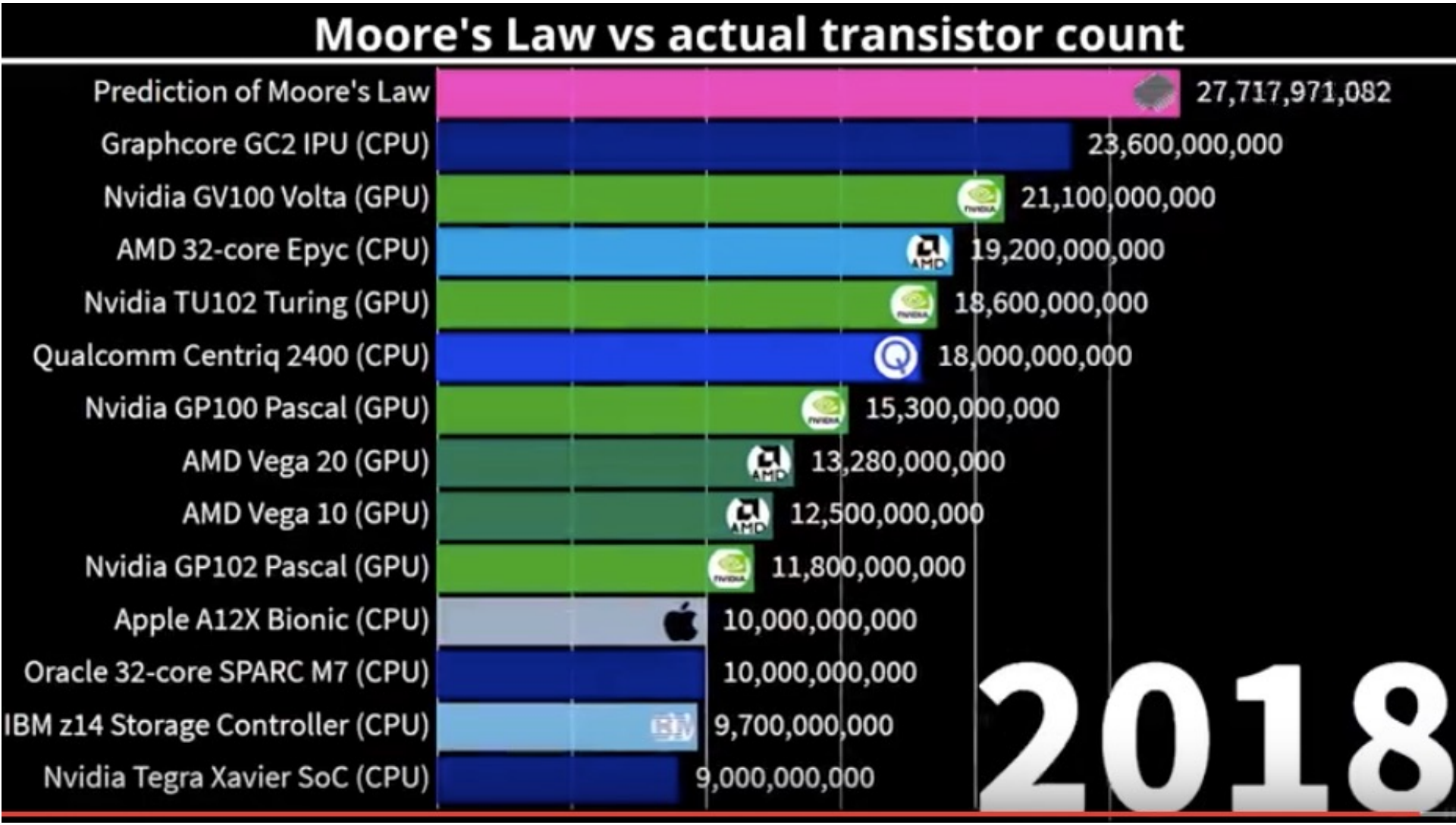

Moore’s Law 2020

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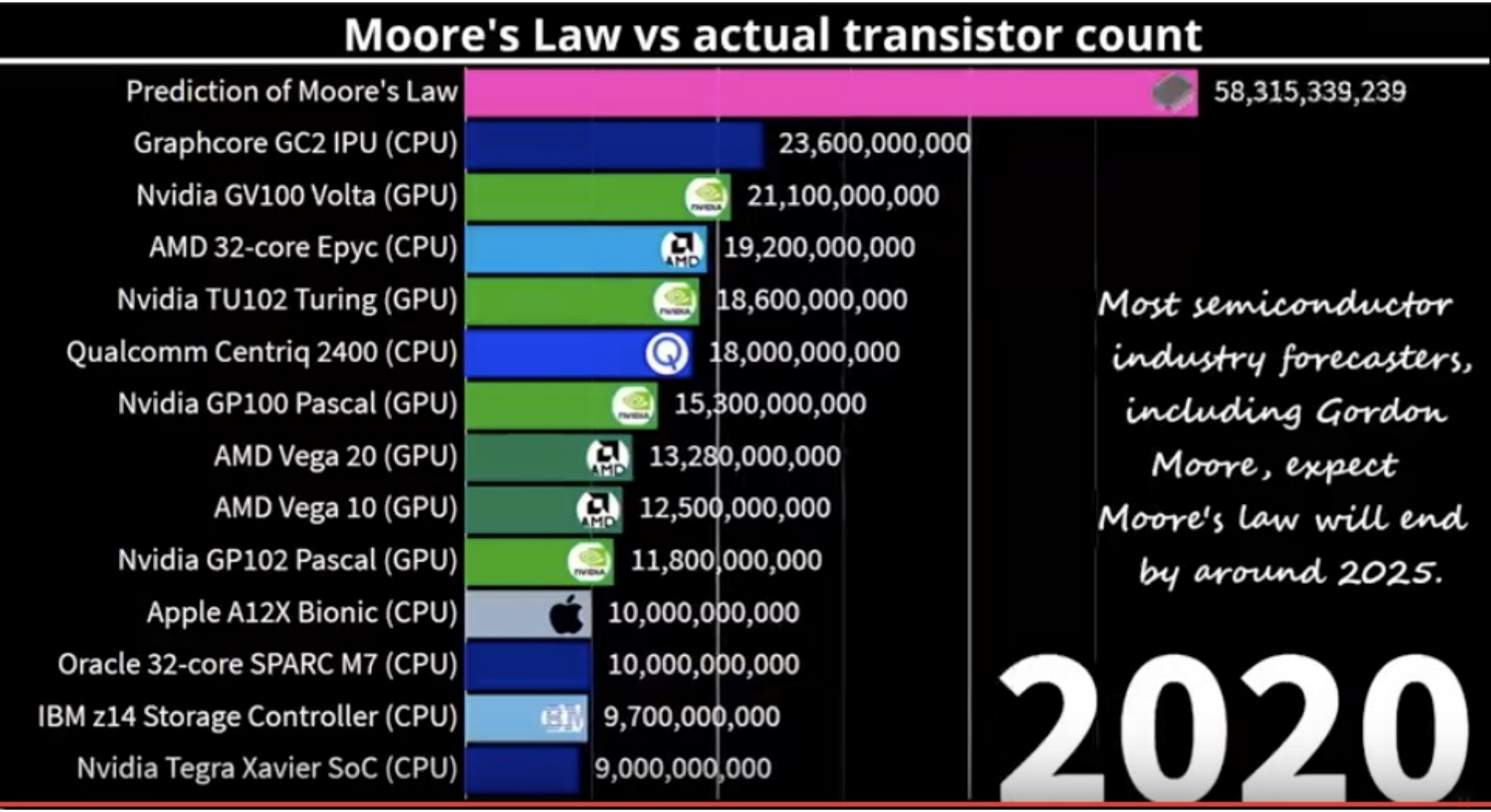

Chips-Moore's Law

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4.5 – 5 GHz

Even with Moore's Law continuing apace, have we reached a plateau where, unless you have a special need like gaming or animation, a 3to6 year old desktop or laptop is good enough for most users? Has the innovation shifted to phones and tablets?

Jeff Drobman, Lecturer at California State University, Northridge (2016-present)

Answered just now

Moore's Law has indeed slowed to a crawl over past serveral years. we see that CPU frequency has plateaued to about 4.5 GHz. performance has been gained by adding cores, incl specialized cores like GPU, NPU.

Performance Factors

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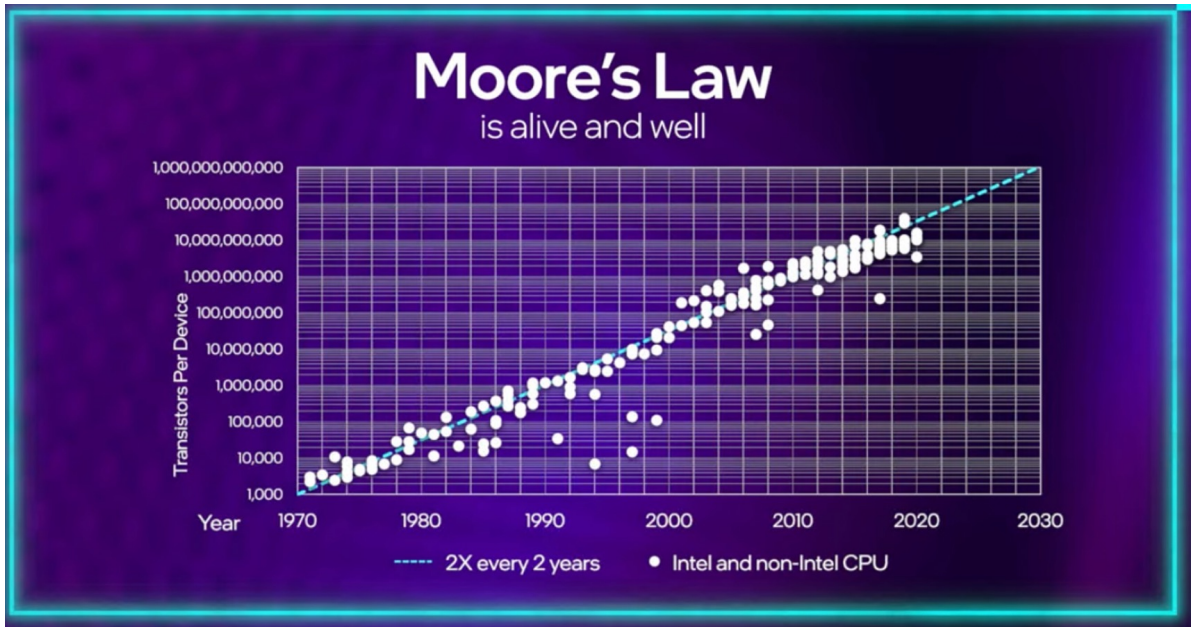
Will computing stop improving when Moore's law ends?

Jeff Drobman, Lecturer at California State University, Northridge (2016-present)

Answered just now

yes and no. an individual core (CPU or GPU) will not have its integer scalar performance increase. but "ILP" can be applied to cores, along with parallel data as vectors or matrices. achieving greater degrees of parallelism (in both hardware and software) is the fertile ground for performance increases.



Intel's View of Moore

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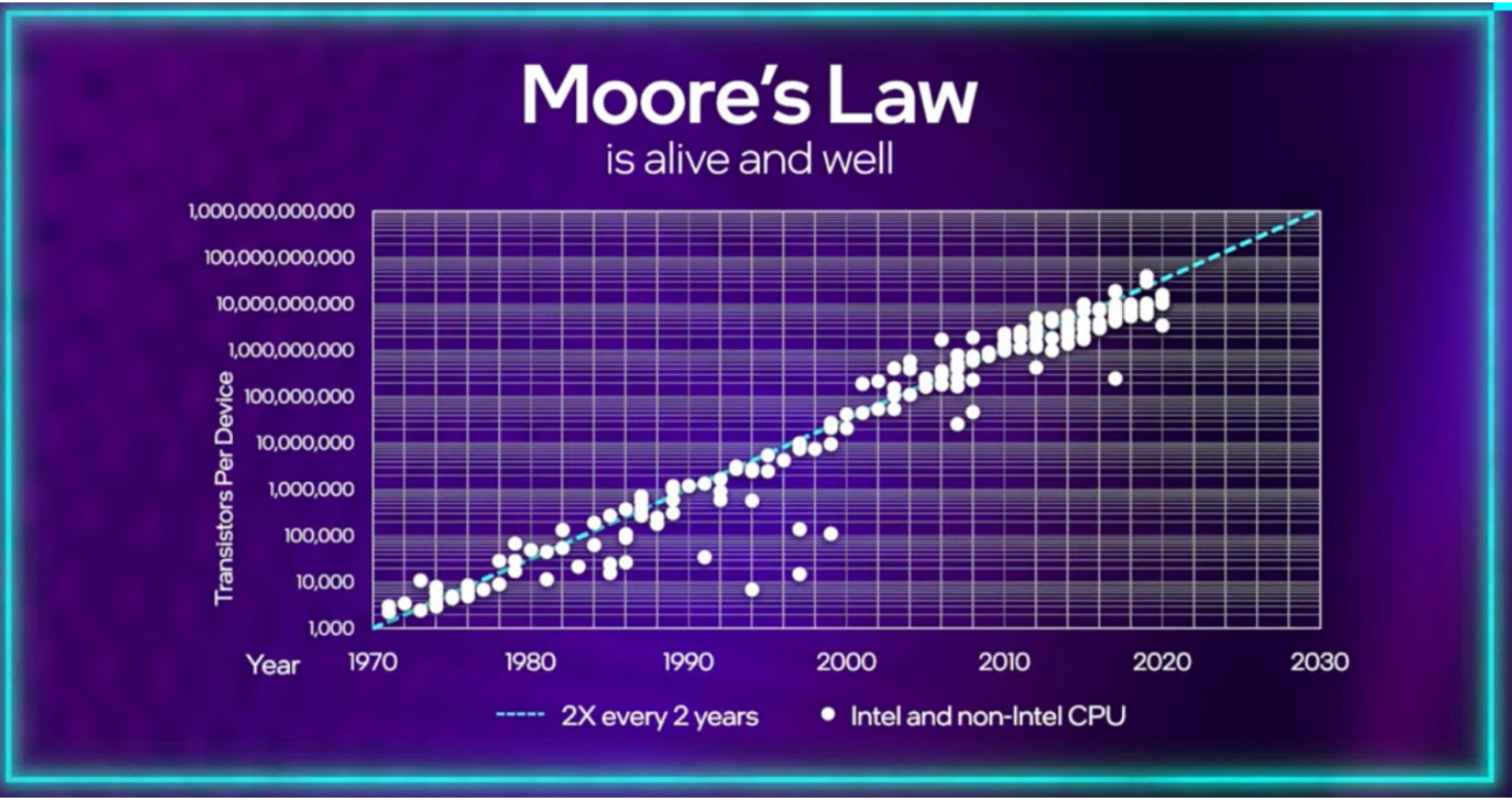
Jeff Drobman

Nov 2021

Intel CEO Gelsinger just claimed Intel will exceed this rate!



Moore's Law Future

Jeff Drobman

Jan 2020

Arm Shows Backside Power Delivery as Path to Further Moore's Law

Delivering power to devices from the other side of the silicon will enable smaller processors

Chips

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Chip Shortage

Chip Shortage

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REUTERS

Biden zeroes in on chip shortage

Chip Shortage: SEMI

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MILPITAS, Calif. – April 1, 2021 – SEMI, the industry association serving the global electronics design and manufacturing supply chain, today applauded the inclusion of initiatives to strengthen U.S. semiconductor manufacturing and research and calls for investment in the Biden Administration's American Jobs Plan. In addition to calling on Congress to invest $50 billion in semiconductor manufacturing and research, in line with the bipartisan CHIPS for America Act, the plan lists semiconductors as a field of focus in its call for an investment of another $50 billion in the National Science Foundation (NSF).

"Reversing the 50% decline in the U.S. share of semiconductor manufacturing capacity over the past 20 years requires bold action, and the Biden administration's support for significant funding to bolster the industry in its American Jobs Plan is an important step forward," said Ajit Manocha, SEMI president and CEO. "Funding the authorized CHIPS For America Act provisions and enacting an investment tax credit to support investment in the U.S. semiconductor supply chain will make the United States a globally competitive location for new semiconductor facilities. The plan's focus on addressing workforce development in the industry is encouraging as well, as the competition for talent is intensifying to support projected growth."

About SEMI

SEMI® connects more than 2,400 member companies and 1.3 million professionals worldwide to advance the technology and business of electronics design and manufacturing. SEMI members are responsible for the innovations in materials, design, equipment, software, devices, and services that enable smarter, faster, more powerful, and more affordable electronic products. Electronic System Design Alliance (ESD Alliance), FlexTech, the Fab Owners Alliance (FOA) and the MEMS & Sensors Industry Group (MSIG) are SEMI Strategic Technology Communities, defined

Intel CEO on Chip Shortage

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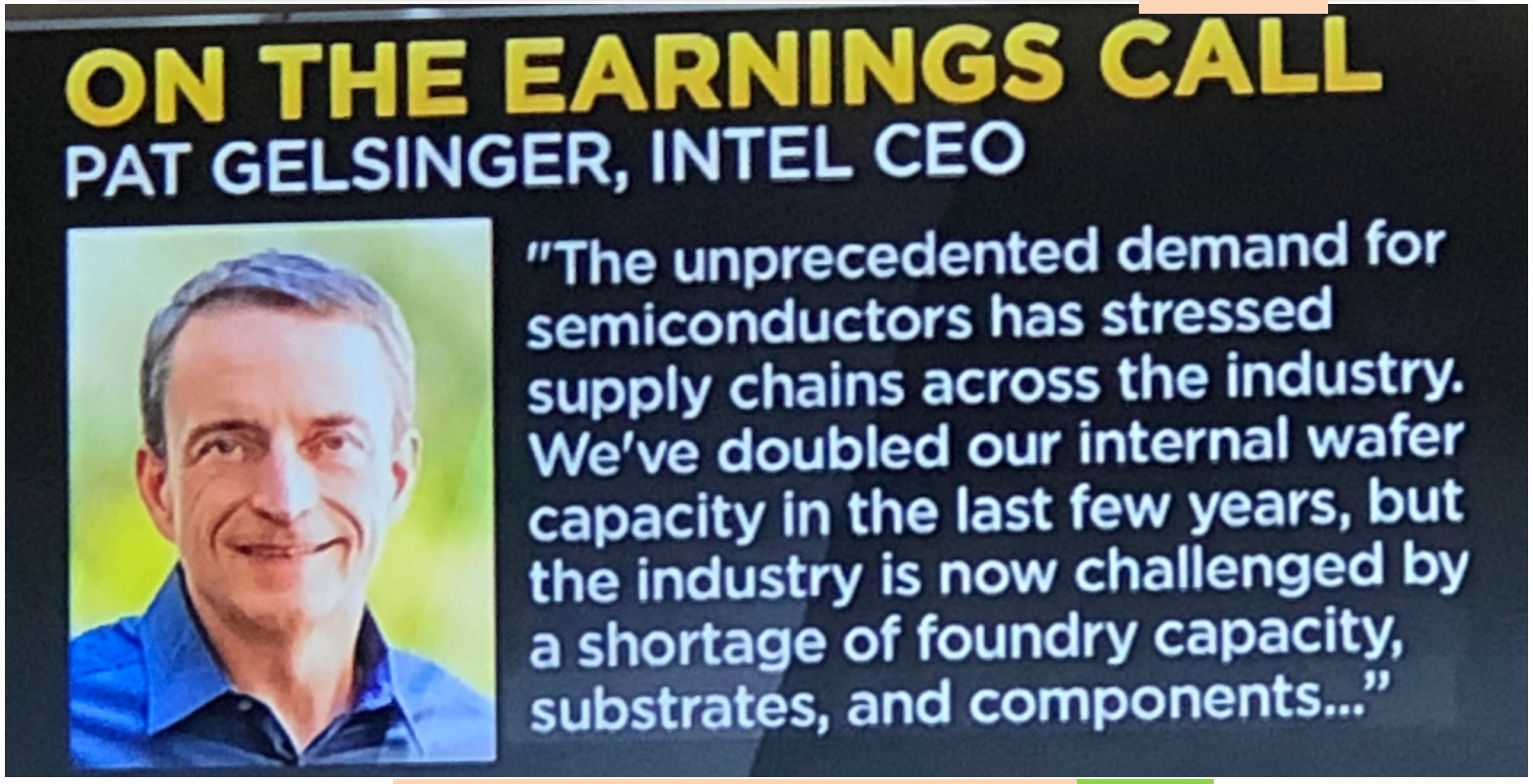
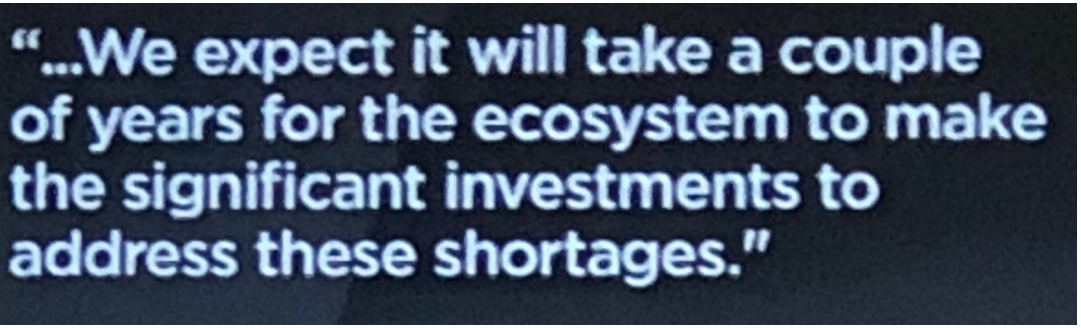
4-23-21



Intel building 2 new fabs in AZ **$20B**



- Intel, Micron only remaining US fabs
- Intel produces **17%** of world supply
- US produced **37%** 20 yrs ago
- AMD divested its 25 fabs in 2006

Chip Shortage

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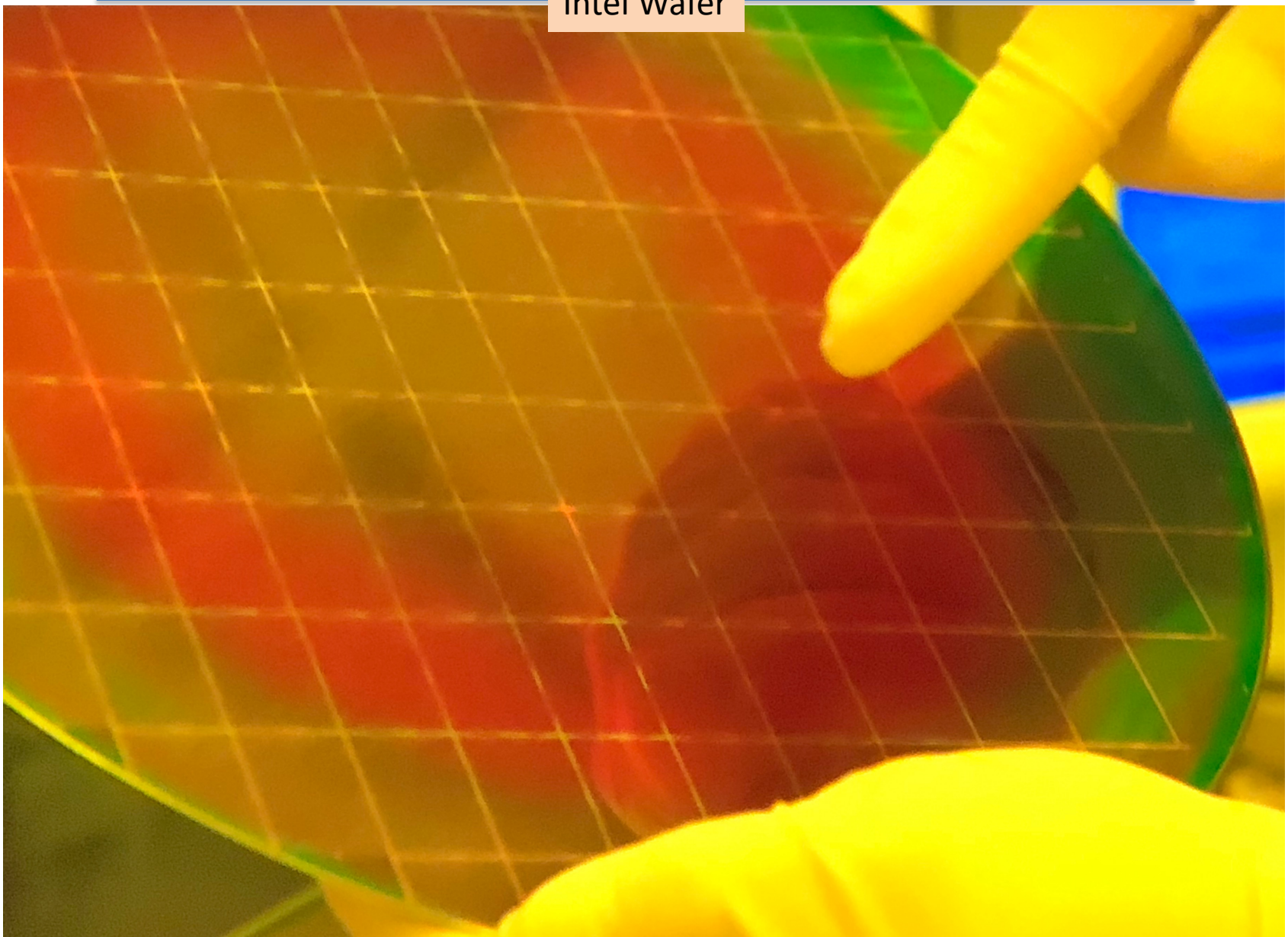
Intel Wafer



Chip Shortage

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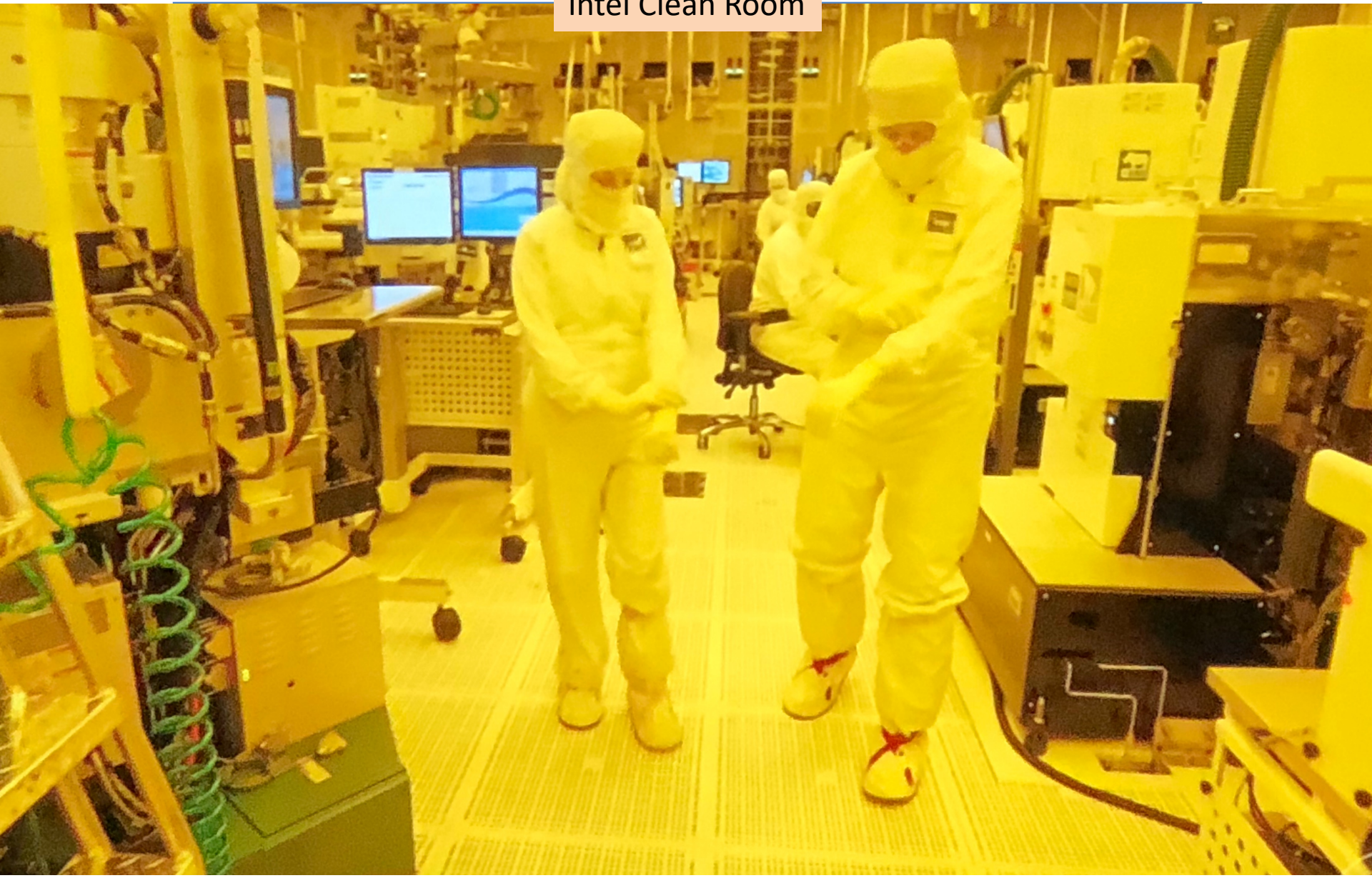
Intel Clean Room



Chip Shortage

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Intel Automated Fab

Chip Shortage

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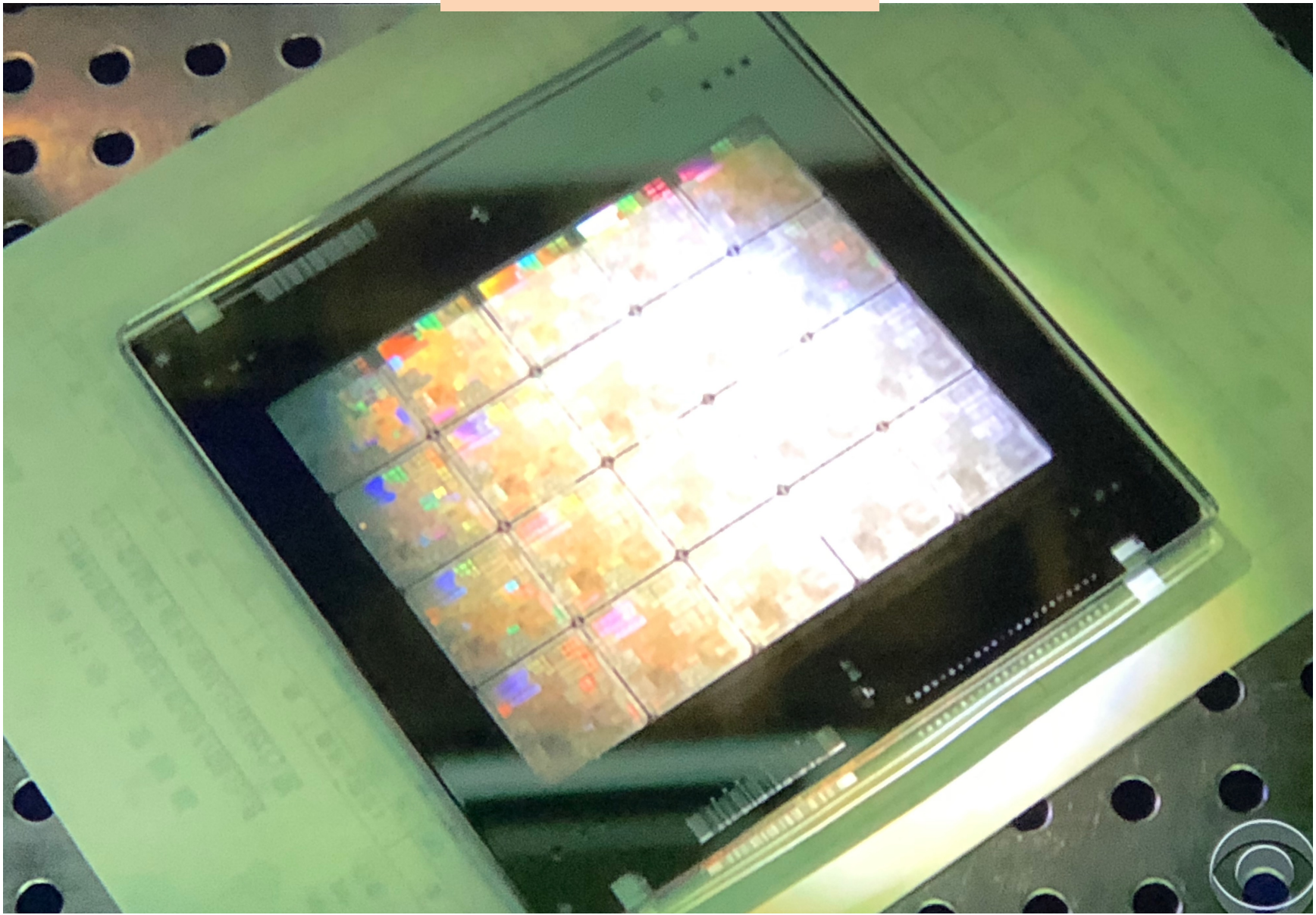
Intel Automated Wafer Test



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Wafers

Semiconductors: Si, Ge

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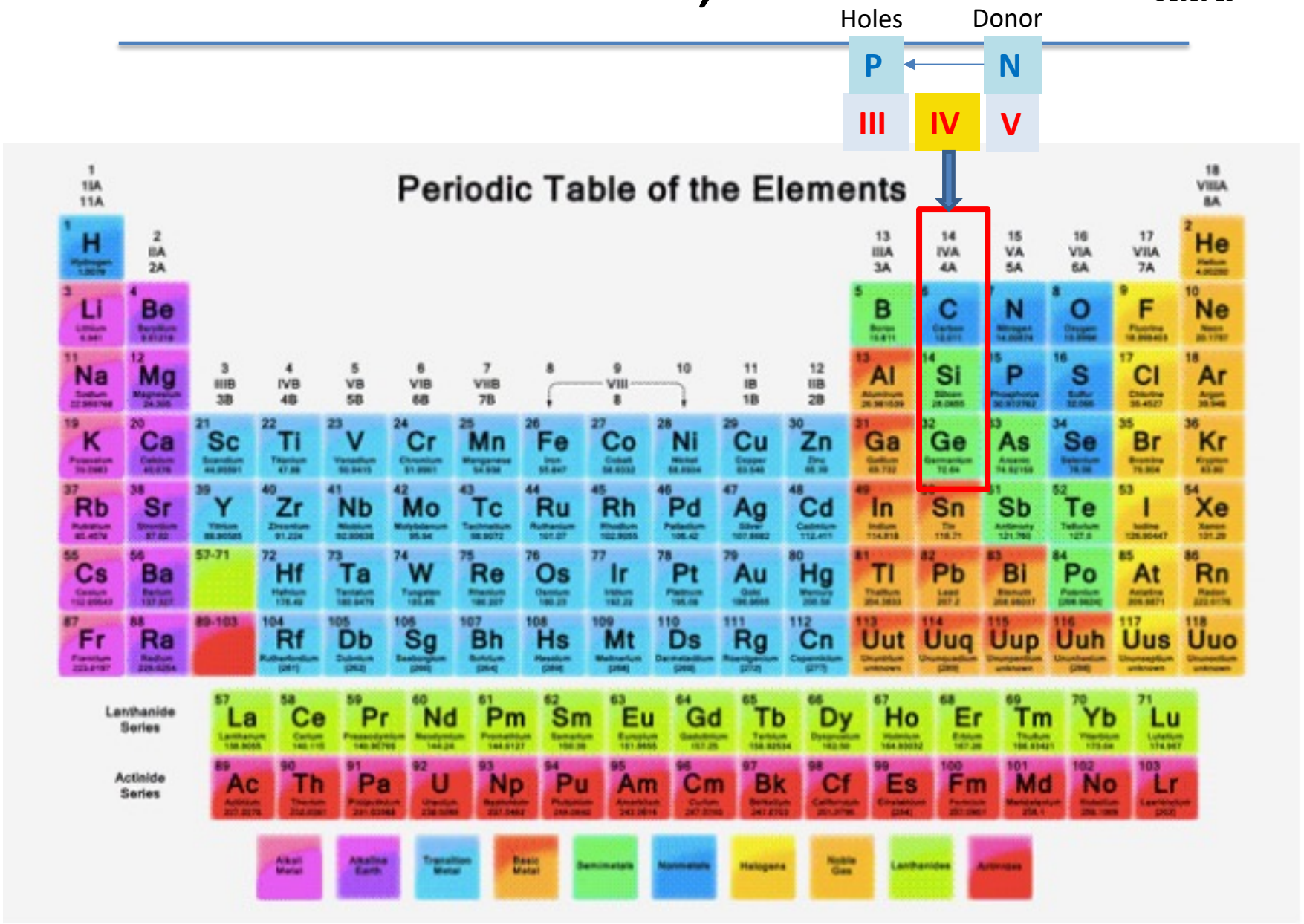
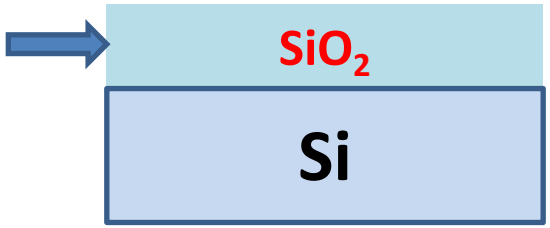
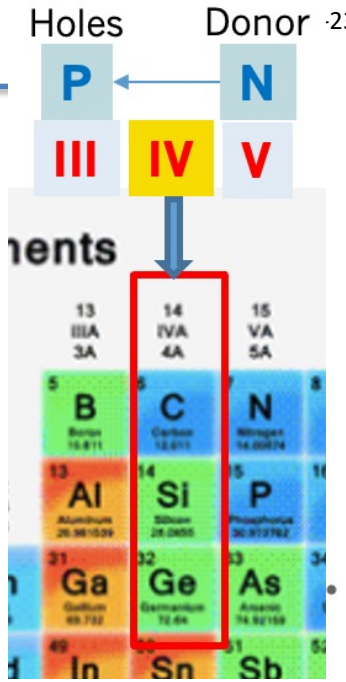


Si vs Ge





Quora

Chris Bevis · Follow
Lives in Silicon Valley (1997–present) · Updated Sep 9

Related **Why is silicon mostly used in tech companies than germanium?**

The earliest semiconductor devices were made of germanium. This started to change when the first planar IC's were developed. It is easy to grow a stable, insulating oxide film on silicon but not on germanium, so silicon was the material of choice. One of the key breakthroughs in silicon processing was made by Andy Grove and a colleague: the Grove-Deal model of SiO2 growth kinetics.

These days, most advanced devices have channels made of an alloy of Si and Ge doped with boron (SiGeB). The percentage of Si and Ge is carefully controlled and varied over the height of the channel to produce strain which enhances the mobility of electrons or holes.

Silicon Crystal Ingot (Boule)

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Wafers

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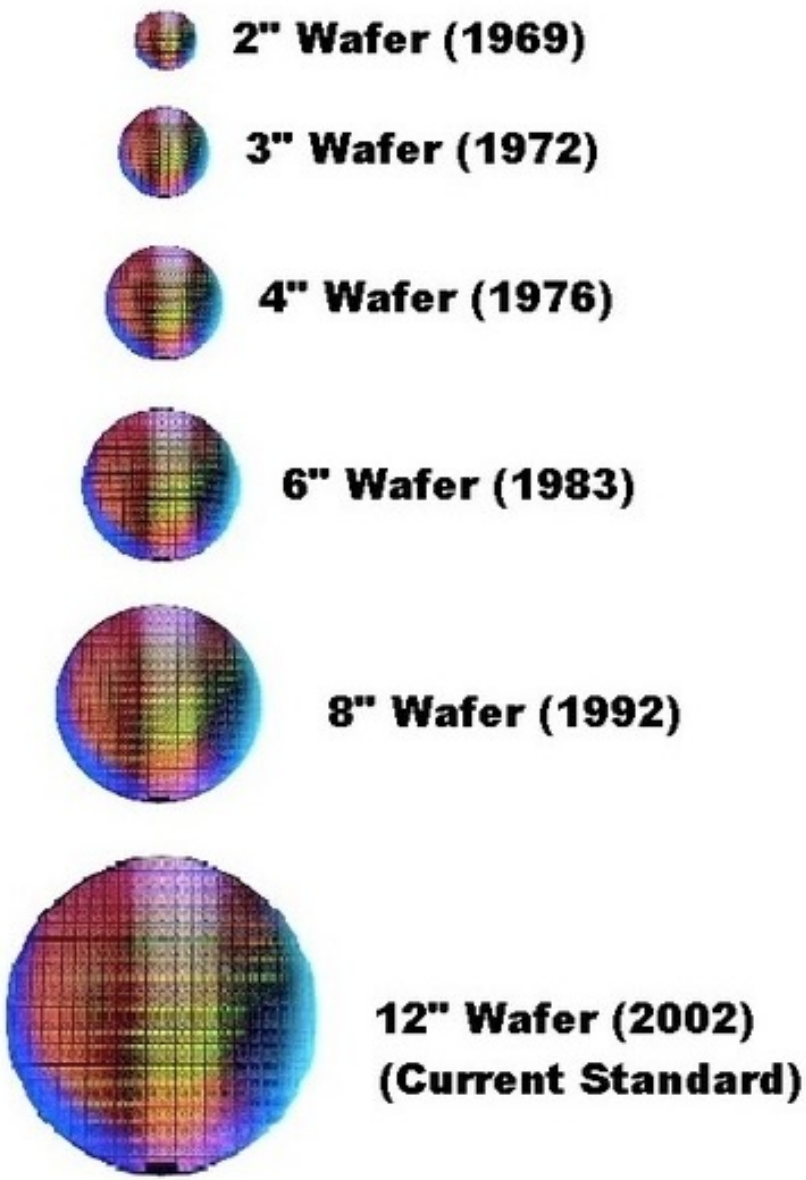

300mm

Samsung 300mm Wafers

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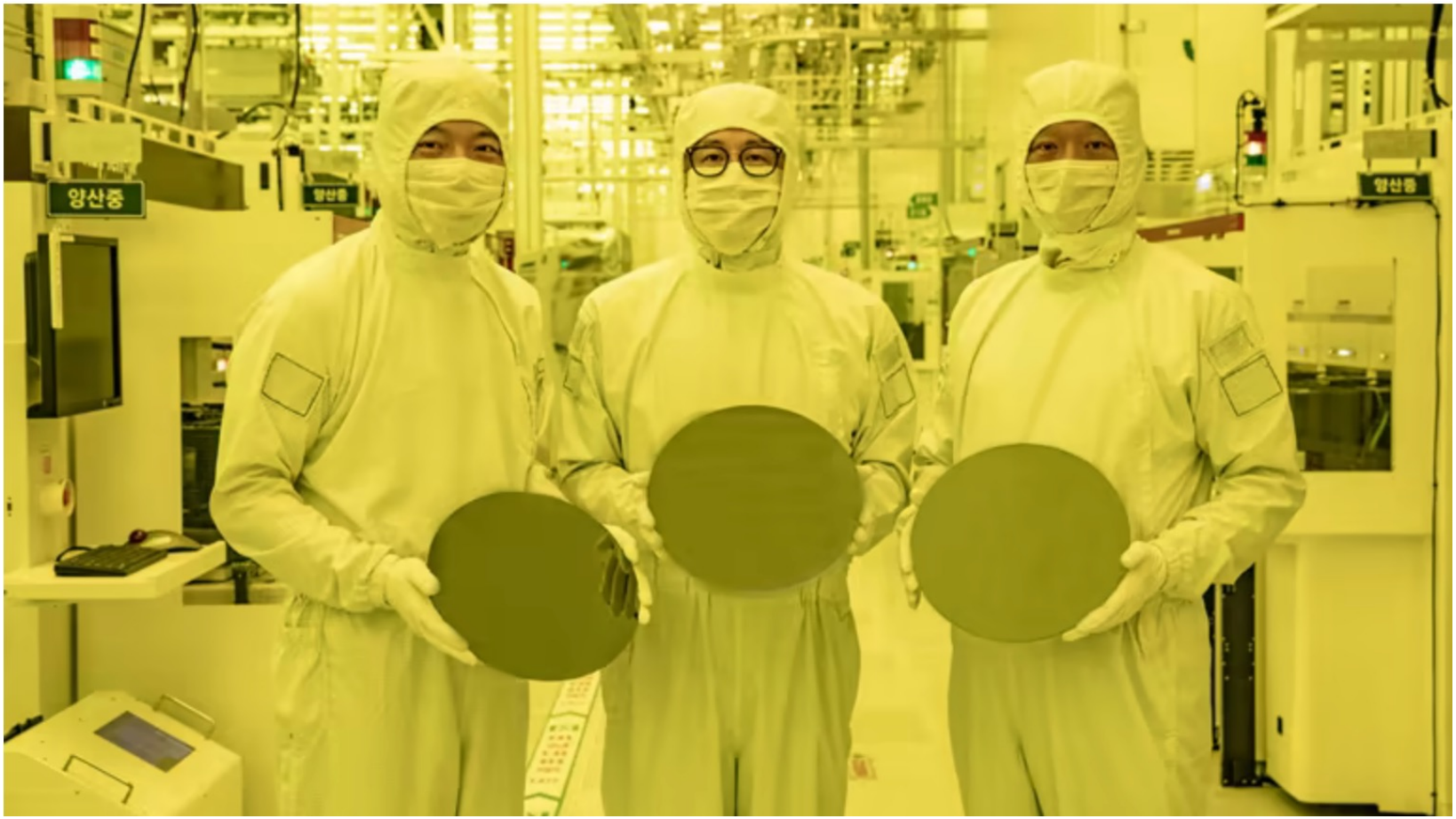

Wafers

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200 And 400 mm wafers

Die on a Wafer

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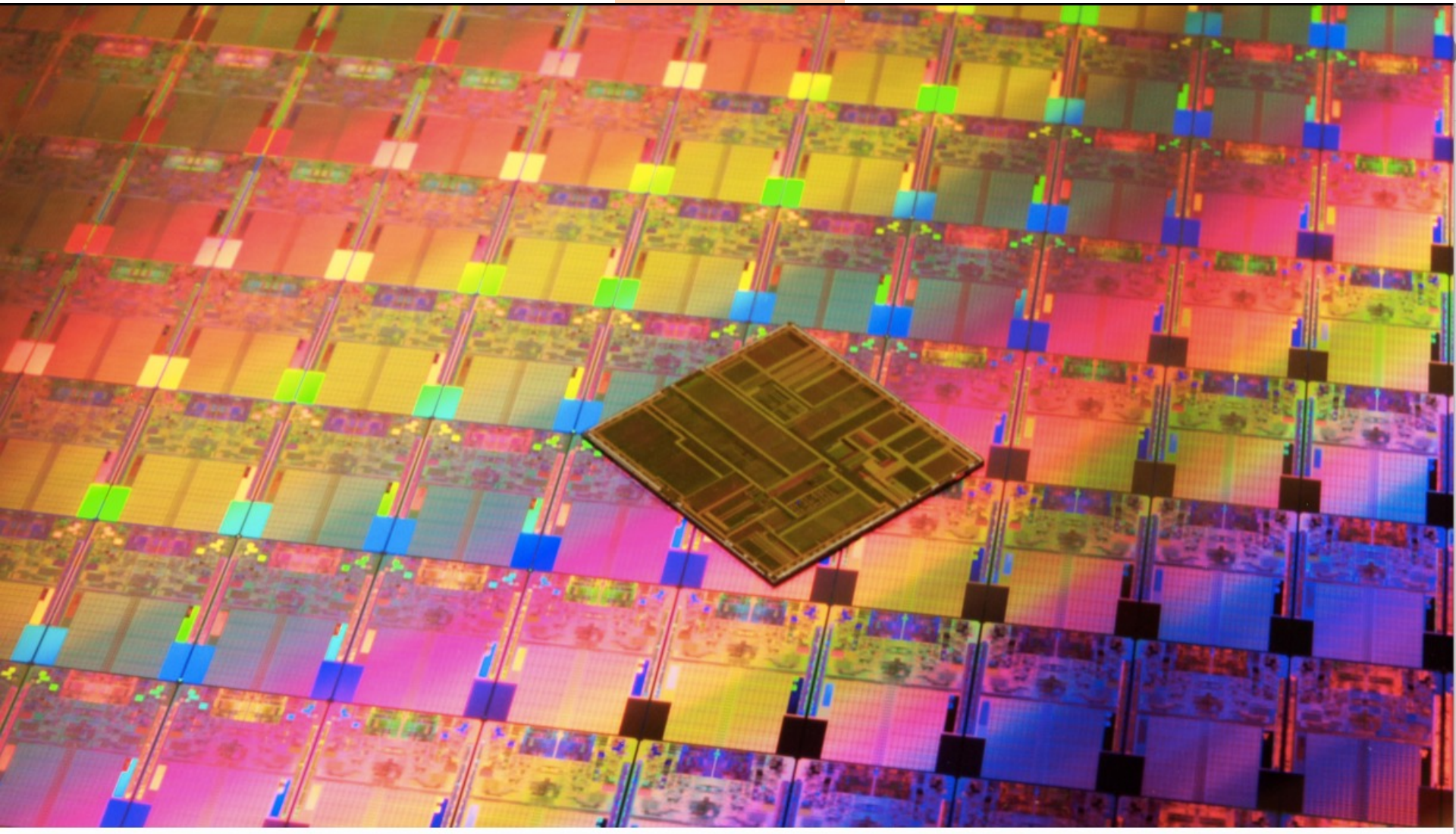
Intel Pentium



Intel Pentium microprocessor die and wafer

Quora

Wafers

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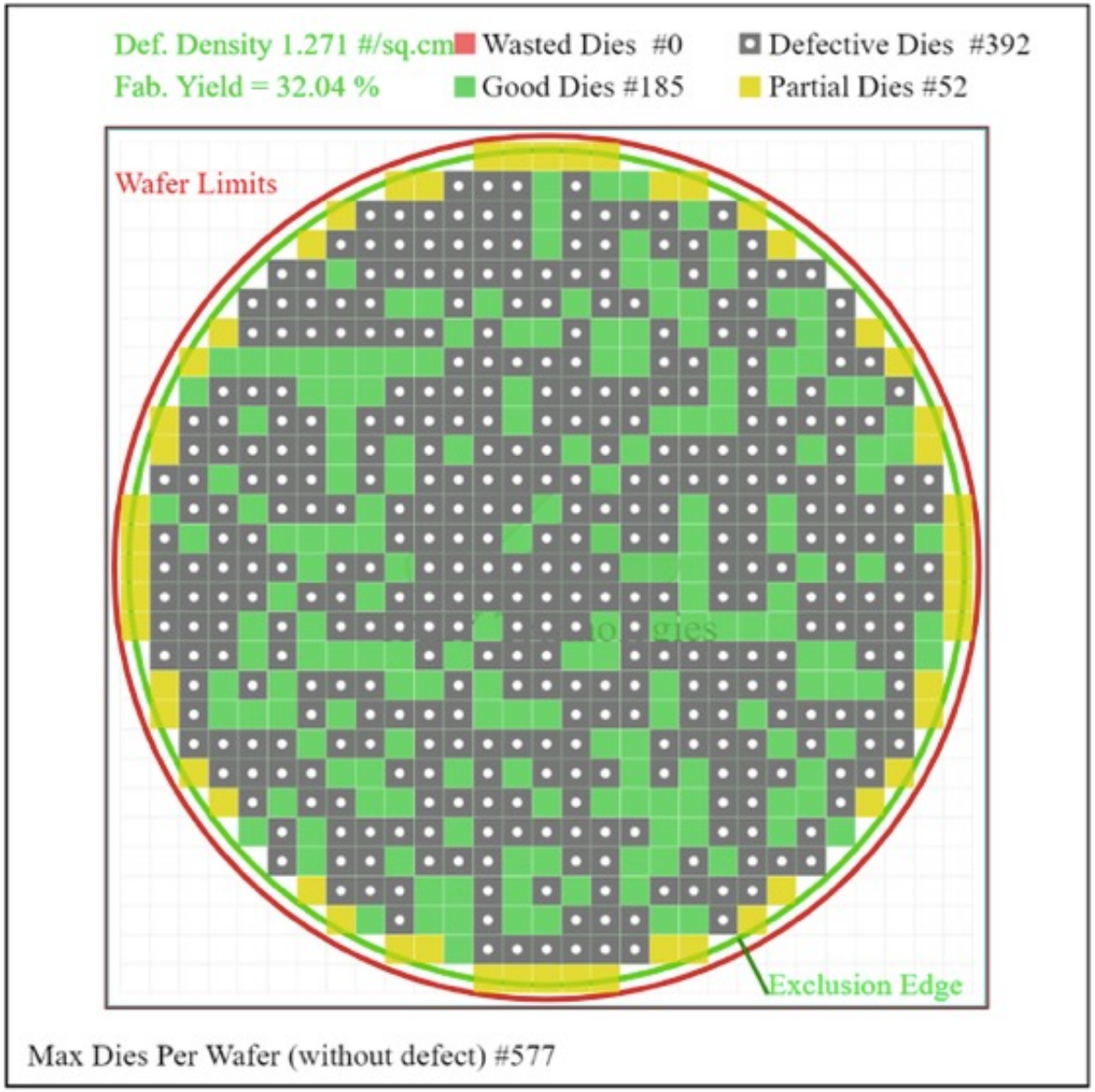

Wafers

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Quora

After taking into consideration the wasted dies intersecting the "Exclusion Edge" there are a possible 577 dies produced. In this sample, 392 have defects of some sort, leaving only 185 that can be used as intended.

Assuming these are CPU dies with integrated GPU, any defect in a GPU region can result in a CPU with the GPU disabled and be sold at a lower price. If this is a die with six CPU cores, one pair of cores can be disabled to make it a quad core. In that way, maybe half of the defective chips can be salvaged.

With say 14nm production there are fewer transistors per die, and thus a lower probability of defects as compared to 7nm production. The defect rate goes up because there simply are a lot more transistors and a lot more opportunities for a defect to occur.

The problem is greatly compounded when the die is quite large, because then the possible number of good dies per wafer goes down and the probability of getting defects goes up. GPU dies like those made by Nvidia are easier to bin because multiple compute units can be disabled and still result in a perfectly functional product.

Just as a case in point. A RTX 2080 has 46 compute units, while a RTX 2060 KO has only 30. But they both use the same TU104 silicon. The 2060 KO edition has a whopping 16 of its compute units disabled. Fully 1024 of its GPU cores are dead. You simply can't do that with CPU silicon.

Wafers

Quora

Angus Mccamant · Follow
Former Device Physics Semiconductor ICs, Metrology · Jul 3

Related **How many chips can be fabricated on a wafer? How much do companies pay per chip when buying from semiconductor fabrication plants (fabs)?**

The number of chips on a wafer is determined by the chip size. Most modern fabs use 300mm wafers which have about 70,000 square mm. As small chips can be one mm on a side for a square chip you could get 70,000 chips on one wafer.

There are complications. All wafer fabs have test devices on wafers for monitoring the process. A finished 1mm per side chip also has to have room for sawing the wafer into individual chips. The width of the saw blades results in about 100 microns (0.1mm) mandatory spacing between chips. In real life you will get more like 50,000 one mm chips on a wafer.

The fabs do not sell chips, they sell wafers. There is a minimum wafer lot size you have to order for your custom design. This results in a huge up front cost, millions of US dollars, for all the tooling, masks and prep work done to get the design ready for the fab. Many fabs, including TSMC, regularly run project wafers where you purchase only a small portion of a wafer. This will avoid much of the fixed cost as it can be shared by tens of customers. Most fab customers will run prototype chips on multiple customer project wafers before committing to buying wafer lots.

Intel Core i7 Die

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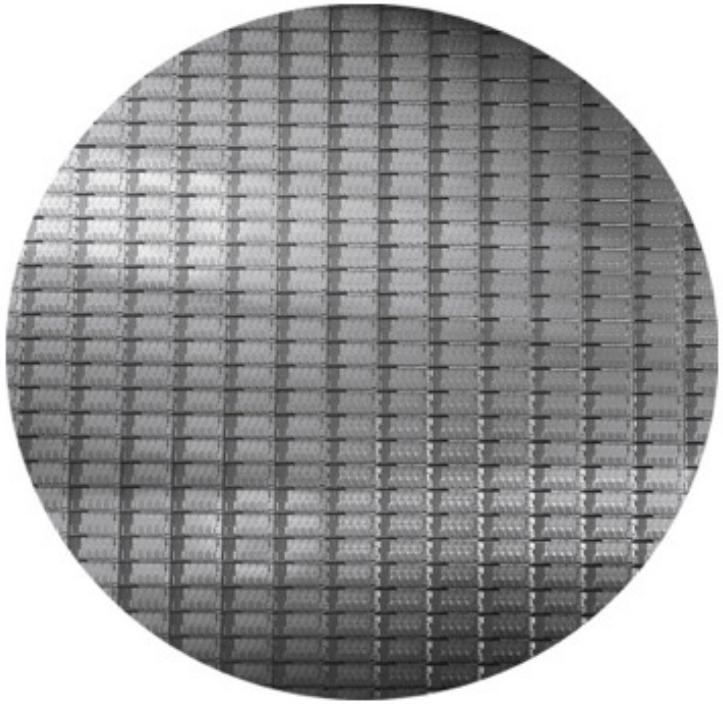
Hennessy & Patterson

Figure 1.5.2: A 12-inch (300mm) wafer of Intel Core i7 (Courtesy Intel) (COD Figure 1.13).

The number of dies on this 300 mm (12 inch) wafer at 100% yield is 280, each 20.7 by 10.5 mm. The several dozen partially rounded chips at the boundaries of the wafer are useless; they are included because it's easier to create the masks used to pattern the silicon. This die uses a 32-nanometer technology, which means that the smallest features are approximately 32 nm in size, although they are typically somewhat smaller than the actual feature size, which refers to the size of the transistors as "drawn" versus the final manufactured size.



Wafer

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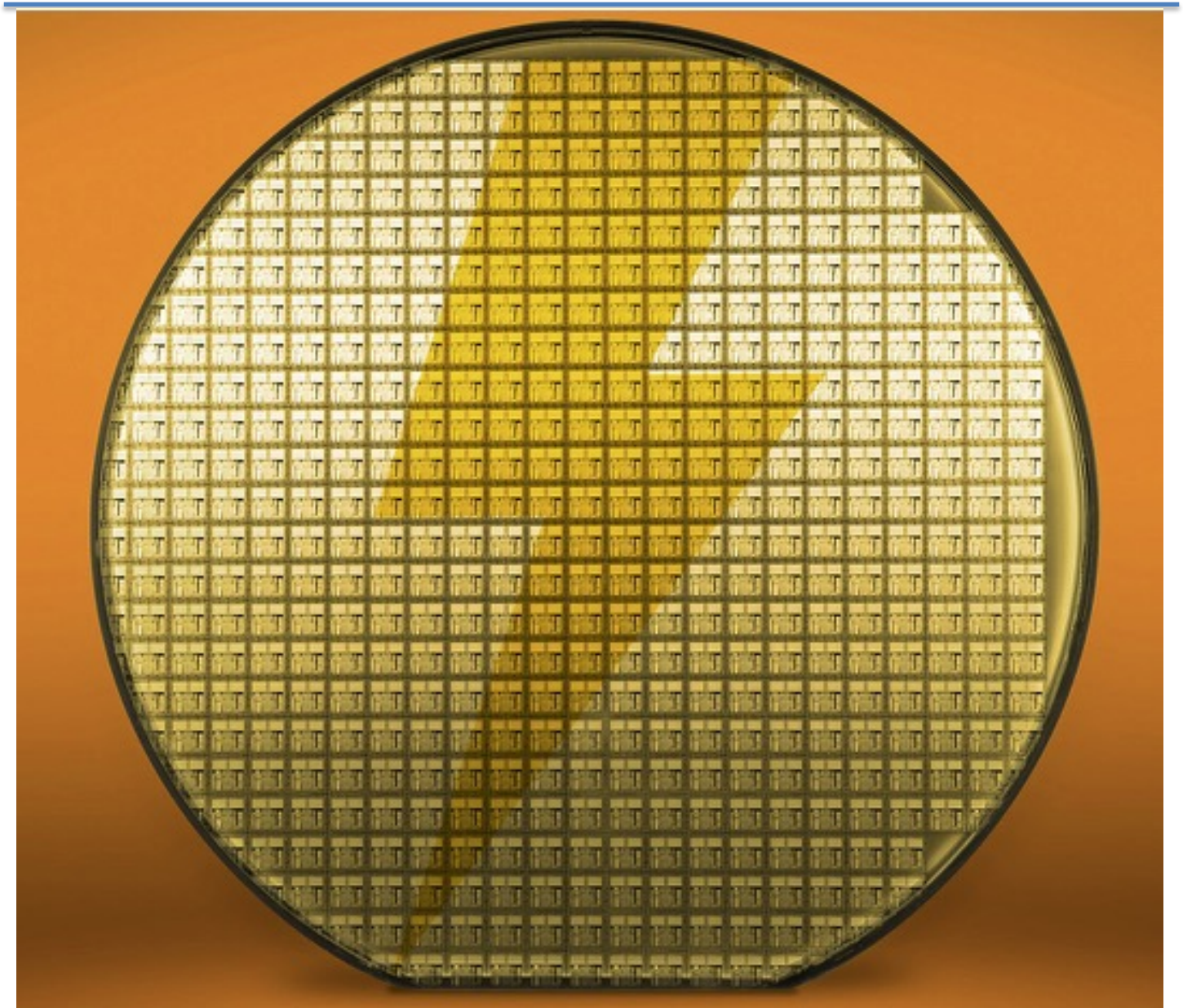

Wafers: Yield

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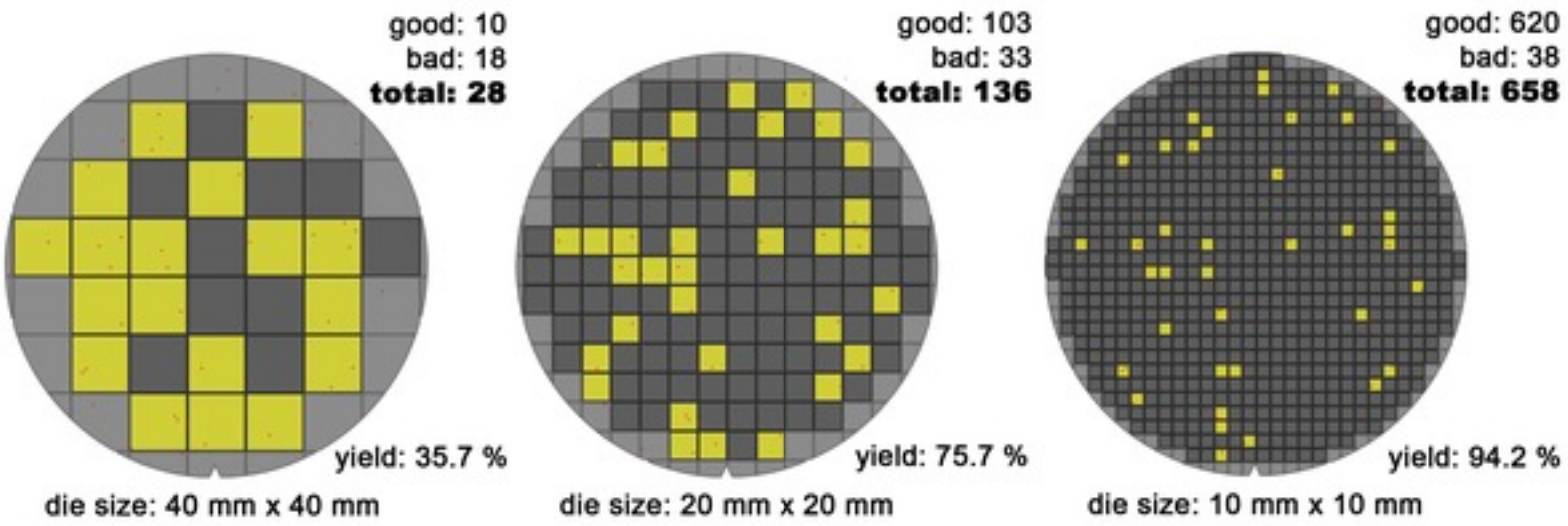

yellow shows bad dice (a function of defect density)

Wafer Fab

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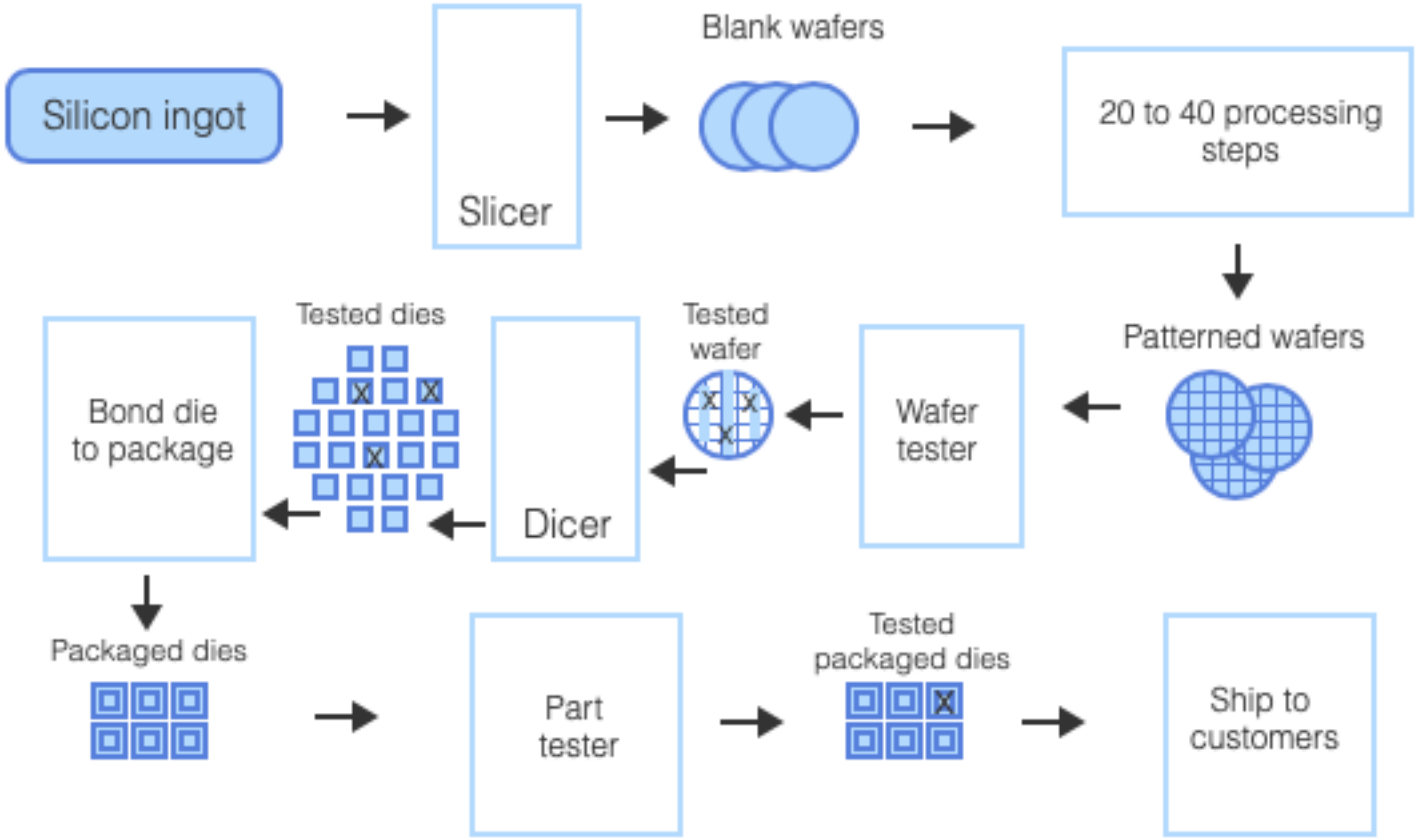
Hennessy & Patterson



Chips

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Process Nodes

MOS Transistor

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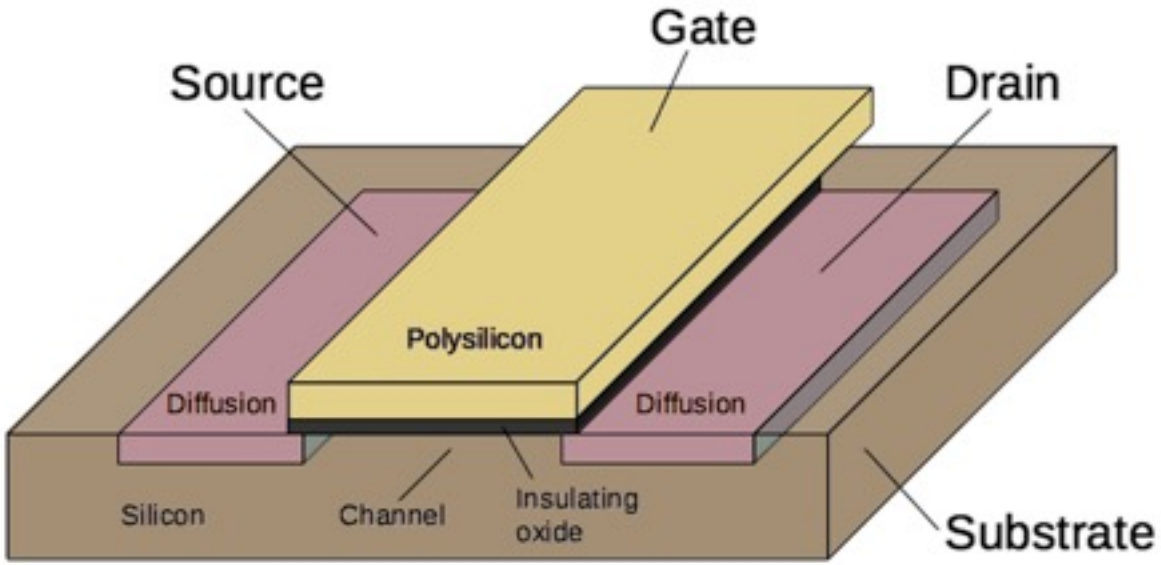
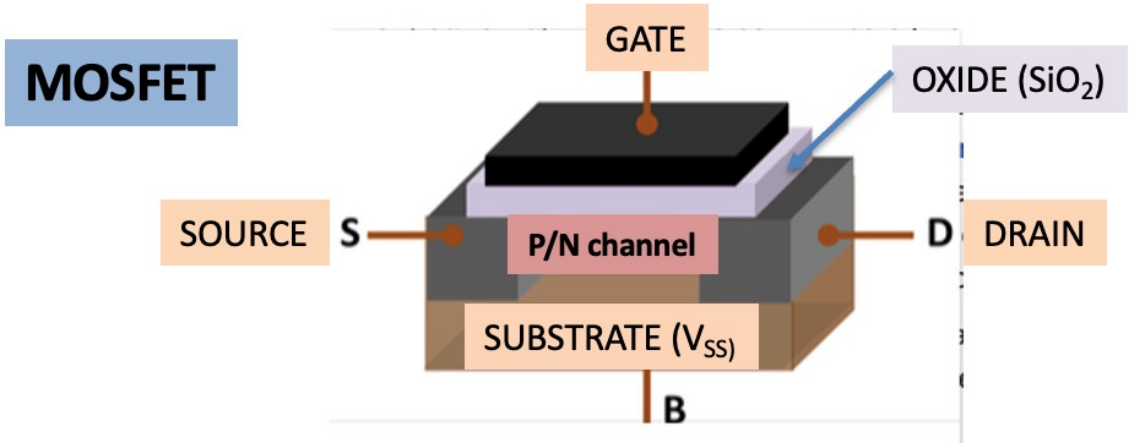
WikiSemi



Structure of a MOSFET in the integrated circuit.



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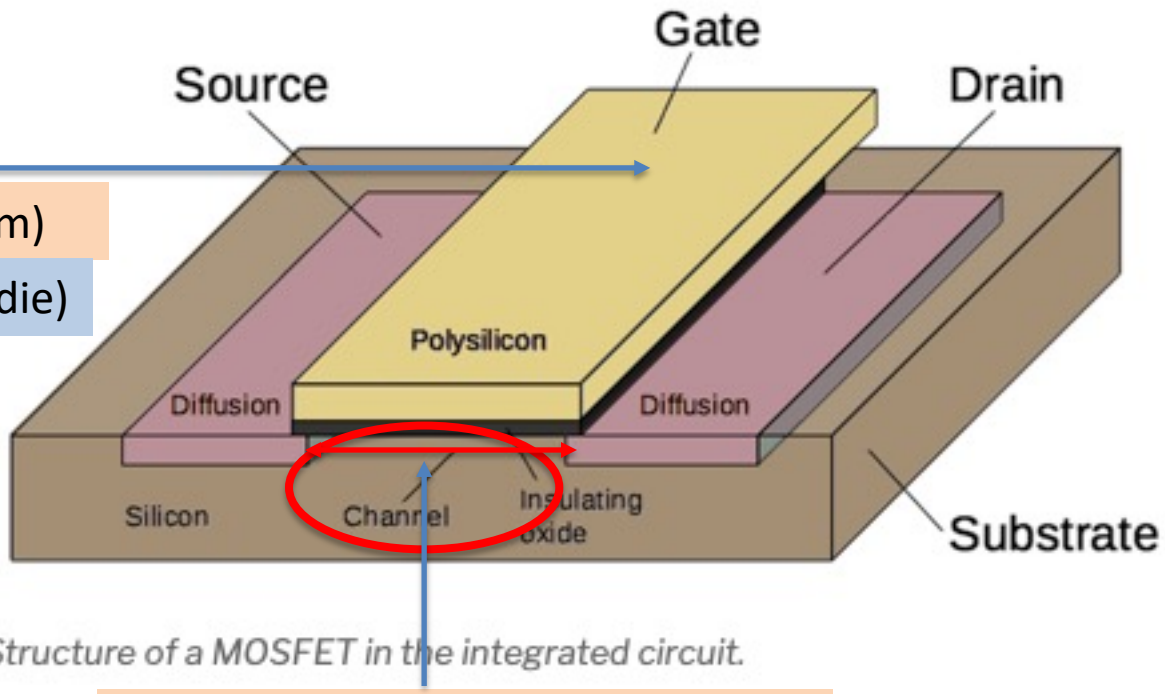
MOS Transistor

V_g = 5→3.3→1.8 V

Gate



Structure of a MOSFET in the integrated circuit.

Pitch (e.g.14nm)

Density (xtor/die)

Smallest feature size (e.g. 5nm)

Performance (F_t)

IC Process & Interface

TTL compatible — **5V → 3V**

❖ *Bipolar*

5V

➢ RTL→DTL→TTL → *Schottky* TTL→ *LS* TTL

1960	1965	1970	1975	1980	1985	1990

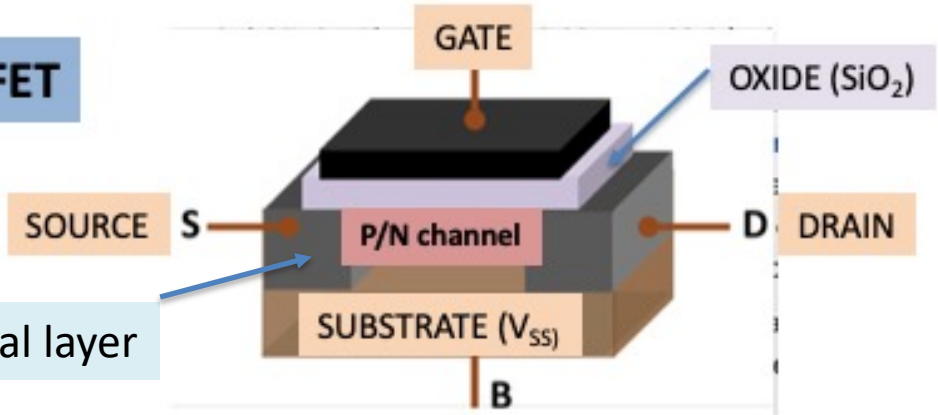
❖ *MOS*

➢ PMOS→NMOS → **CMOS** → CMOS (TTL I/O)→ 3.3V

5V → 3V

BiCMOS

MOSFET



Epitaxial layer

The **metal–oxide–semiconductor field-effect transistor**, also known as the **metal–oxide–silicon transistor**, is a type of field-effect transistor that is fabricated by the controlled oxidation of a semiconductor, typically silicon. It has an insulated gate, whose voltage determines the conductiv

MOS Transistors

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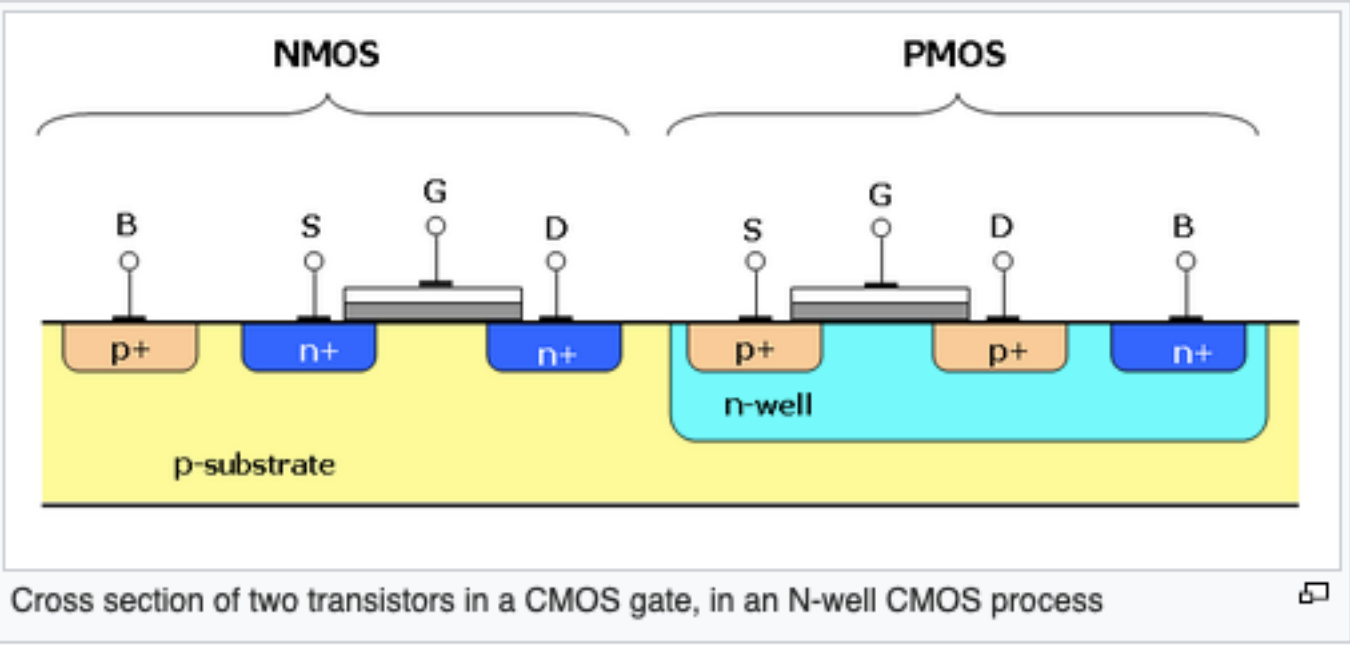
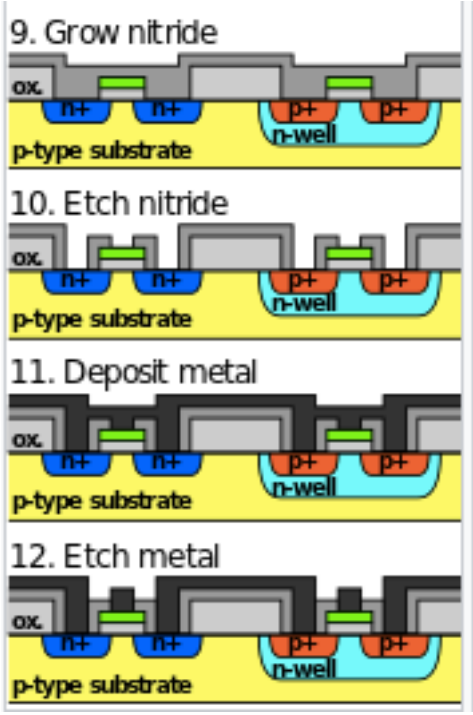
MOSFET



Cross section of two transistors in a CMOS gate, in an N-well CMOS process



Last 4 steps

MOS Transistors

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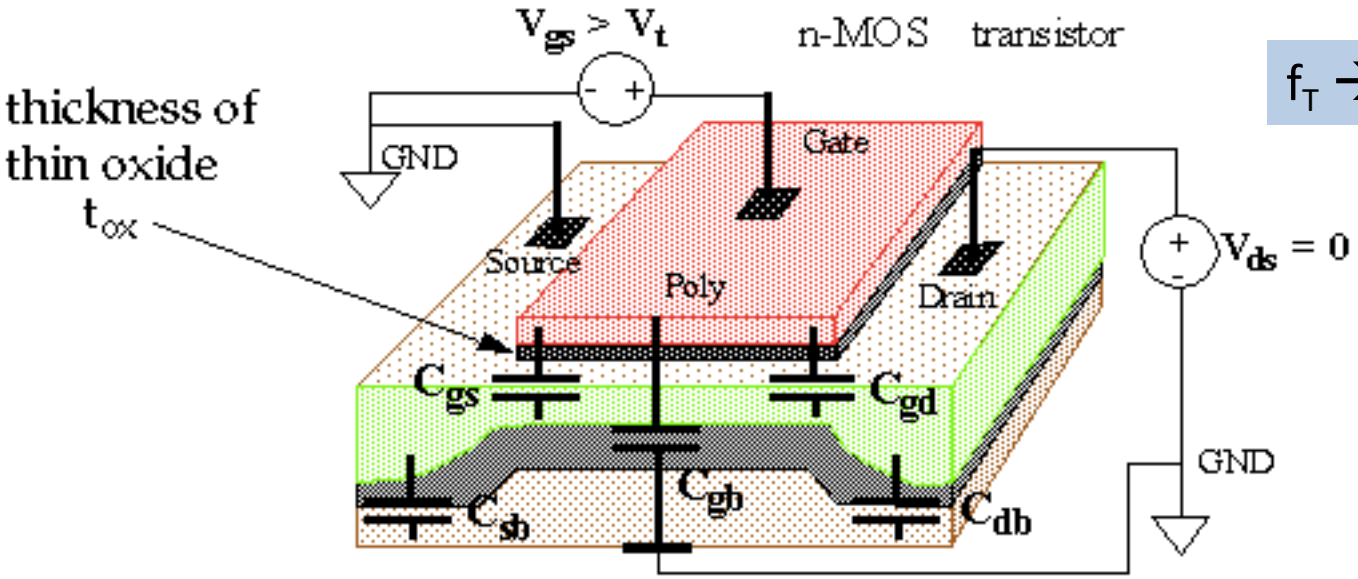
The channel will have a length (distance from one electrode to the other) and a width (imagine this diagram coming out of the screen). The electrodes have geometries. The gate doesn't always span the full width of the channel and is its own critical dimension.

The sizes of each of these things are critical dimensions. They all have an effect on the performance of the device because they will contribute parasitic capacitance and resistance.

Parasitic capacitances



$f_T \rightarrow$ lengths

Parasitics depicted by University of New Mexico

Chip Fab

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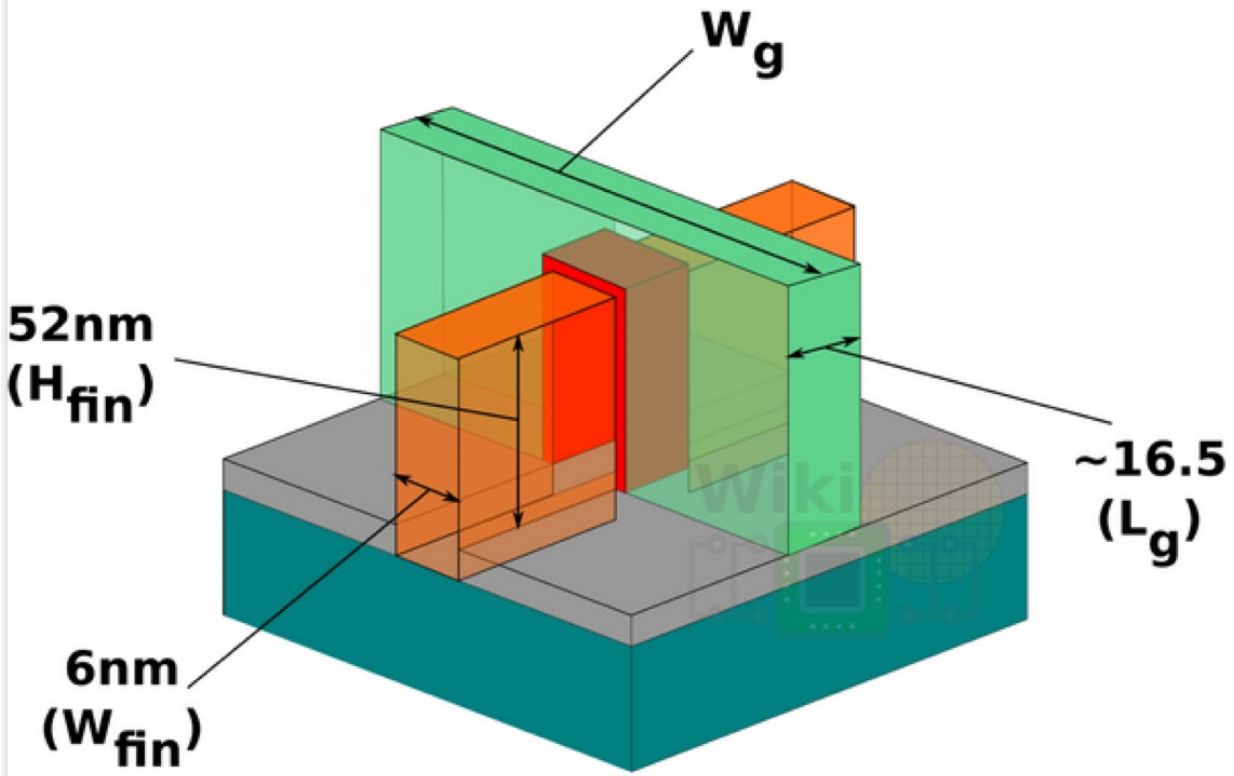
7 nm **TSMC**

What's a 5nm FinFET transistor look like?

Well... I didn't find a good pic for 5nm, but I found a pic for 7nm here:



We can assume 5nm is slightly smaller on all axes.

The first thing to note is that the gate length (L_g) is 16.5nm. The width of the gate will vary, but I am going to go out on a limb and guess it is no smaller than $3W_{\text{fin}}$, or 18nm. And the overall structure is tall: 52nm plus another few nm

New Processes

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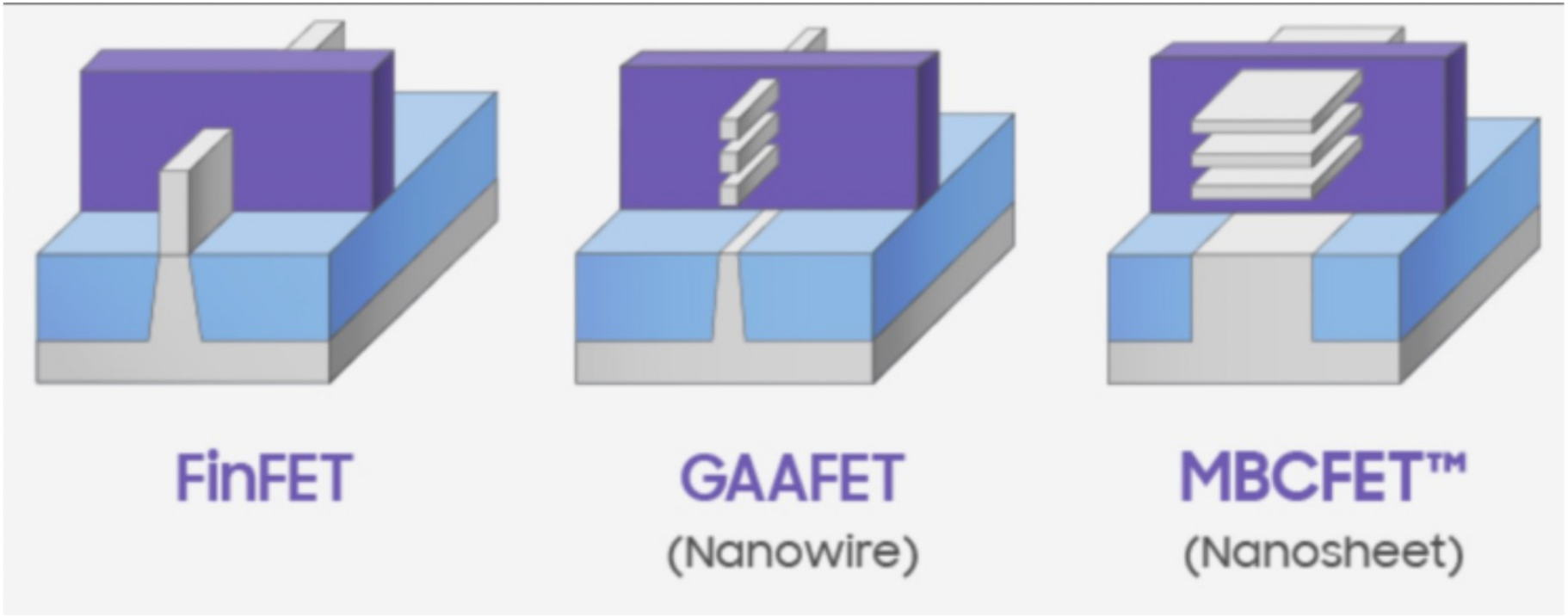

New Nodes: IBM 2nm

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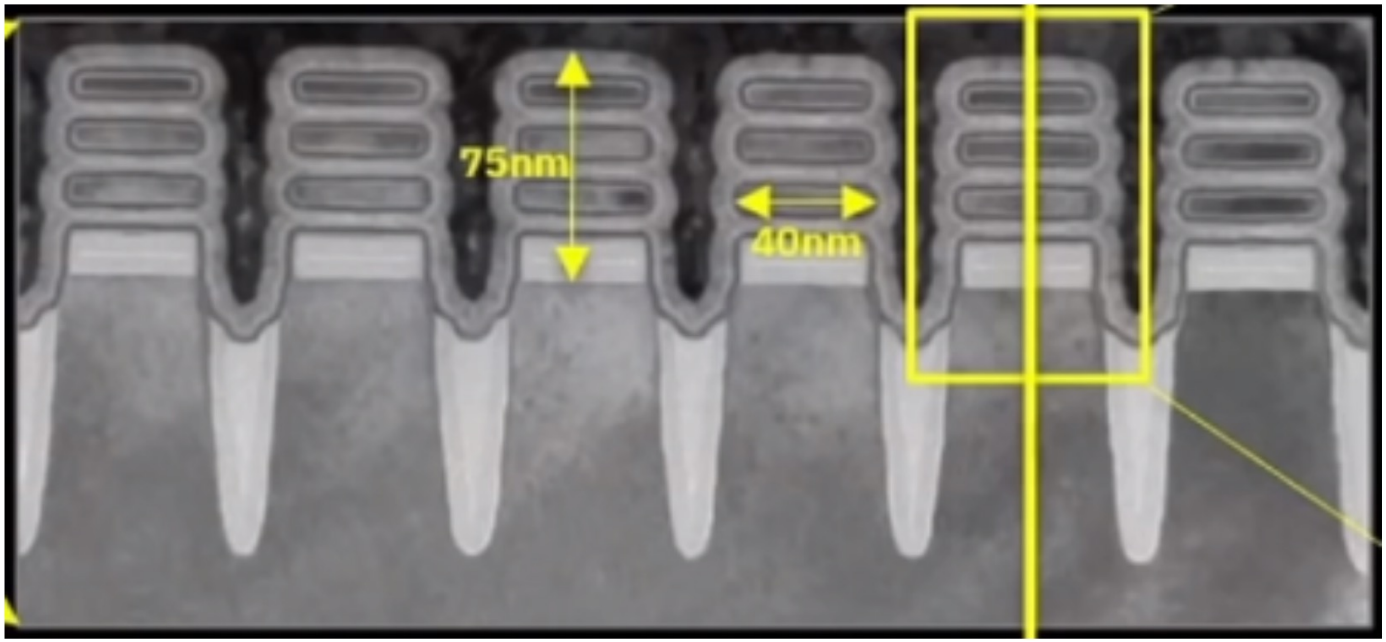

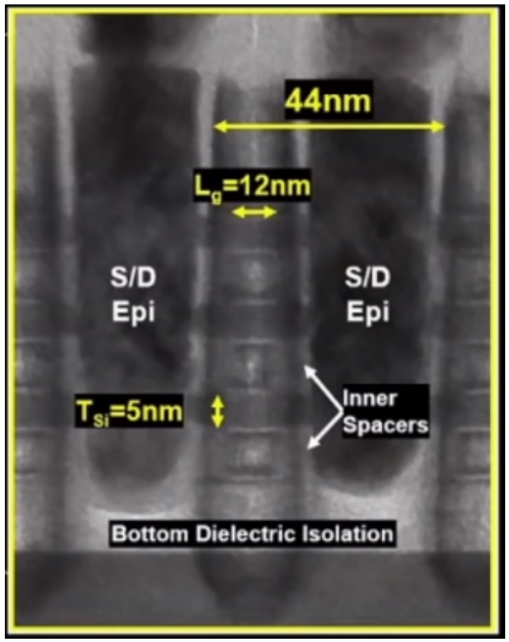

Images of IBMs 2nm Chip architecture

TSMC Making 3nm

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Jeff Drobman

12-2-21

TSMC Begins Pilot Production of 3nm Chips: Report

By Anton Shilov 3 days ago

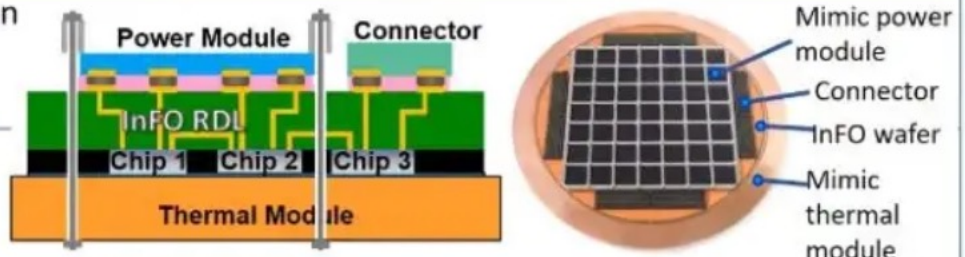
TSMC's N3 enters risk production.

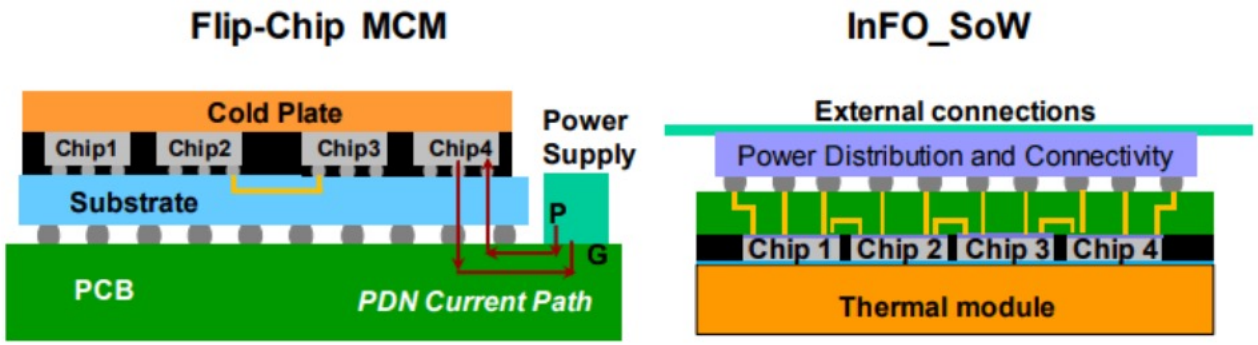
Taiwan Semiconductor Manufacturing Co. has started risk production of chips using its N3 (3 nm-class) fabrication process, two reports from Taiwan read. As usual, it will take the contract maker of chips and its partners several quarters to polish off the technology and designs before both enter high-volume manufacturing (HVM).

TSMC initiated pilot production of N3 chips at its Fab 18 at the Southern Taiwan Science Park near Tainan, according to reports from DigiTimes and TechTaiwan. HVM of chips using the new node will commence in the second half of the year, but since cycle time for the new process is over 100 days, the first N3 chips made by TSMC will ship in early 2023.

TSMC

Index	Key Advantages of InFO_SoW- Higher compute density & faster training time
Electrical Performance	✓ Low latency C2C communication ✓ High bandwidth density ✓ Low PDN impedance
Cost & Yield	✓ Mature InFO process ✓ Known-good chip ✓ Heterogeneous integration



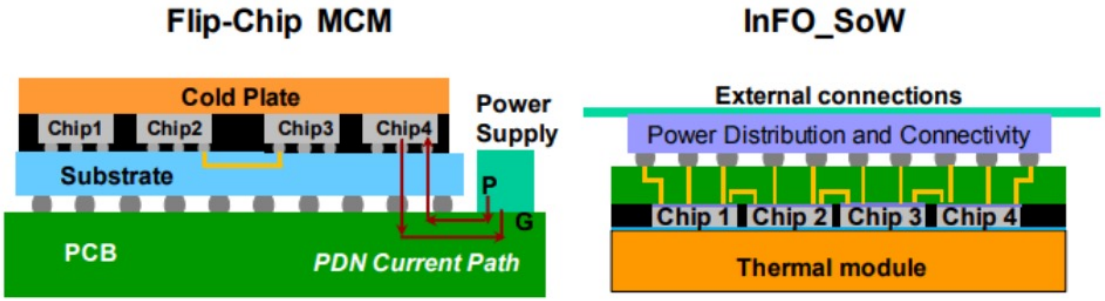


Line width / space (μm)	10 / 10	5 / 5
Line density	1x	2x
Bandwidth density	1x	2x
PDN impedance	1x	0.03x

Fig. 2. Electrical performance comparison between Flip-Chip MCM and InFO_SoW

TSMC

This breaks through the current barriers with multi-chip modules. With an interposer-based technology such as Nvidia datacenter GPUs, they are limited by interposer manufacturing limits. TSMC's 5th generation CoWoS-S recently went into mass production with interposers that are 3x the reticle limit. The reticle limit is 26mm by 33mm and is associated with the maximum area a lithographic machine can pattern in one instance. This method involves reticle stitching and other manufacturing difficulties because the interposer is a silicon chip itself. This type of packaging has limitations in scaling the number of chips for huge AI workloads.



Line width / space (μm)	10 / 10	5 / 5
Line density	1x	2x
Bandwidth density	1x	2x
PDN impedance	1x	0.03x

Fig. 2. Electrical performance comparison between Flip-Chip MCM and InFO_SoW

Process Timeline

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INDIE APP DEVELOPER
Jeff Drobman

Recent Timeline:
2018 - Apple ships first 7nm consumer processor (TSMC), AMD later follows suit (TSMC), Intel stuck on 14nm. Samsung debuts 7nm.
2019 - Samsung and TSMC both begin offering 5nm. TSMC samples Apple 5nm processors.
Apple
2020 - Apple ships first 5nm consumer processor (TSMC), AMD expected to follow soon. Intel begins shipping 10nm (laptop) processors in earnest, desktop 10nm expected before 2021.

From 5nm it goes: 5nm → 3nm → 2.1nm → 1.5nm → 1.0nm = 4 shrinks left.
[IRDS roadmap: IEEE Releases Expansive 2018 Roadmap for Devices and Systems]

Remember the marketing problem?
Intel
Intel's 10nm process is considered to be comparable with TSMC's 7nm process. So Intel's roadmap may be a little more indicative of how many shrinks we have left.
10nm → 7nm → 5nm → 3nm → 2.1nm → 1.5nm → 1.0nm = 6 shrinks left.

TSMC vs Intel Nodes

Intel Versus TSMC Nodes and Timing

	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027
TSMC											
- Node	7	7/7+	5	5	3	3	2	2	1.5	1.5	
- Status	Risk	Full	Risk	Full	Risk	Full	Risk	Full	Risk	Full	
Intel											
- Node	14	14	10	10SF	10SF	7	7	5	5	3	3
- EN	13.8	13.8	7.1	7.1	7.1	4.1	4.1	2.4	2.4	1.3	1.3
- Status	Full	Full	Full	Full	Full	Ramp	Full	Ramp	Full	Ramp	Full

- Risk = risk starts, Ramp = production ramp, Full = full production, EN = TSMC equivalent node.
- TSMC is assumed to stay on a new node every two years with shrink similar to the 5nm and 3nm announced shrinks.
- Intel 5nm and 3nm are assumed to be on two year intervals and to be 2x density improvements consistent with the announced 7nm density shrink.

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TSMC vs Intel Nodes

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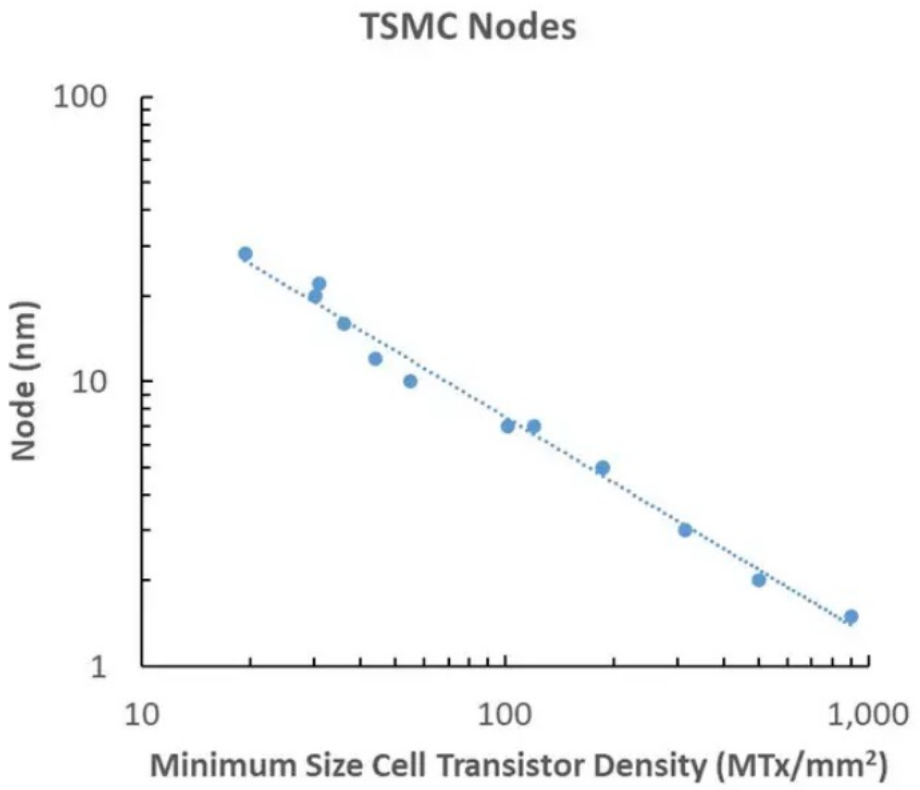
TSMC Nodes

- TSMC nodes versus transistor density.
- 28nm through 5nm are actual.
- 3nm is projected based on TSMC announcements.
- 2nm and 1.5nm are IC Knowledge projections.



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Semicon News

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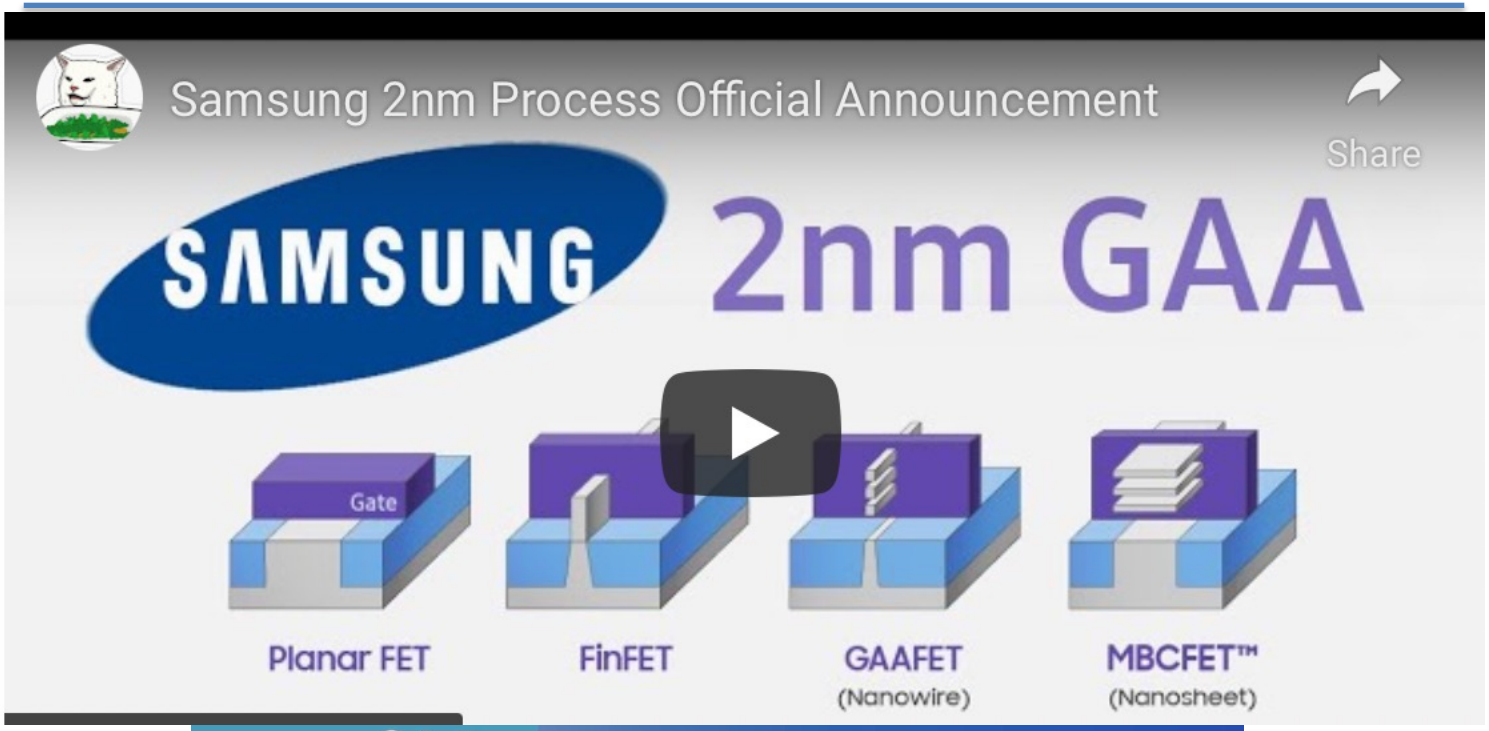

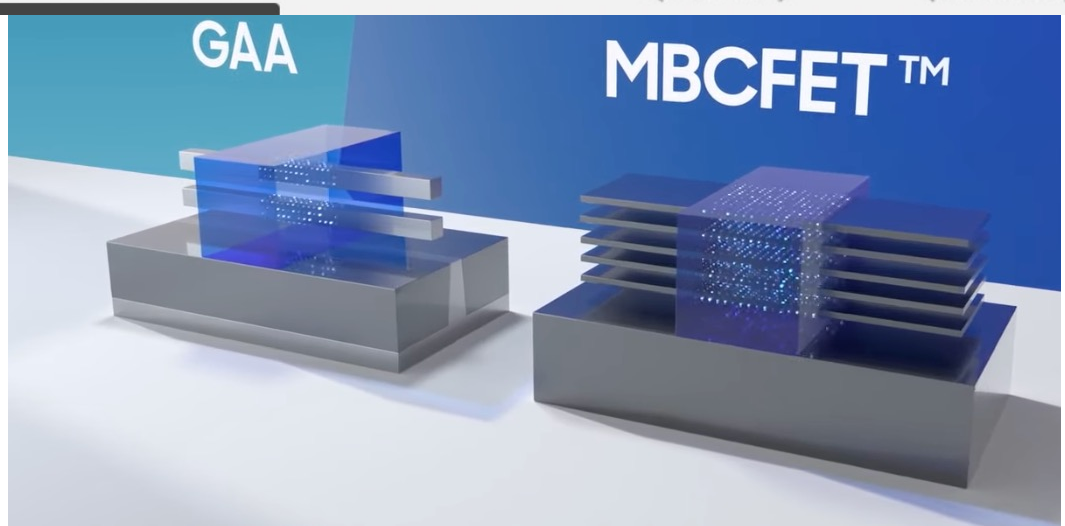

Tesla at TSMC

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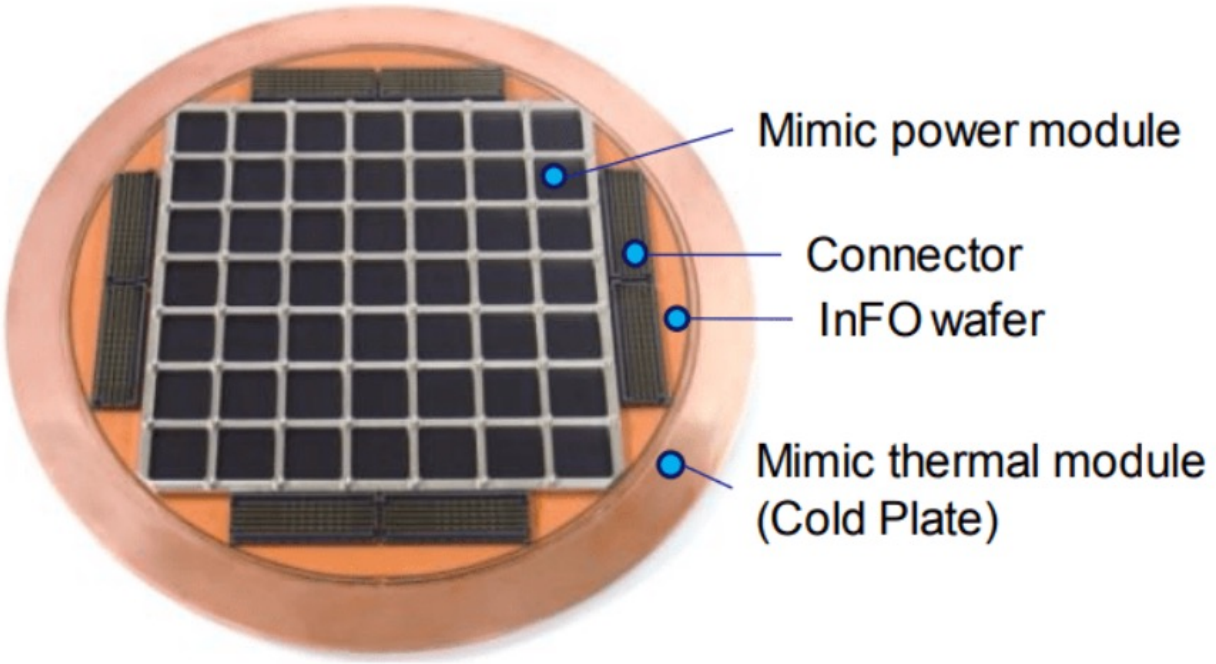

Fig. 10. InFO_SoW system assembly demonstration

This image looks remarkably similar to the Tesla chip and offers some insights. Just like the tesla image, there is a cold plate. Various chips arrange in a grid, an InFo Wafer, and connectors. The structures look to be a 1 to 1 match but the exact details them look to be slightly different than the initial TSMC research.

Tesla at TSMC

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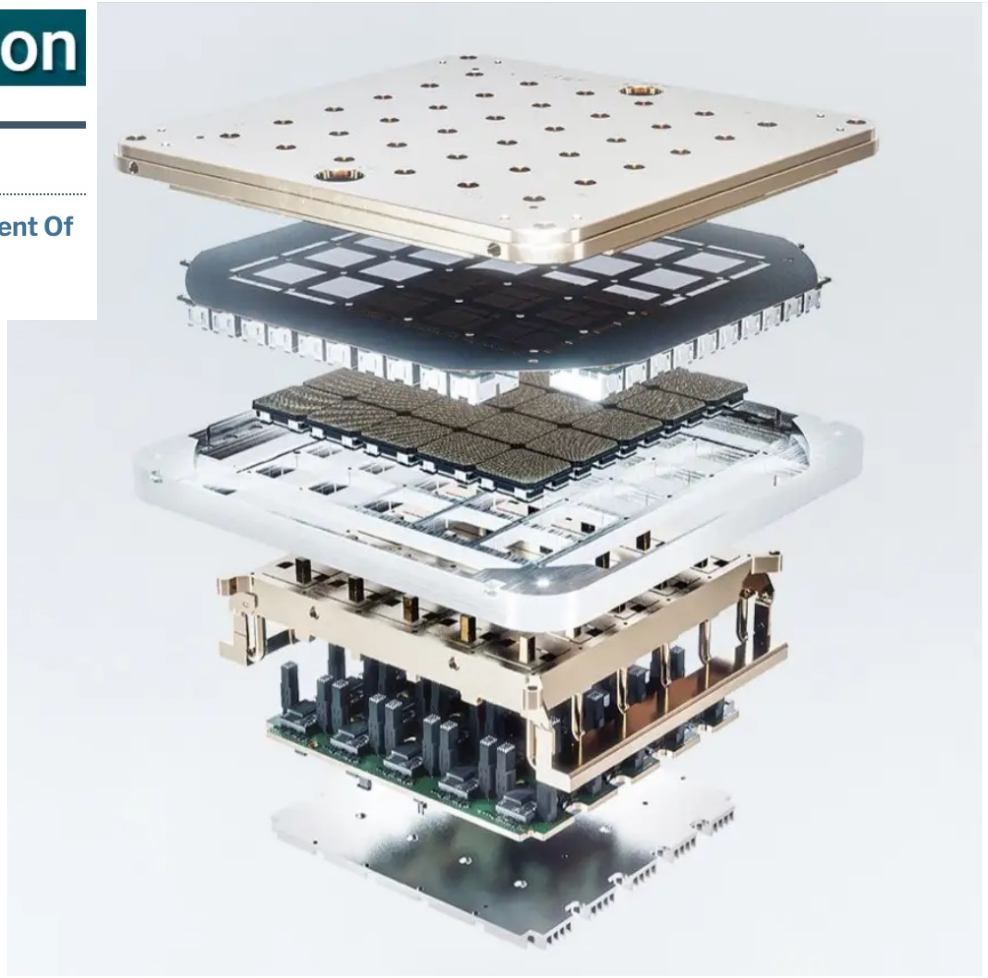
TSMC's Chiplets Integration

TSMC

Tesla AI Day Supercomputer Chip Teaser | Is This The First Deployment Of TSMC InFO_SoW?

by Dylan Patel on 08-08-2021 at 10:00 am
Categories: Events, Samsung Foundry, TSMC



At first glance it looks like there is a carrier, heatsink, and power delivery. The most interesting part of course, is the chips. It has a large array of BGA solder pads and a 5×5 array of chips. This type of packaging looks incredibly unorthodox and the only thing we can think of is TSMC's integrated fan out system on wafer technology (InFO_SoW). Here is the link to the paper on IEEE.

Chip Cooling

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SEMICONDUCTORS AND ELECTRONICS | RESEARCH UPDATE

New semiconductor cools computer chips

05 Aug 2021 Isabelle Dumé

A novel semiconducting material with high thermal conductivity can be integrated into high-power computer chips to cool them down and so improve their performance. The material, boron arsenide, is better at removing heat than the best thermal-management devices available today, according to the US-based researchers who developed it.

BAs = boron arsenide

III-V semi

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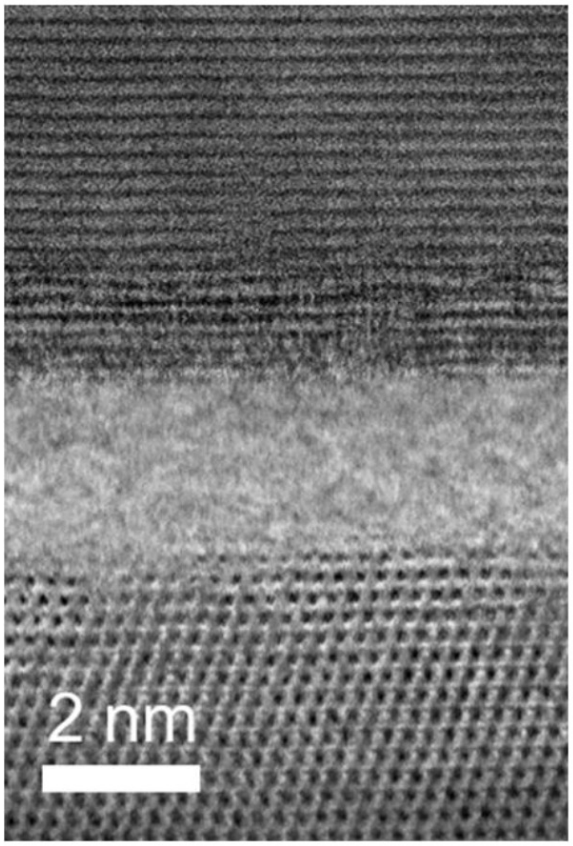

An electron microscopy image of a gallium nitride-boron arsenide heterostructure interface at atomic resolution. Courtesy: The H-Lab/UCLA

The size of computer chips has been shrinking over the years and has now reached the nanoscale, meaning that billions of transistors can be squeezed onto a single computer chip. This increased density of chips has enabled faster, more powerful computers, but it also generates localized hot spots on the chips. If this extra heat is not dealt with properly during operation, computer processors begin to overheat. This slows them down and makes them inefficient.

Defect-free boron arsenide

Researchers led by Yongjie Hu at the University of California, Los Angeles, recently developed a new thermal-management material that is much more efficient at drawing out and dissipating heat than other known metals or semiconducting materials such as diamond and silicon carbide. This new material is known as defect-free boron arsenide (BAs), and Hu and colleagues have now succeeded in interfacing it with computer chips containing wide-bandgap high-electron-mobility gallium nitride (GaN) transistors for the first time.

Chips

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Metal Interconnect

Metal Interconnect

Quora

Aluminum → Copper → Cobalt

Jeff Drobman, Lecturer at California State University, Northridge (2016-present)

a little elaboration. the top layer of all IC's have been the metal interconnects, which have gone from 1 layer to 4 layers to 8 or more — similar to PCB's. aluminum has been used due to cheap and easily vaporized for vapor deposition through masks. copper is a better conductor, but more expensive and harder to deposit. a few manufacturers have used copper, such as IBM. Note that the metal pitch has to match the transistor pitch (now about 10–14nm).

Jerry Coffin · 25m ago

Copper interconnect was introduced 25 years ago, and has been in widespread use for over 20 years now. Intel recently started using Cobalt for the first couple of layers.

As far as layer count goes: around a dozen is now pretty common.

Jeff Drobman · Just now

thank you for the information. I know copper was first used in the 1980's, with IBM a leader. I don't think it has ever been "widespread", with aluminum being the bulk of use. I have not heard of cobalt being used for metal, and I don't understand why it would: cobalt is more than 2x the resistivity of aluminum (62.4 to 26.5 nOhm-m). maybe it is used for its hardness against heating?

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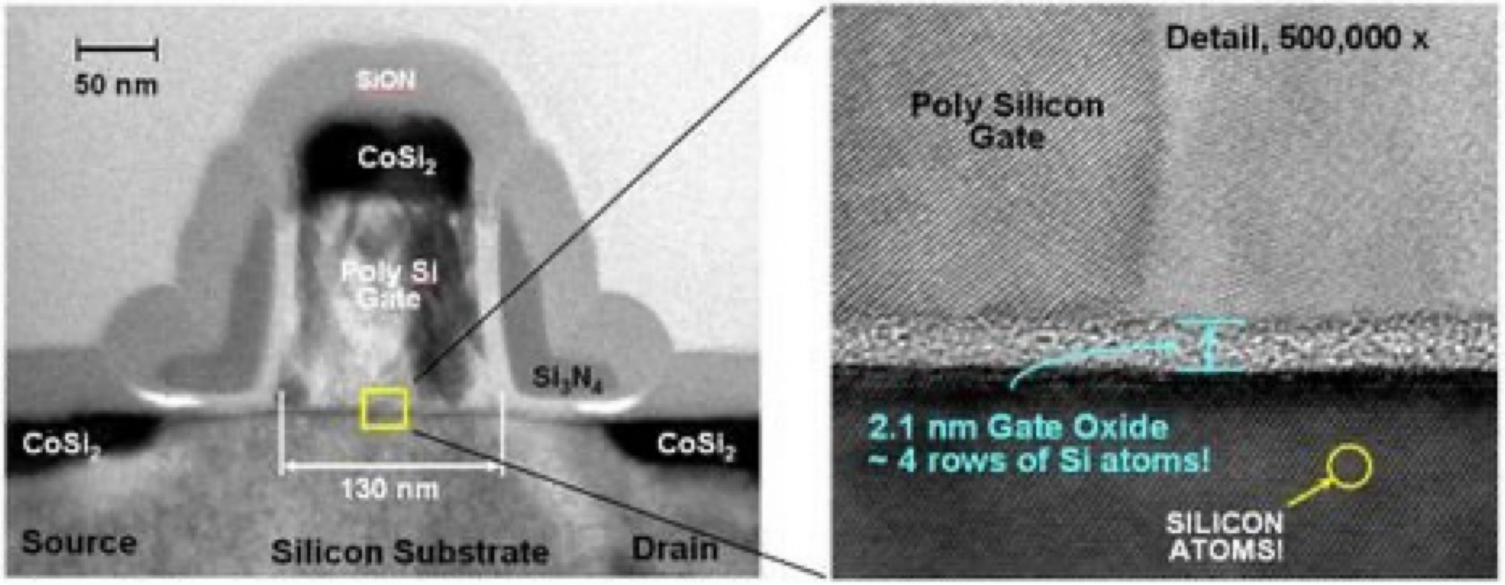
Figure 1 - Electron Micrograph of CMOS FET Cross Section



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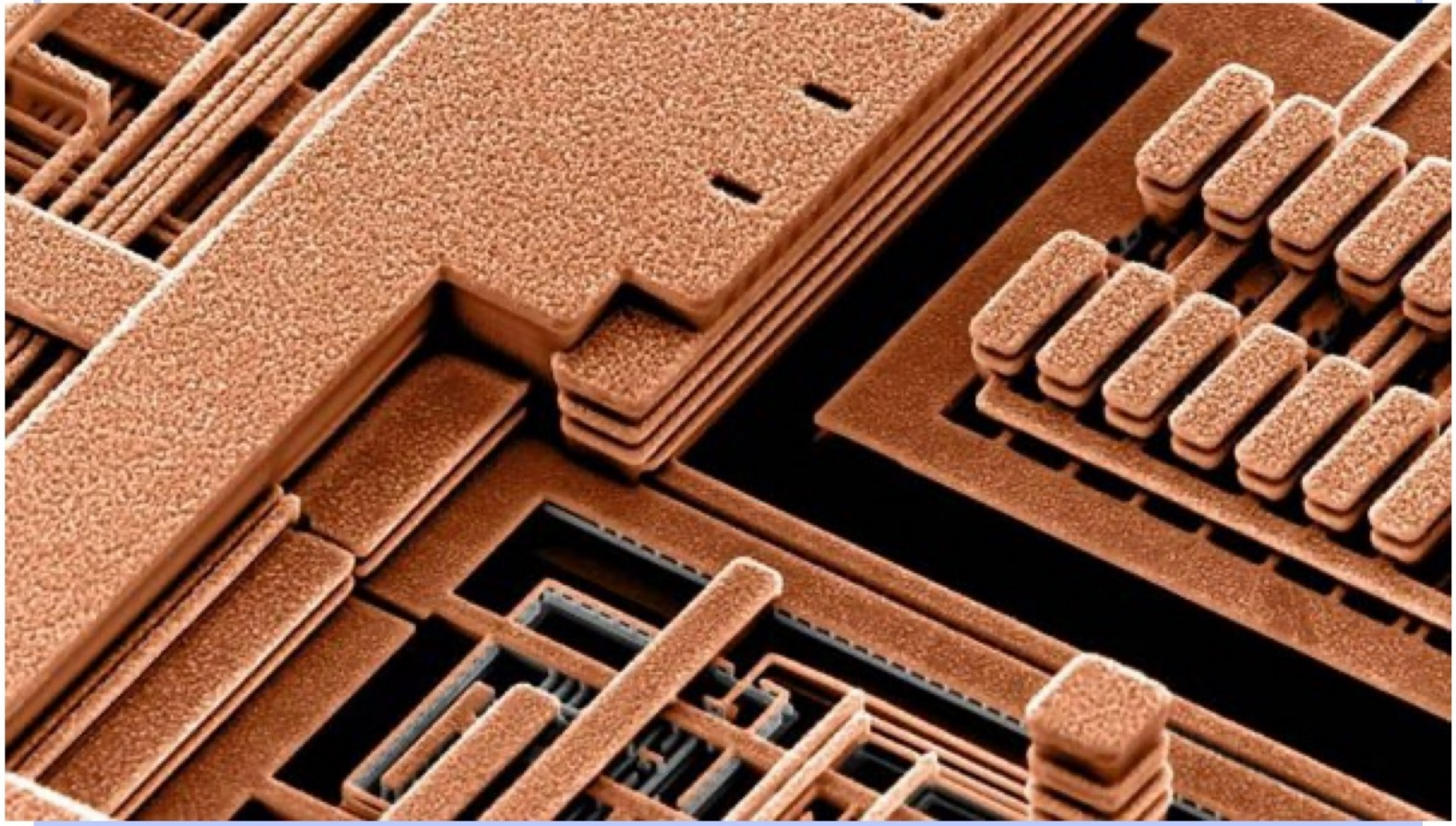
The transistors connect to each other using metal wires called interconnects. There are several layers of them (more then 8). Usually the space between them is filled with an insulator to provide structural rigidity, and expel air which can expand when heated and damage the chip, but IBM very kindly took the insulator out of one of their chips to show what the interconnect looks like:



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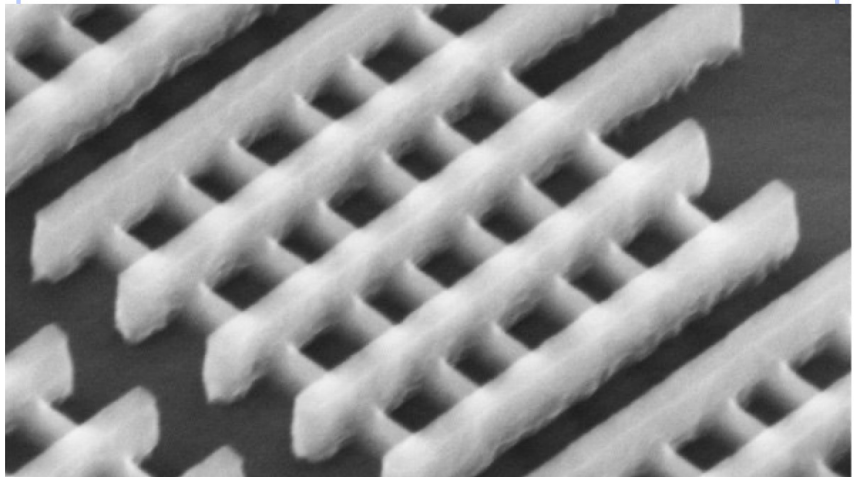
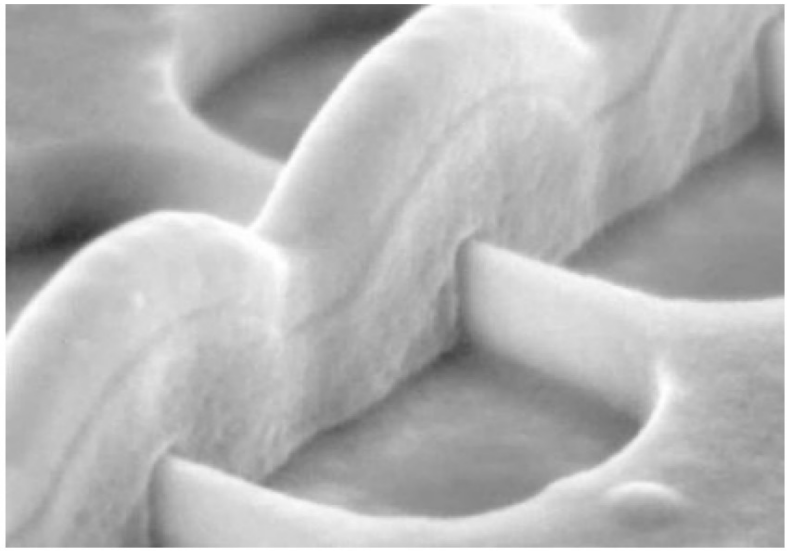
This is cross section of an old school planar transistor. Intel now uses 3D transistors called Fin-FETs which look like this:



TSMC is getting there with this:



Jeff Gruszynski · Follow
Worked at Intel (company)

Quora

Metal Interconnect

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Aluminum → Copper → Cobalt

Cobalt is already used as a copper barrier layer. What's unique with Intel is using it as a conductor for an entire metal layer.

The main reason for cobalt over copper is that at ~20 nm pretty much all materials stop behaving like their macroscopic forms with dimensions above 20 nm in terms of physical properties. This is a large part of what "nanotechnology" is about exploiting: everything changes at low nanometer scales of physical dimension.

The reasons are that grains and crystal structures start to reach their limits as "statistical mechanics"-described materials and they transition to being primarily described by only pure quantum mechanics. Mathematically this is a huge transition. And in terms of control of outcomes, it's also huge.

So it turns out that copper ceases being "one of the best electrical conductors" at these dimensions. And somewhat bizarrely, cobalt is better. Even when at macroscopic (human dimension) sizes, cobalt is not a particularly good electrical conductor. Not bad but there's a long list ahead of it (copper is 5x more conductive than cobalt in macro-scale dimensions):

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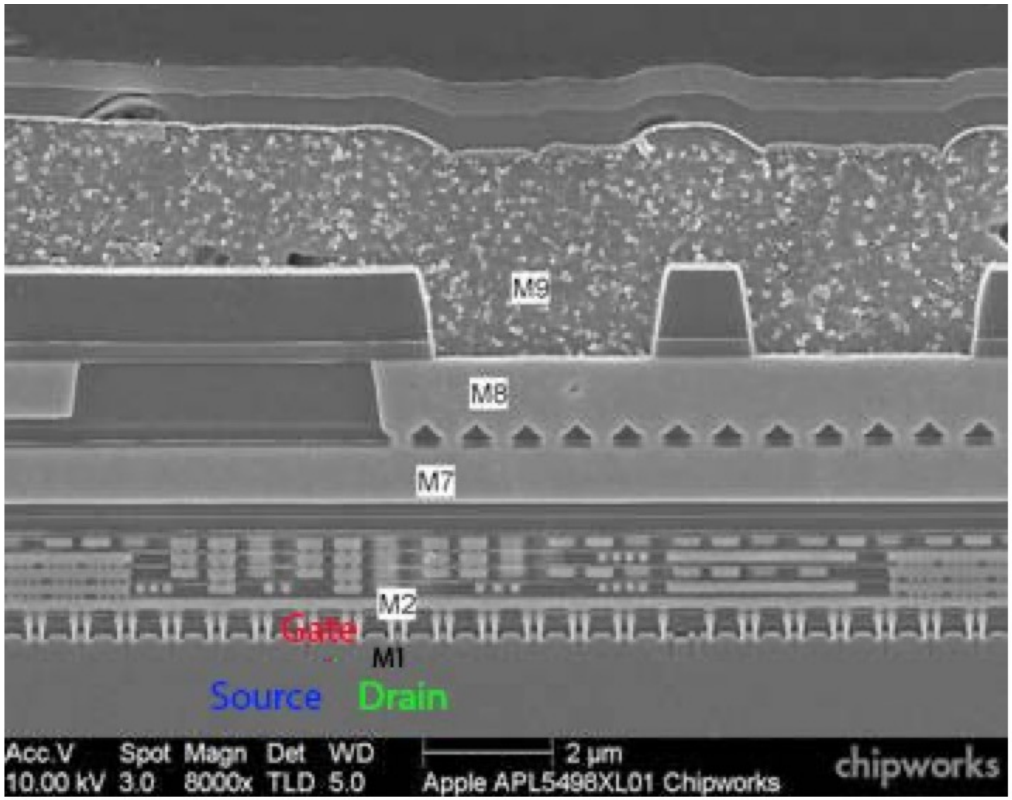
Aluminum → Copper → Cobalt

But now we are at physical dimensions of ICs where this nanoscale difference becomes important so it's out with copper and in with cobalt if you want to achieve thinner metal lines.

But why is that only now a problem? Here's the dirty little secret about metal lines: even in a 7 nm process, the metal interconnects are generally equal or larger than 30 nm. You can see this fact in this electron microgram:



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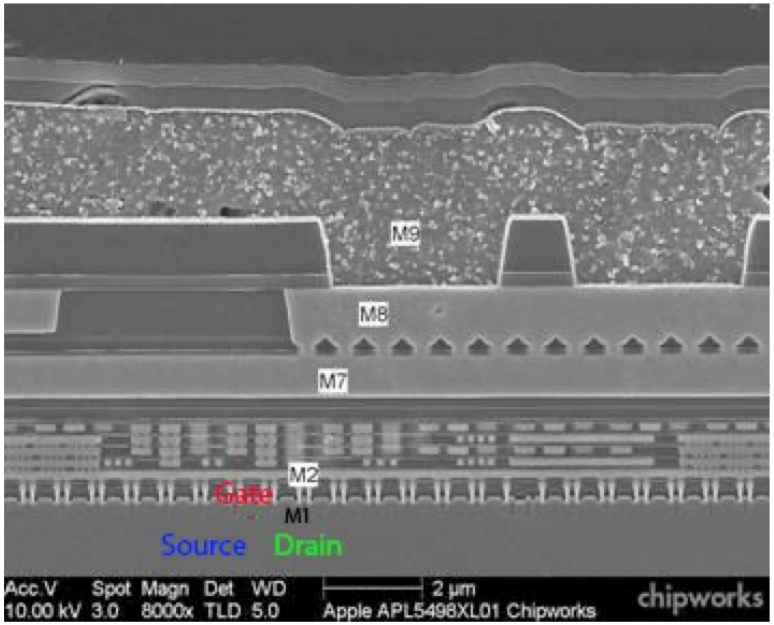
Aluminum → Copper → Cobalt



I've added the approximate location and size of a transistor's key terminals. They are actually smaller at the labeled scale but I was at single pixels in the original image.

The main reason for have 9 levels of metal is because of this line width limit and how it limits packing density. At the bottom you can "see" the transistors being tiny and existing

Instead you need to "cross over" other metal lines more to achieve decent packing density. And to do that you need more metal layers that are wider and wider (as power supply currents accumulate under Kirchoff's Current Law).

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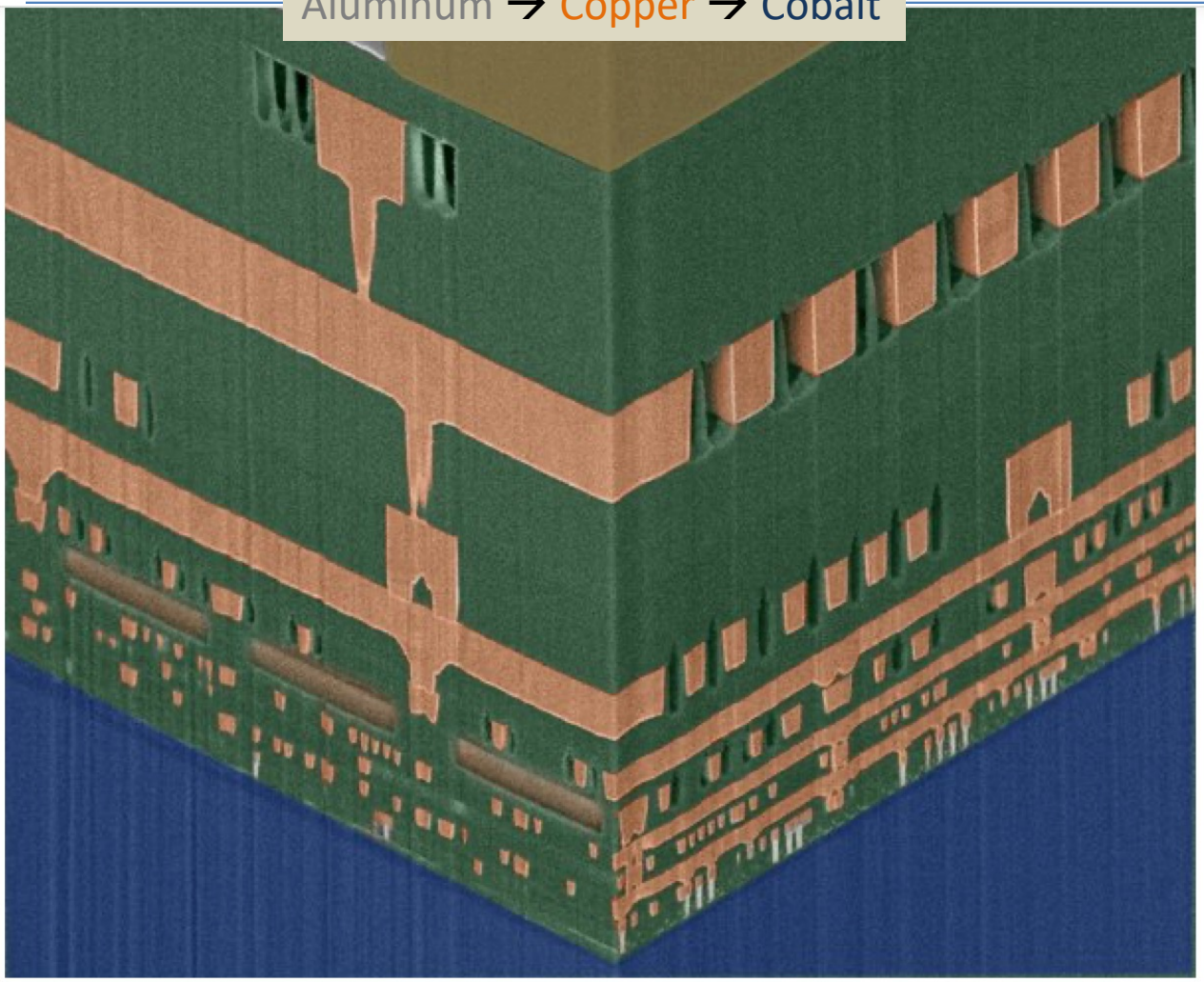

So simply having a 7 nm transistor does NOT mean you can actually pack everything as tight as you want/like (to 7 nm or some smallish multiple between transistors, for example). The metal lines minimum dimensions dictate how tight you can actually pack things. And that minimum dimension is limited by a failure mode called electromigration.

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Aluminum → Copper → Cobalt

So simply having a 7 nm transistor does NOT mean you can actually pack everything as tight as you want/like (to 7 nm or some smallish multiple between transistors, for example). The metal lines minimum dimensions dictate how tight you can actually pack things. And that minimum dimension is limited by a failure mode called electromigration.

And this density problem what Intel is trying to address with full cobalt Metal 1 (the lowest bottom metal). Cobalt is better behaved and gives better performance below 20 nm line widths. Copper won't cut it.

Except switching a material so radically is really, really hard because now you have new issues. Primarily reliability issues: i.e. how long will the material remain operating and positioned as originally manufactured assuring the same performance years later as the first day it was made. The real world is not a static thing - everything is in constant change though often slowly. You start dying the day you are born!

When we switched to copper from aluminum, numerous new and unexpected failure modes occurring only with copper were discovered which took time to solve/mediate. It's only more difficult once it's no longer a statistical mechanics problem but instead a quantum mechanics problem. Radically more difficult!

Chips

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Packaging

Chip Packaging

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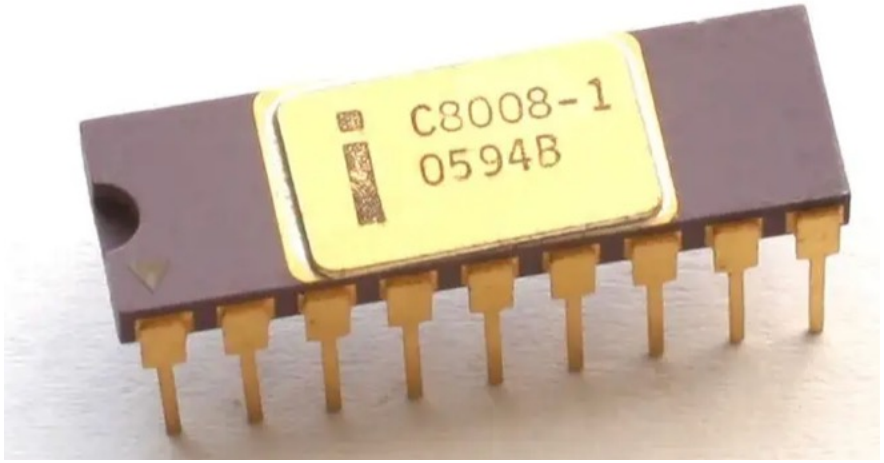
1971 **DIP**

Intel **i8008** 8-bit MPU



Chip Packaging

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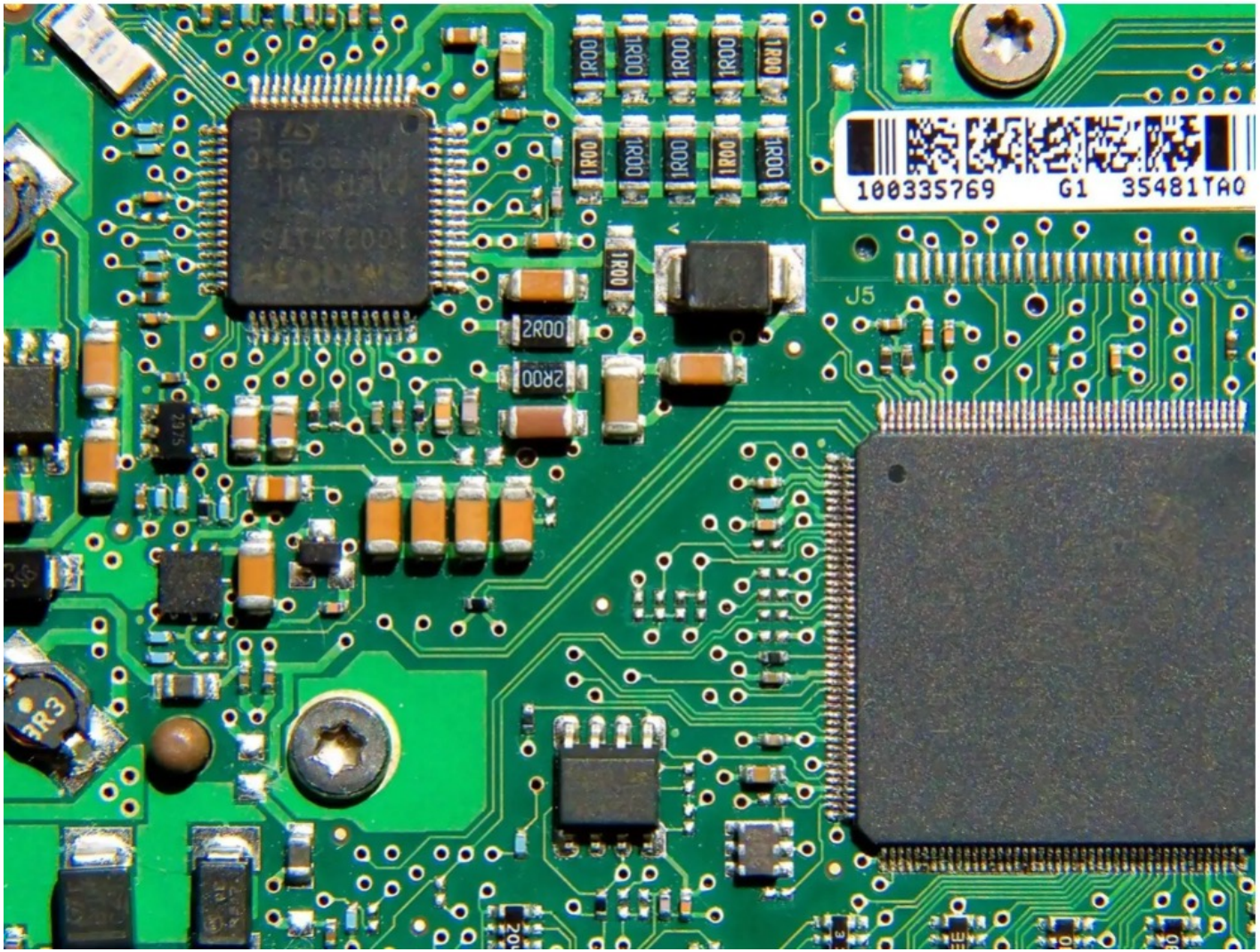
SMT

Surface Mount Packaging (1980s-1990s)



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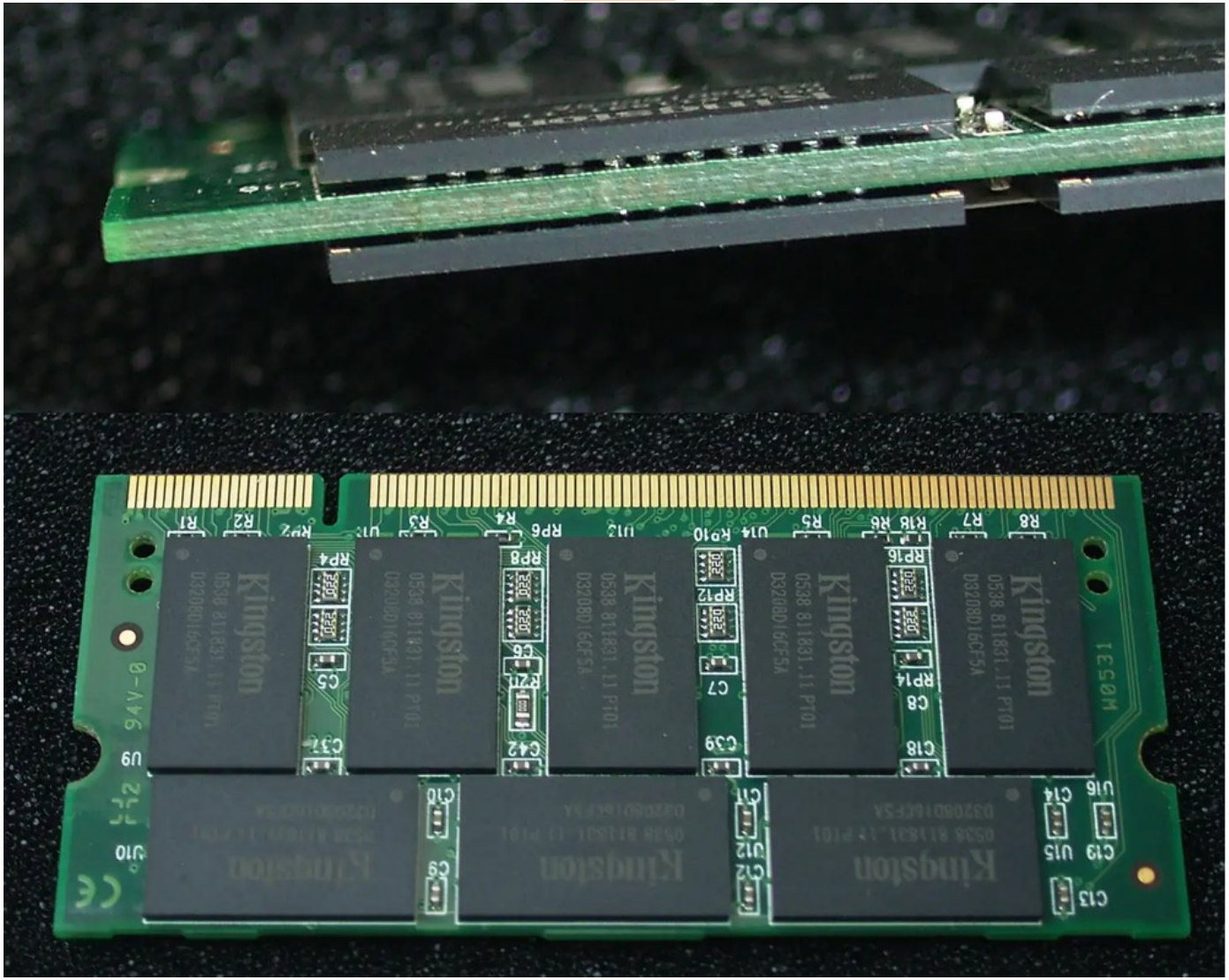
SMT



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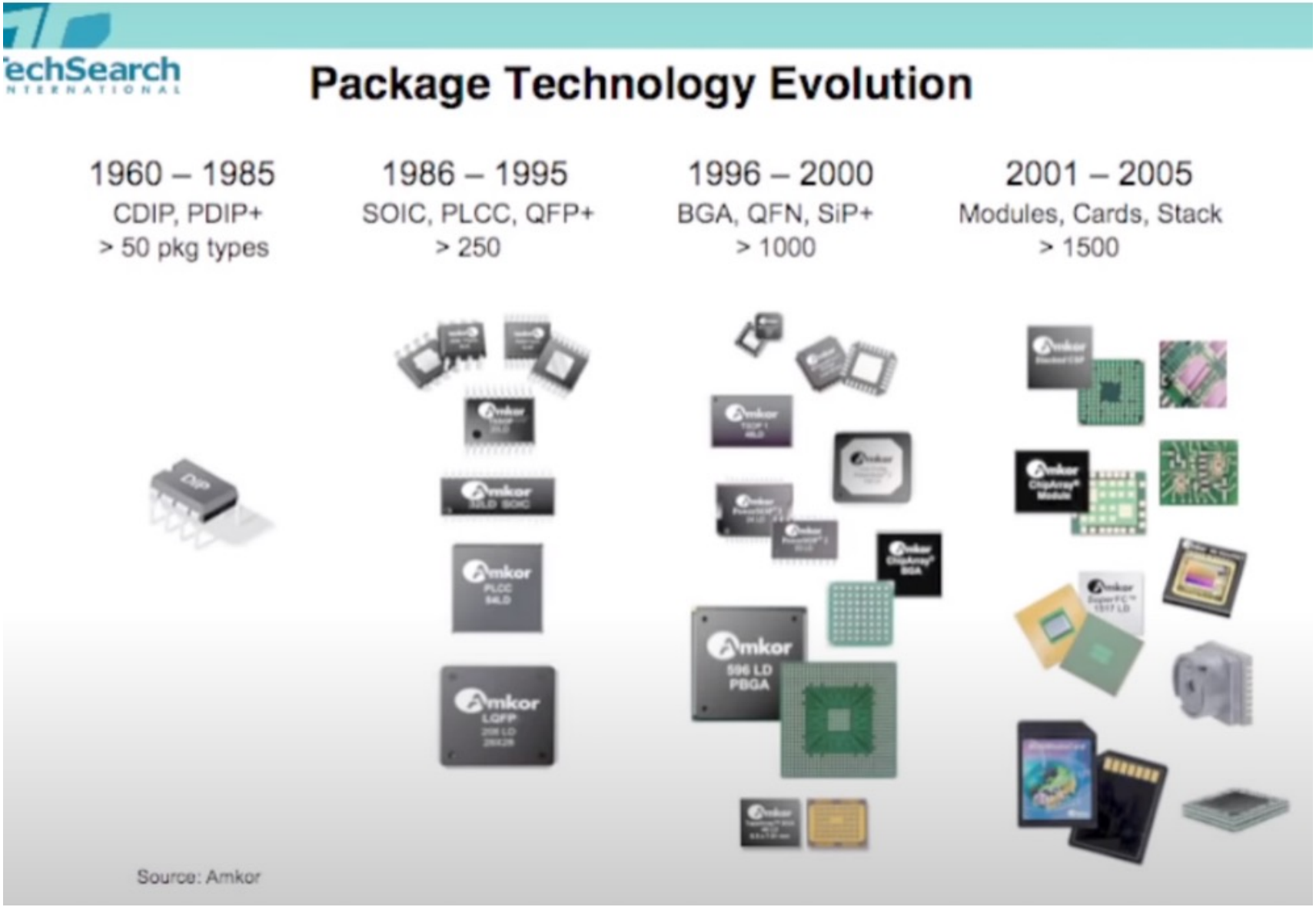

Chip Packaging

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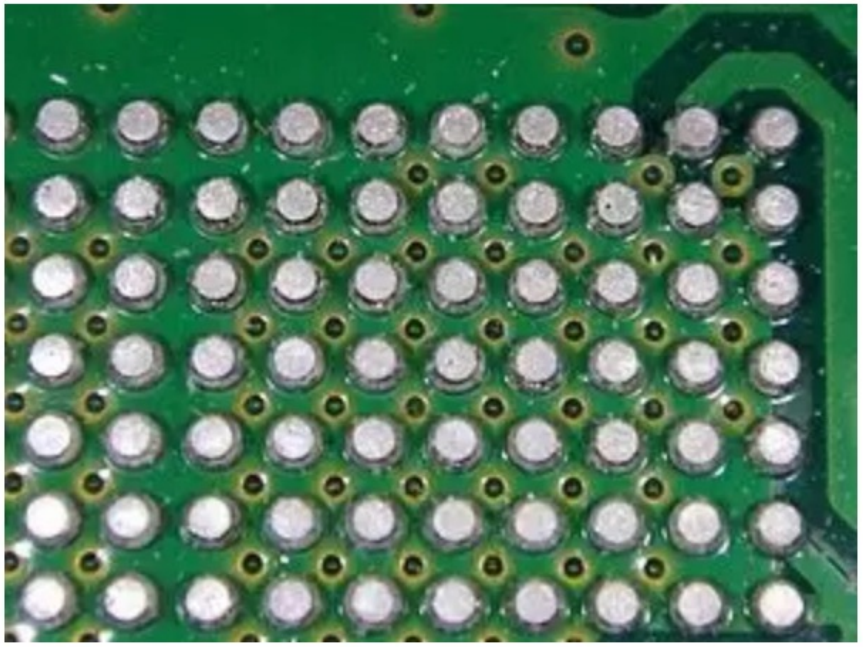
Ball Grid Packaging and Chip Scale Packaging (1990s – 2000s)

As the demands of semiconductor speed continue to pick up, so does the need for better packaging. While QFN (quad-flat no-leads) and other Surface Mounted technologies clearly continue to proliferate, I want to introduce you to the beginning of a package design that we will have to know about in the future. This is the beginning of the solder balls – or broadly Ball Grid Array (BGA) packaging.



Those balls or bumps are called solder bumps/balls

Chip Packaging (MCM)

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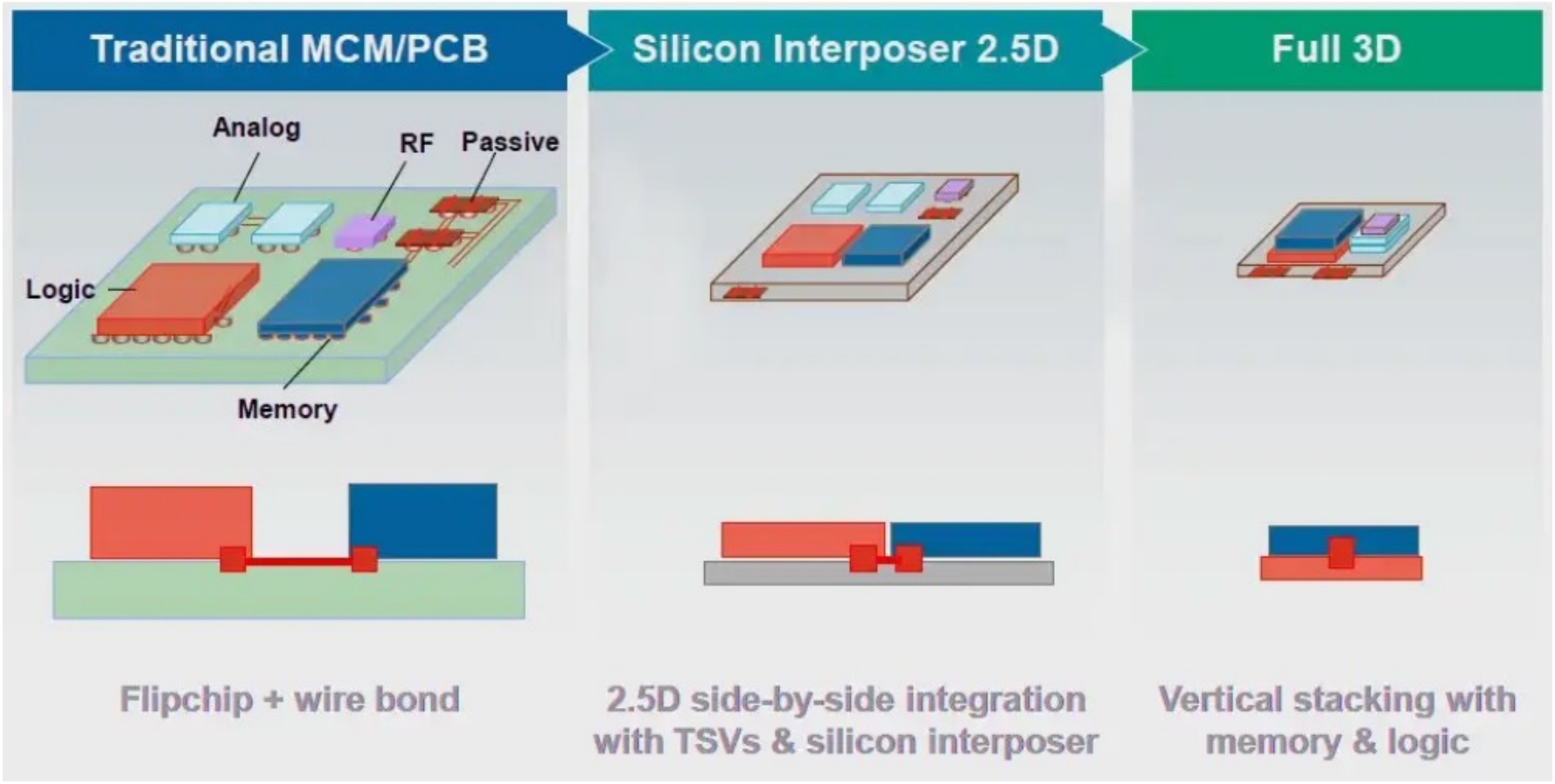

Chip Packaging: 3D Die

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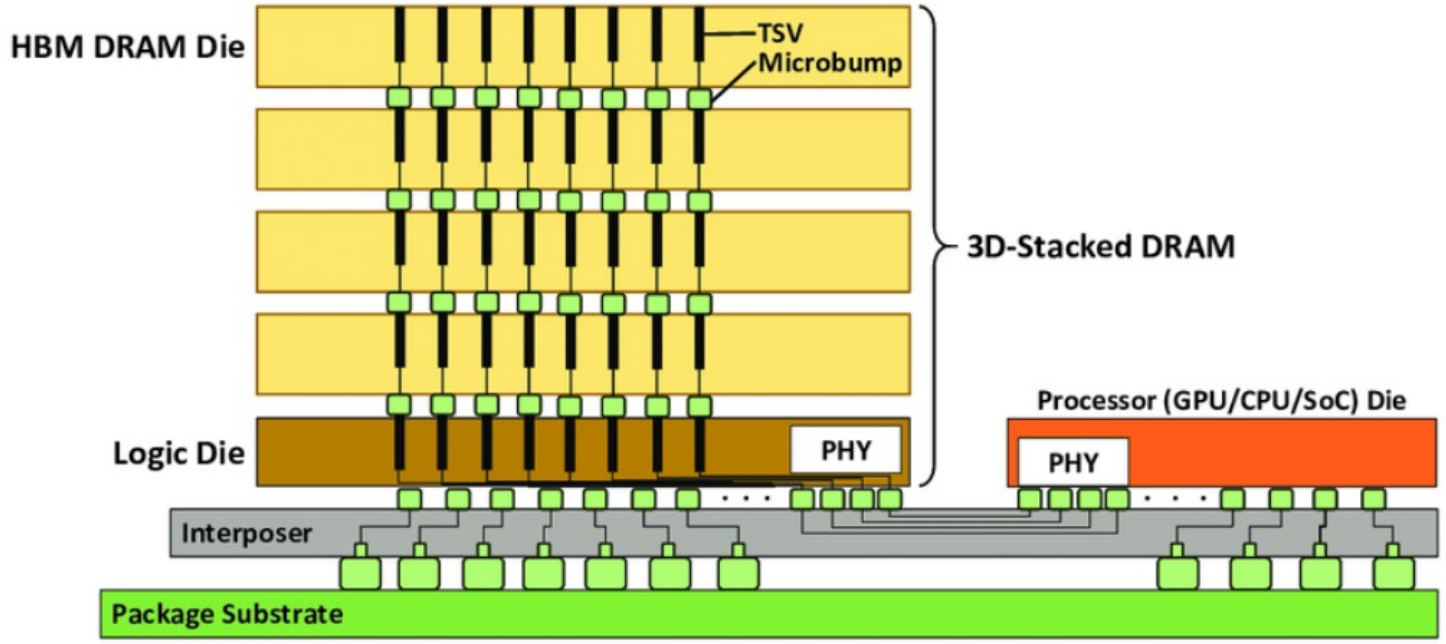
3D DRAM die stack

And what's interesting is we have a clear example of an entire semiconductor market that went 3D – Memory. Memory's push into 3D structures is a very good indication of what's to come. Part of the reason why NAND had to go 3D was that they struggled to scale at smaller geometry. Imagine memory as a large 3D skyscraper, and each of the floors is kept together by an elevator. These are called "TSV"s or Through silicon vias.



This is what the future looks like, and it's even possible we will be stacking GPU/CPU chips on each other or stacking memory on CPU. This is the final frontier

Chip Packaging: 3D Die

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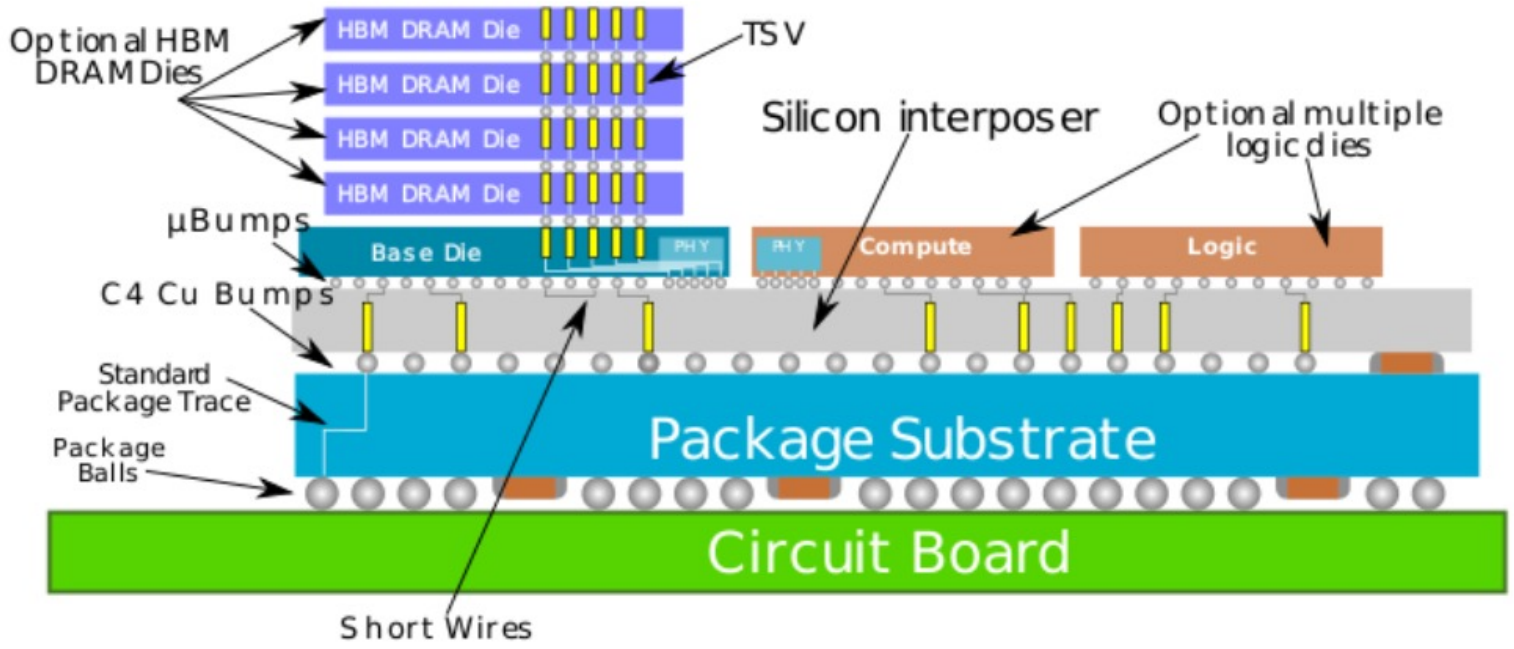
TSMC

A Quick Overview of 2.5D/3D Packaging

TSMC's CoWoS

This is seemingly the workhorse of the 2.5D integration process and was pioneered by Xilinx.



Chips

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Wafer Fabs

Foundries

Foundries Supply Chain

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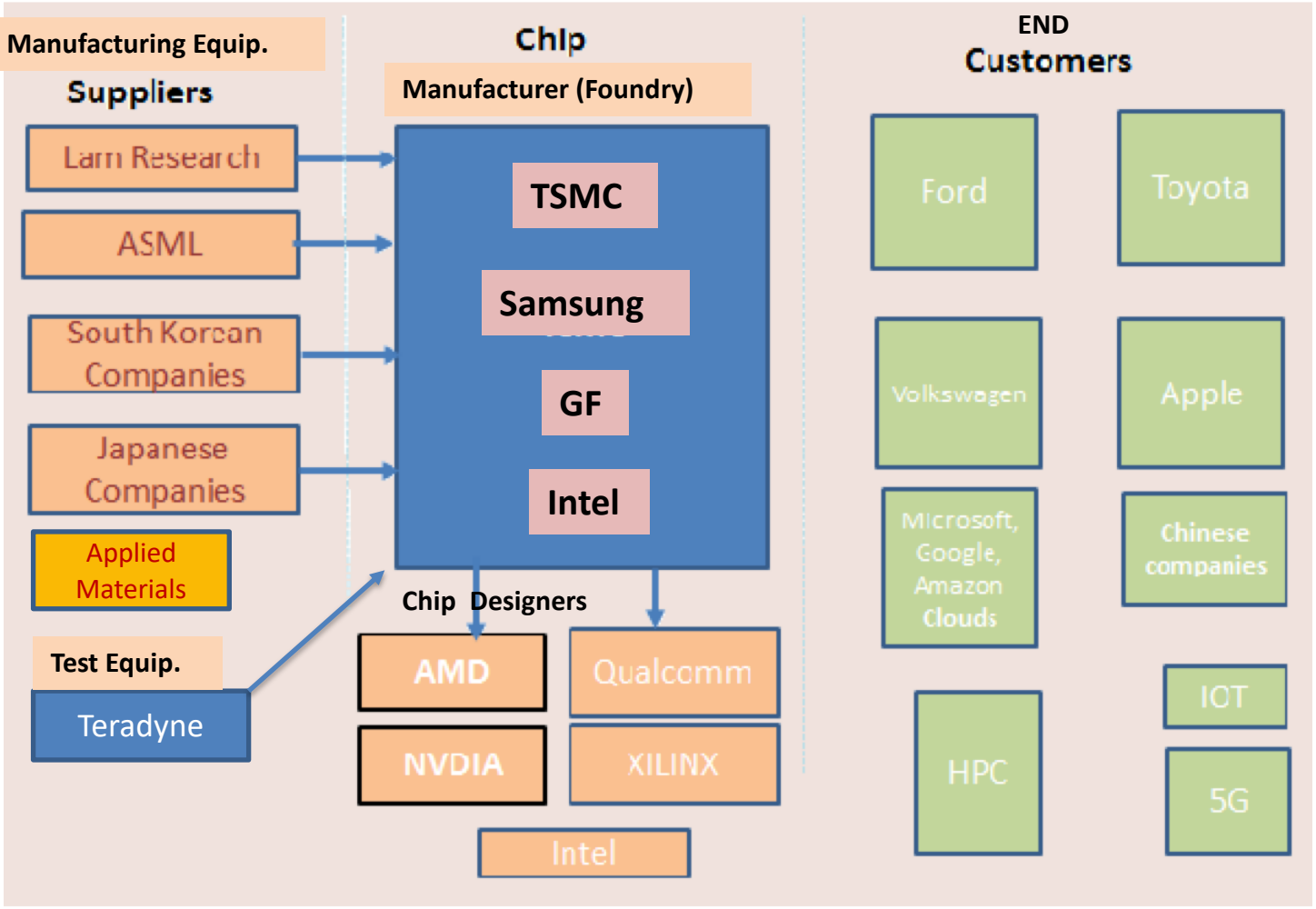
Quora

Harvey King
born in Taiwan, grew up in US, family rooted in mainland China for centuries.



Fab Timescales

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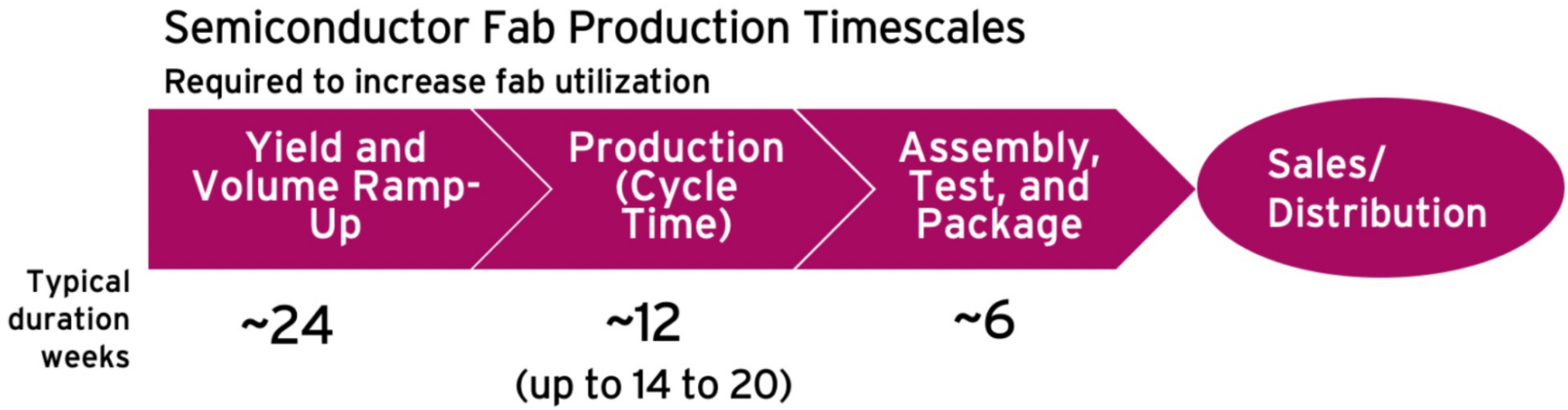
SEMICONDUCTOR INDUSTRY ASSOCIATION



Wafer Fabs Today

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1960	❖ IBM
1968	❖ Intel
1978	❖ Micron**
1980	❖ Samsung
1987	❖ TSMC* (1st foundry)
2009	❖ AMD → Global Foundries*
2010	❖ Chartered → Global Foundries*
	❖ SMIC* (China)

*Pure Foundry

**Internal use only

Foundry Stats 2020

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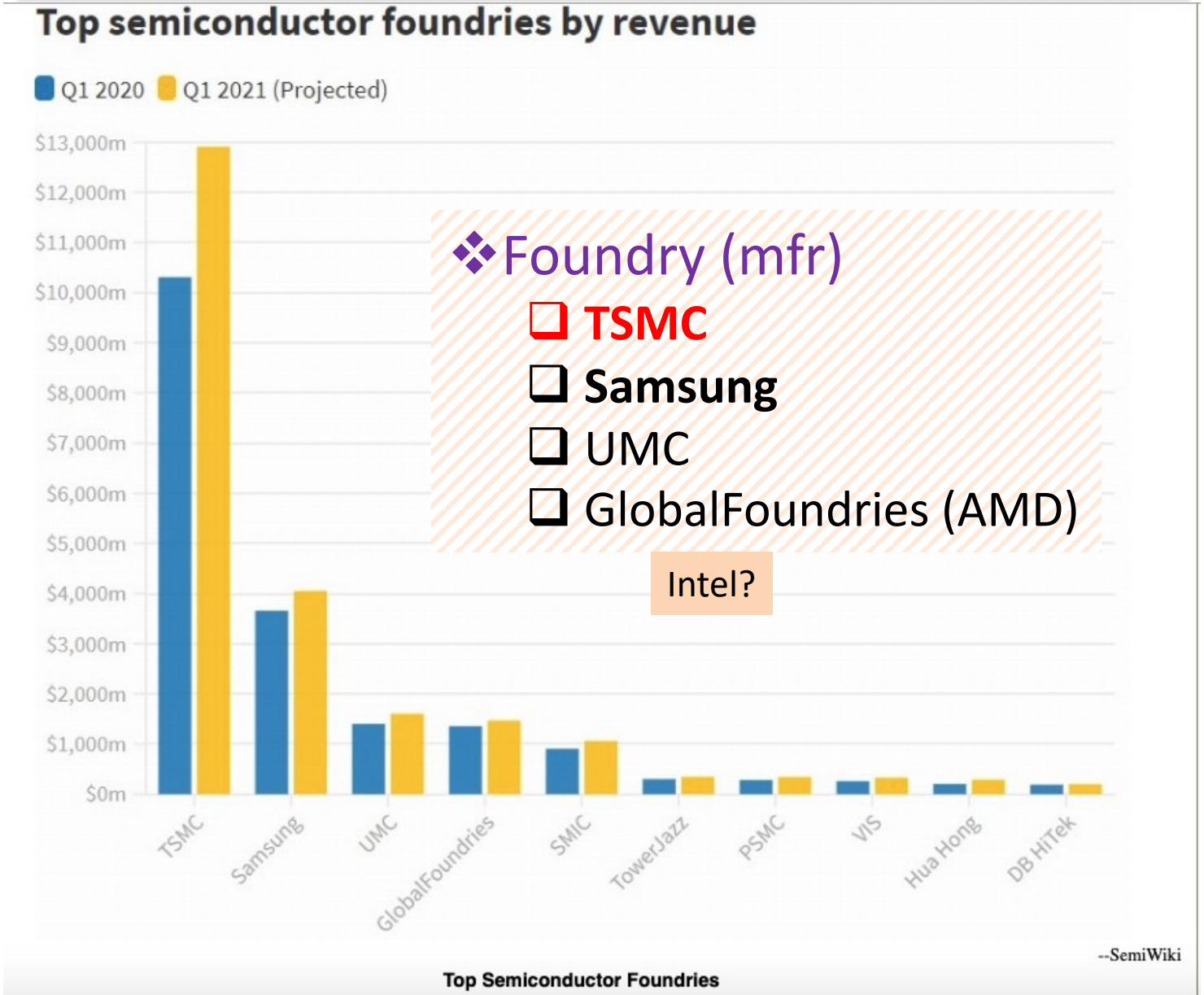

- Foundry (mfr)
  - **TSMC**
  - **Samsung**
  - UMC
  - GlobalFoundries (AMD)

Intel?

Foundry Shares 2Q22

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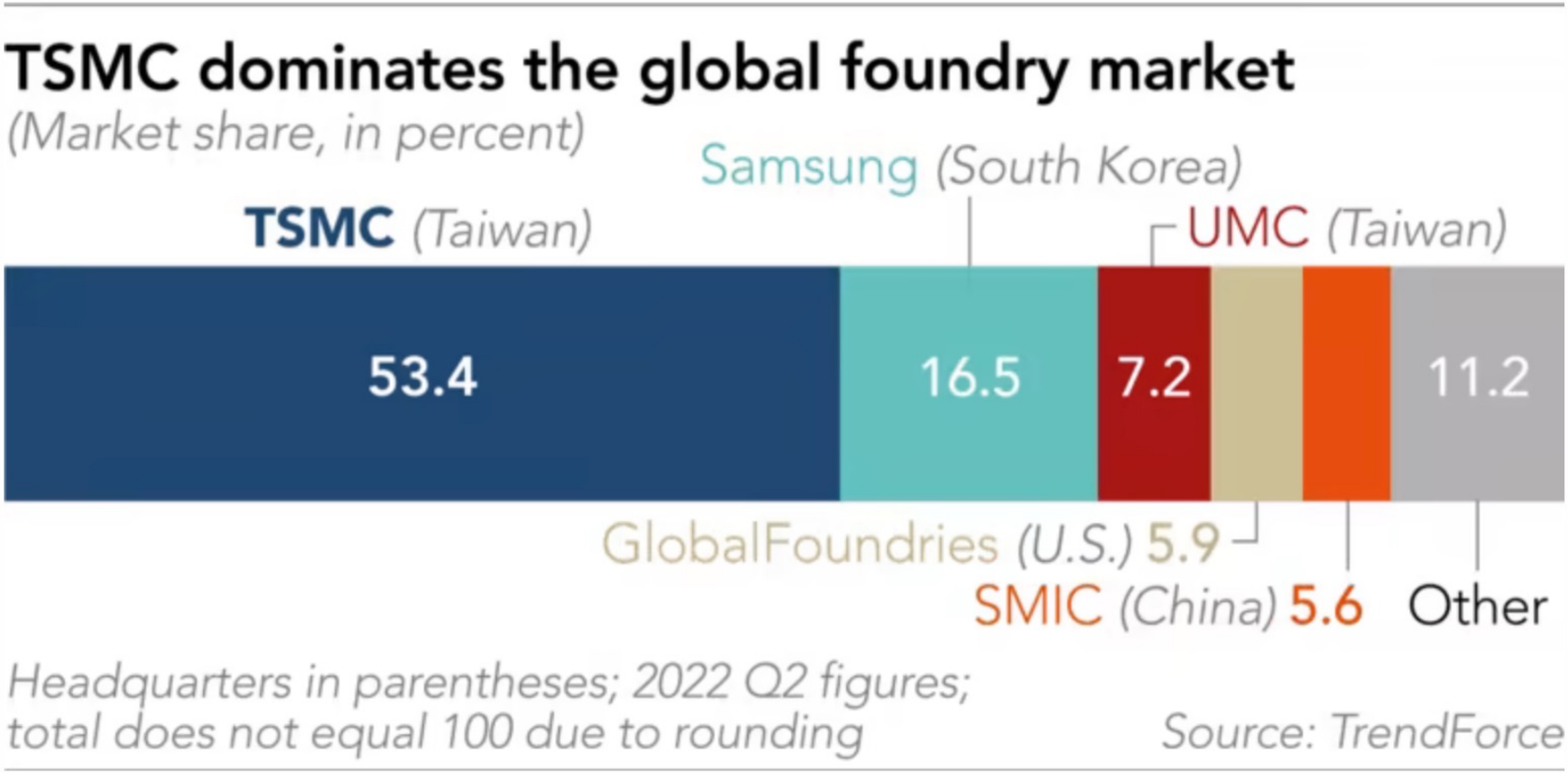

TSMC 3Q22

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Jeff Drobman

- Revenue = $20.23B
- EPS = $1.79
- Wafer revenue shares
  - 5nm = 28%
  - 7nm = 26%

Samsung **7nm** did pretty good but Samsung **5nm** and **4nm** had serious PDK/yield problems and Samsung **3nm** is not really competitive against TSMC N3 and it requires new design considerations for **GAA**.

WW Fab Share by Region

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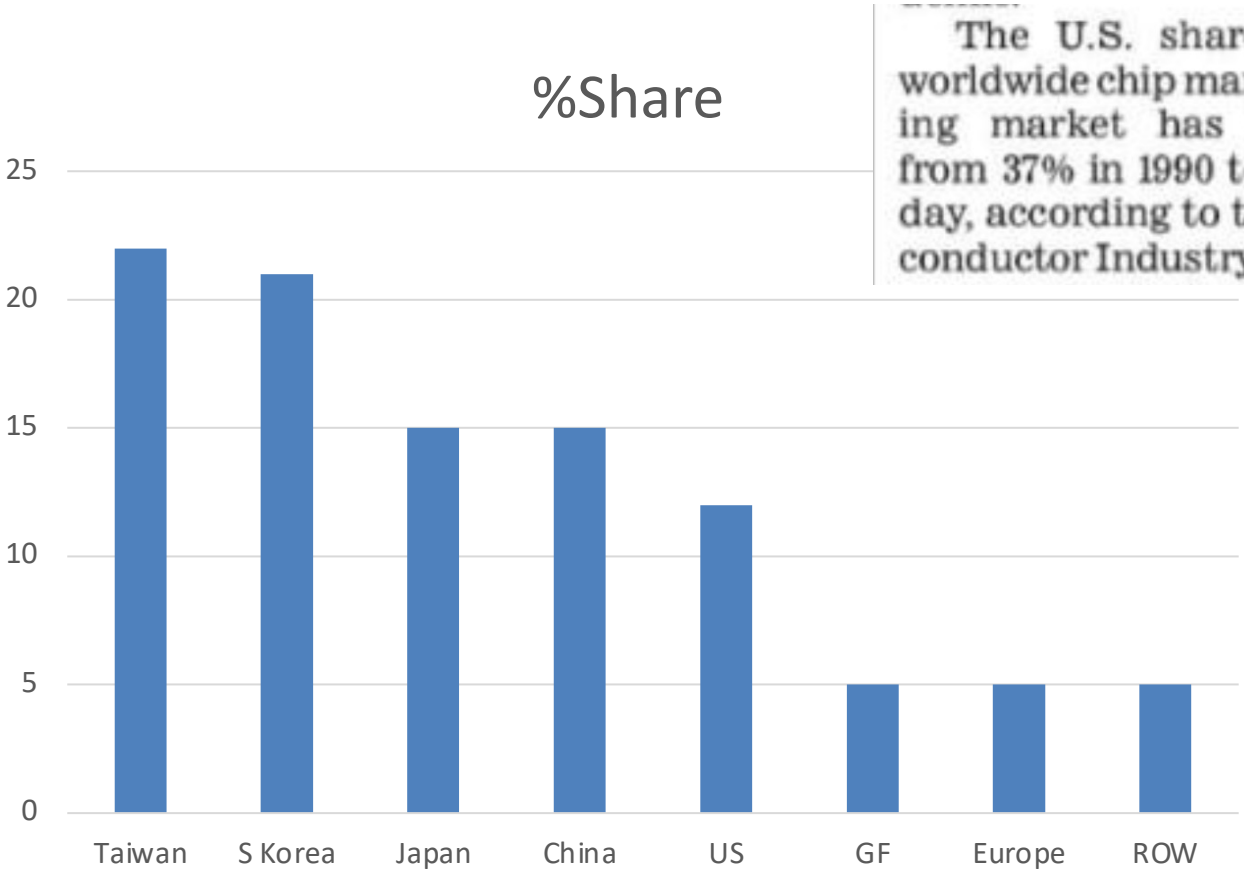

The U.S. share of the worldwide chip manufacturing market has declined from 37% in 1990 to 12% today, according to the Semiconductor Industry Assn.

Source: LA Times/SIA 1/22/22

WW Fabs

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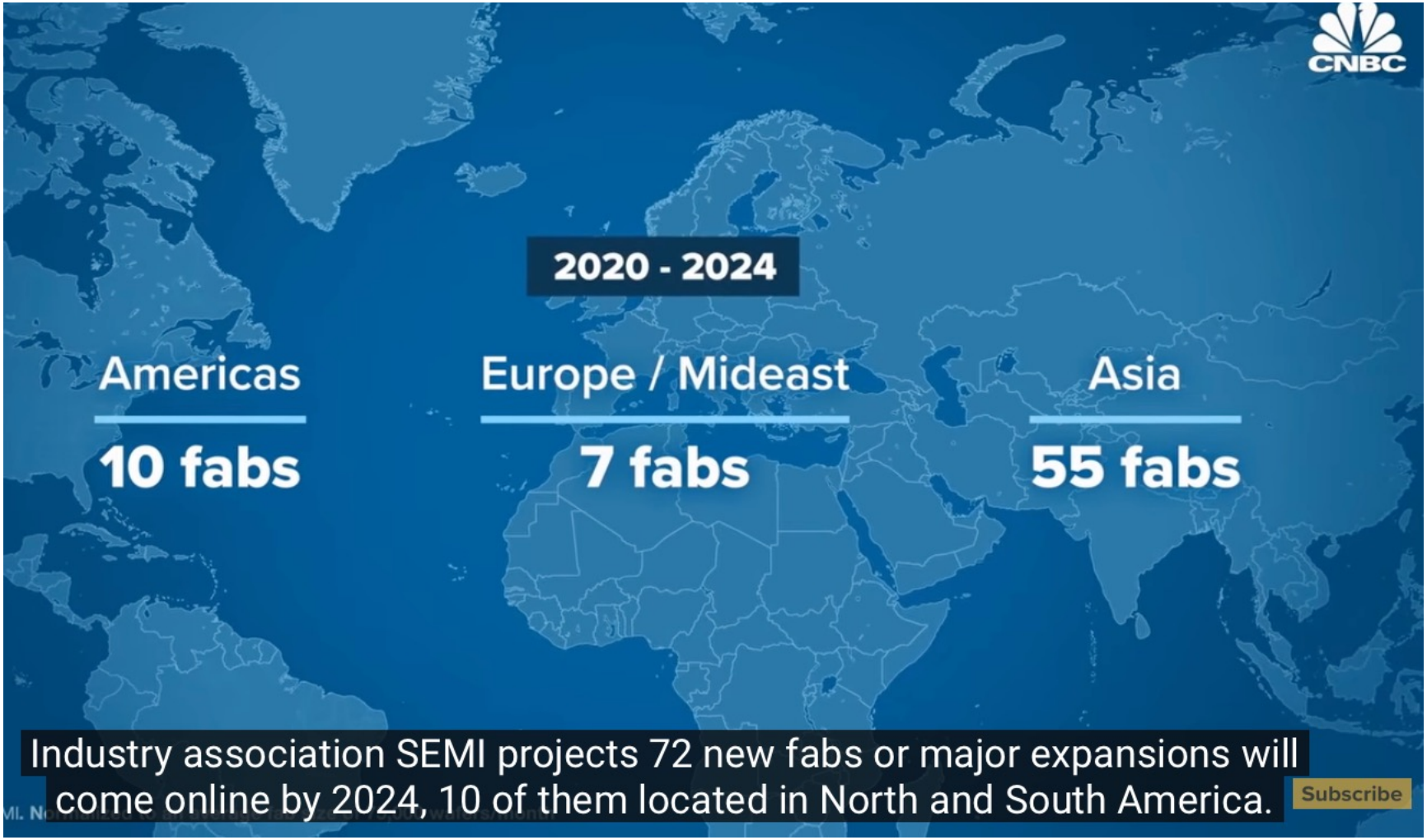

WW Foundries

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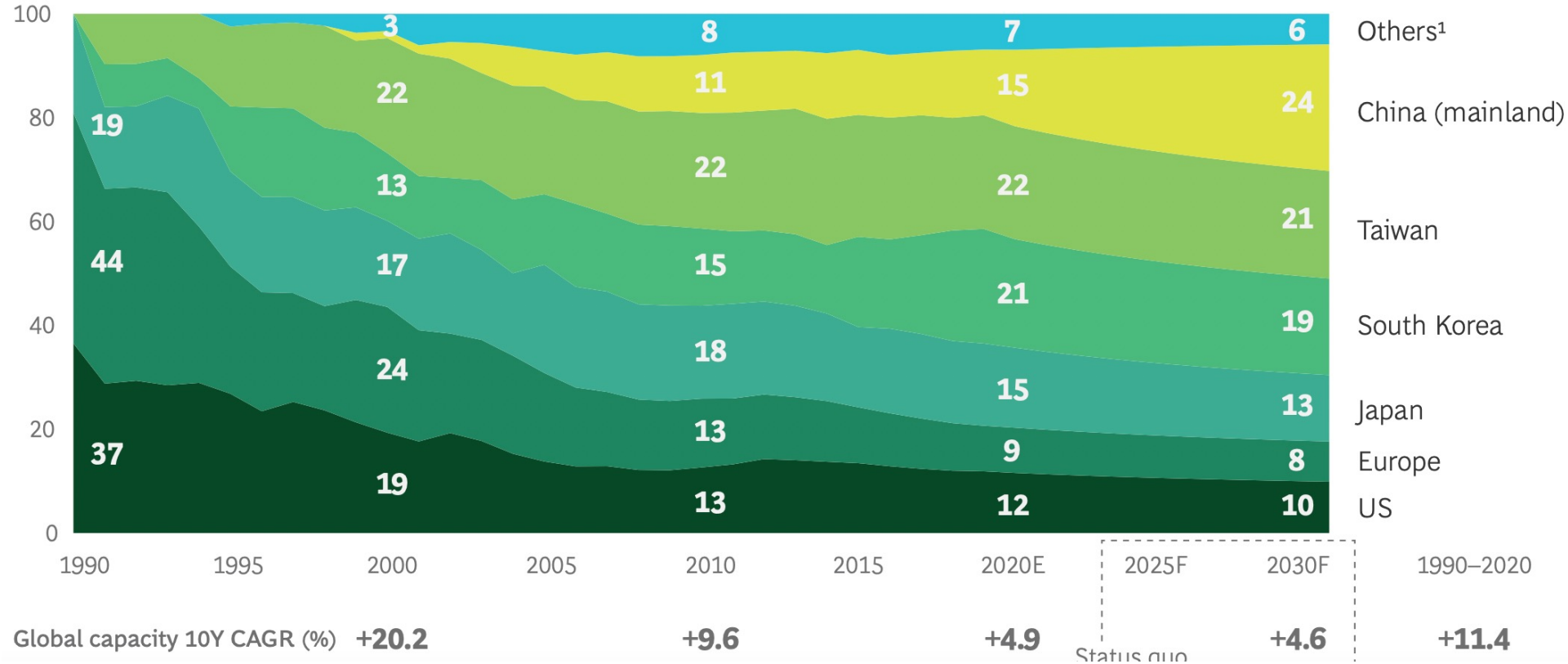
September 2020
By Antonio Varas, Raj Varadarajan, Jimmy Goodrich, and Falan Yinug

Global manufacturing capacity by location (%)



WW Foundries

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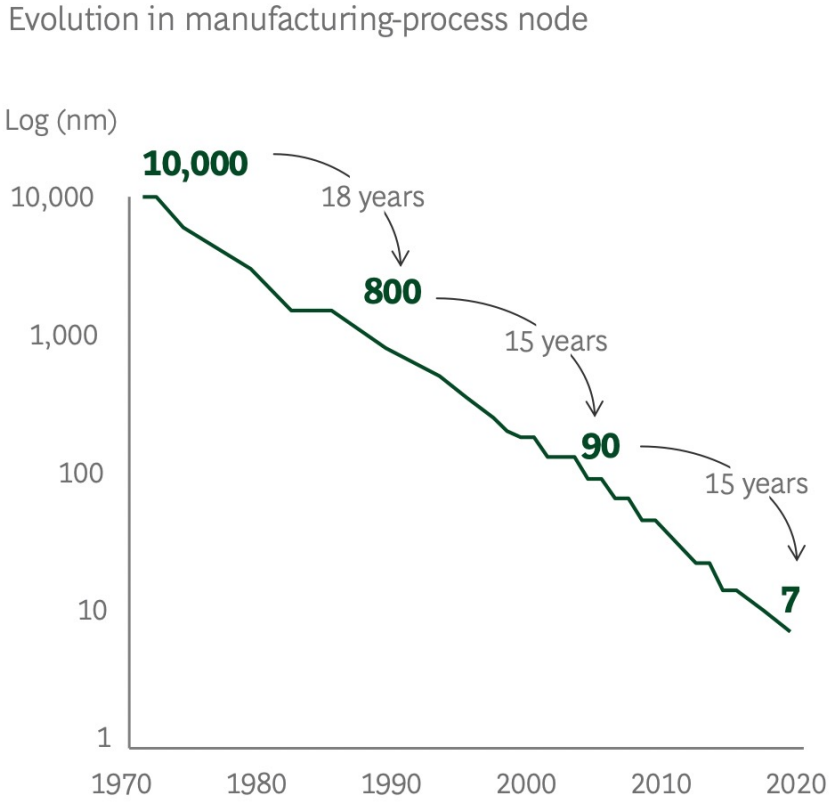

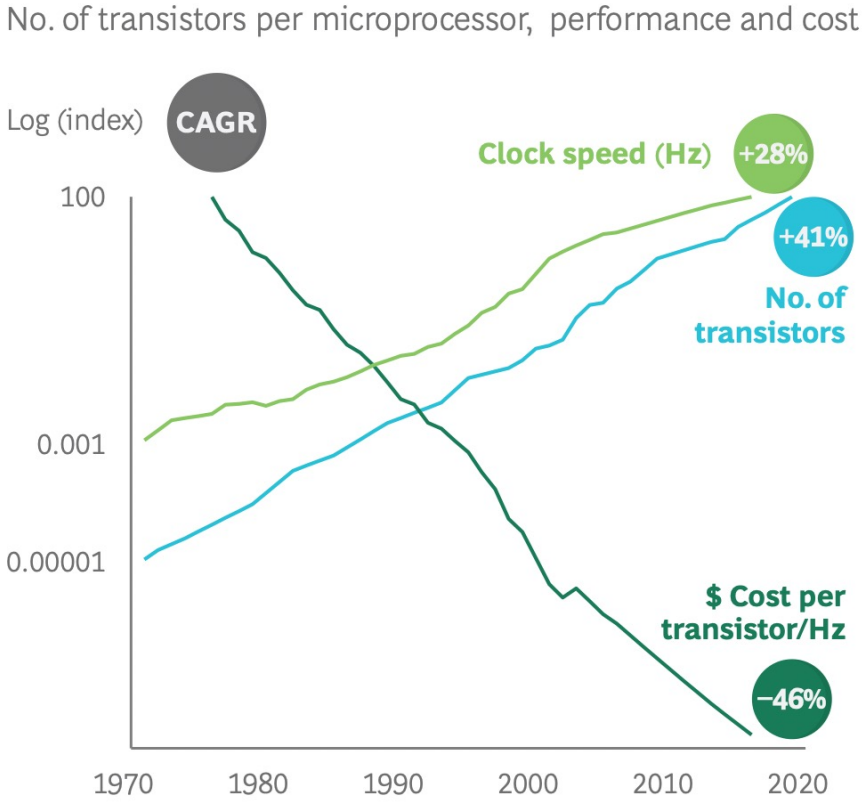

Sources: Intel; Singularity.com; Wikipedia; BCG analysis.

Foundry Biz

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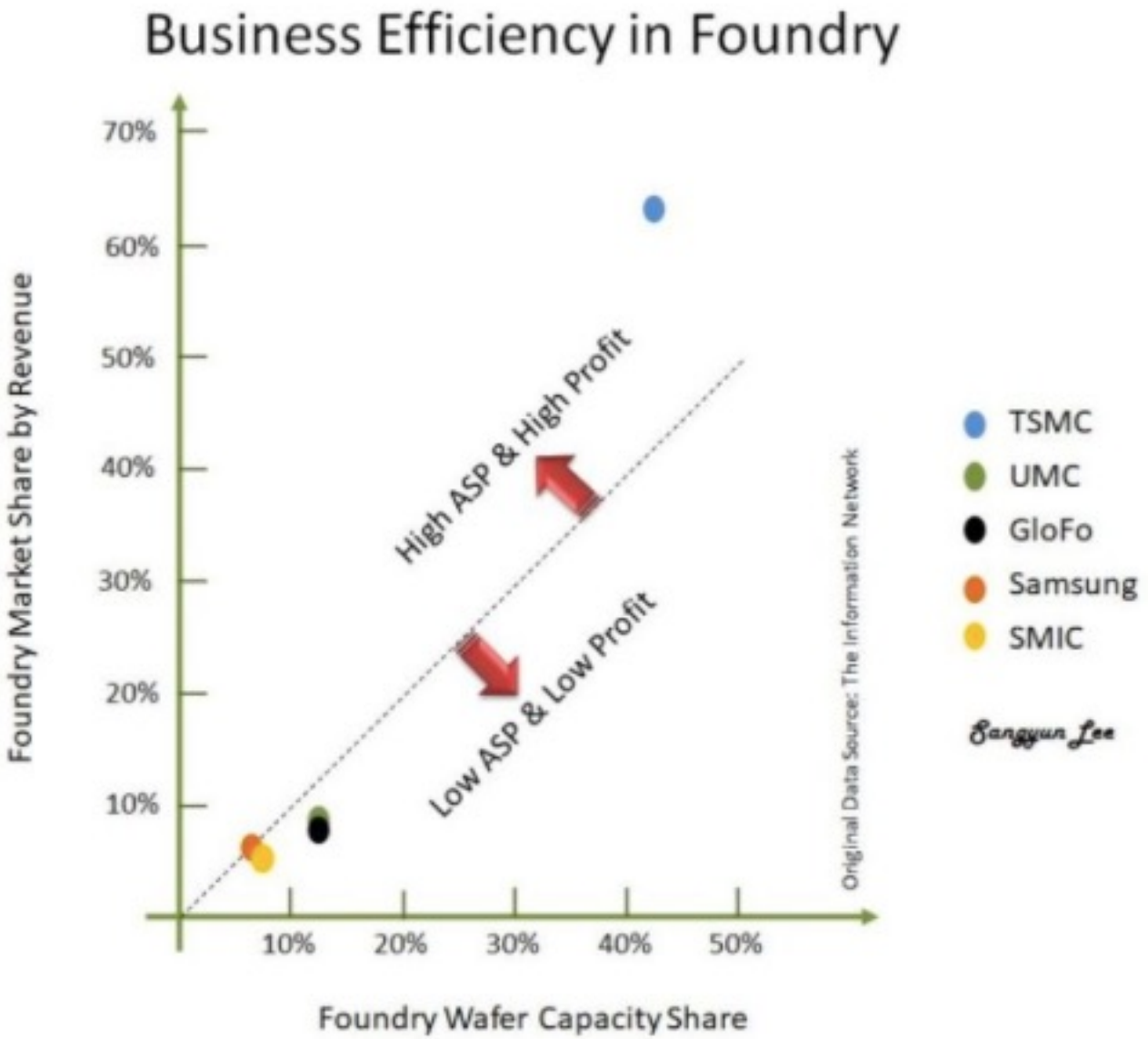

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Chip Fab:
Mask Making
ASML

ASML EUV Machines

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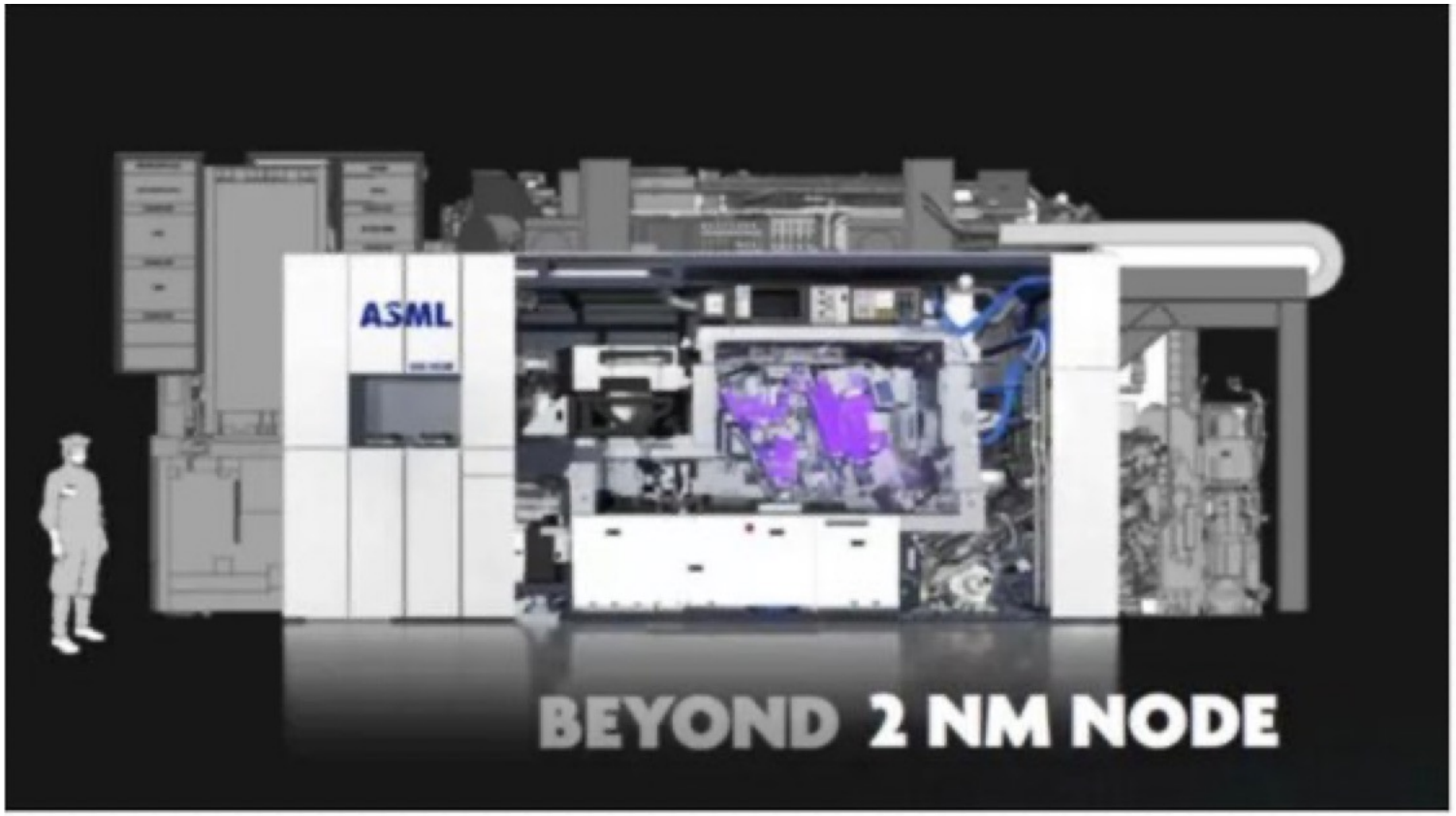
Quora



Current EUV lithography system (NA=0.33) (front) compared to the next generation of high NA EUV lithography system (NA=0.55) (back).

ASML EUV Machines

Quora

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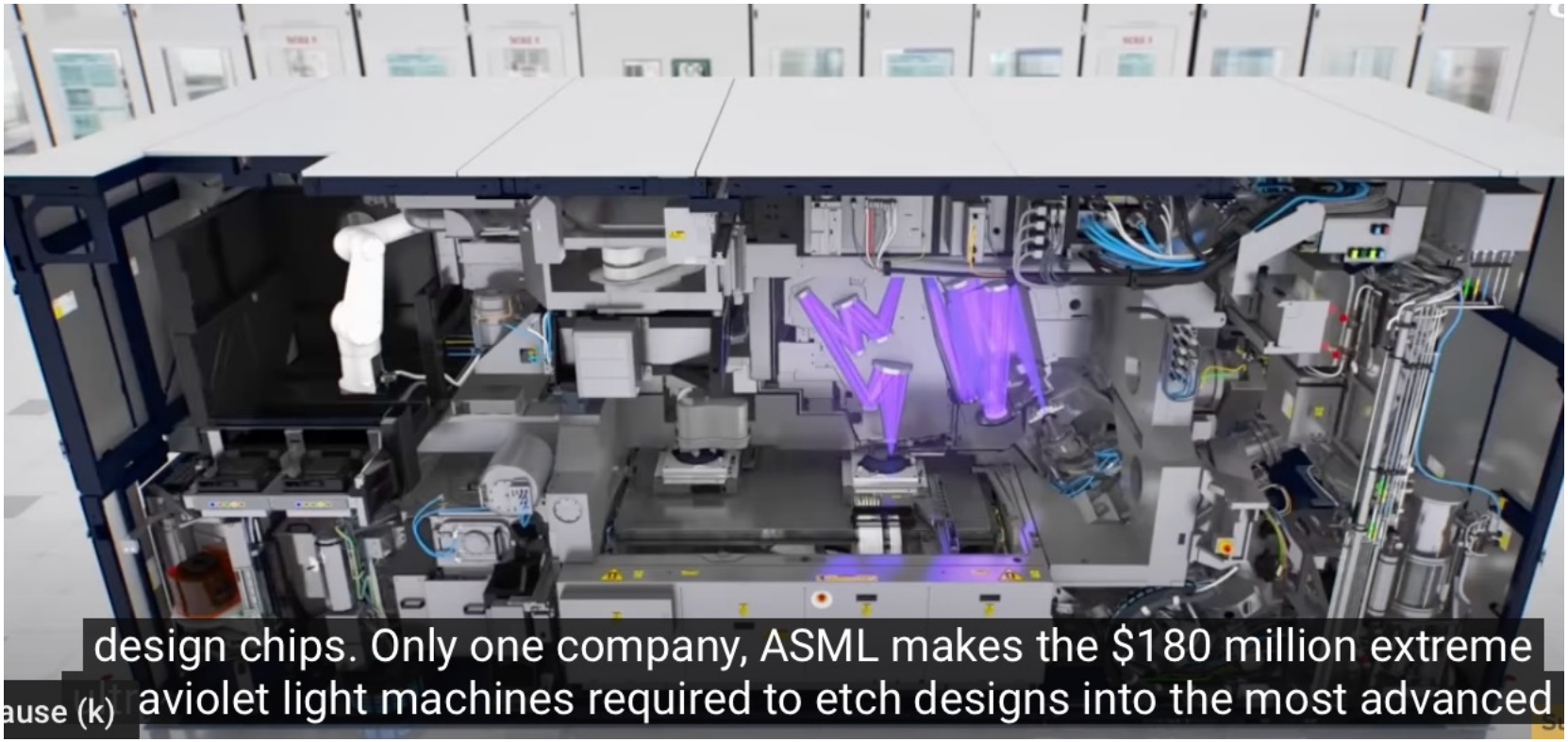

ASML: EUV for Mask Litho

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The open forum for semiconductor professionals

Semiconductor Advisors

Is ASML Immune from China Impact?
by Robert Maire on 10-21-2022 at 10:00 am
Categories: China, Lithography, Semiconductor Advisors, Semiconductor Services

ASML proves litho's place at Apex of semiconductor food chain

ASML announced a great quarter with Euro5.8B in revenue and EPS of Euro4.29/share. Outlook is for revenues of Euro6.1B to 6.6B with gross margins of 49%. Gross margin for 2022 will come in about 50% overall.

Most importantly, orders came in at a huge Euro8.9B, 77% logic, bringing backlog to a multi-year Euro38B. ASML is looking at shipping 60EUV and 375DUV systems in 2023, assuming supply chain issues are resolved.

ASML: EUV for Mask Litho

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The open forum for semiconductor professionals

Semiconductor Advisors

Is ASML Immune from China Impact?
by Robert Maire on 10-21-2022 at 10:00 am
Categories: China, Lithography, Semiconductor Advisors, Semiconductor Services

China immunity from two factors

ASML will have 5% or less impact next year from the China issue for two simple reasons; number one, the majority of current business is non leading edge, above 14NM as ASML was already not shipping any EUV tools to China. Number two, ASML is sold out anyway and there are a large number of customers who will happily snap up any systems that China doesn't or can't take.

In our view, as we had previously commented on months ago, ASML is virtually immune to China embargo issues given their leading positioning in the industry. The semiconductor industry remains a zero sum game and litho systems not shipped to China will go elsewhere to satisfy demand.

ASML: EUV for Mask Litho

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Semiconductor Advisors

Is ASML Immune from China Impact?
by Robert Maire on 10-21-2022 at 10:00 am
Categories: China, Lithography, Semiconductor Advisors, Semiconductor Services

Light source technology is developed by former Cymer, in San Diego, that ASML was allowed to buy by the US government. We are relatively certain that there were agreements regarding Cymers technology in order to win acquisition approval.

Many investors may not be aware that much if not most of the laser technology, especially for EUV, arose out of the "star wars" laser weapons systems of the Regan era as Cymer employed many scientists out of the ex star wars program from both the US and former Soviet Union. The technology used in the 250KW drive laser in EUV systems could be re-purposed for military applications.

77% logic mix shows resilience

The fact that 77% of orders are from logic suggests that a more rapid slowdown in memory will not impact ASML at all. Management also announced orders for High NA systems along with regular EUV systems. Though high NA was not broken out, at over Euro300M a system, the numbers can add up more than twice as fast as DUV systems. We assume that TSMC, Intel and Samsung have likely already ordered multiple High NA EUV systems. TSMC's recent capex cut clearly is not impacting their litho system orders as they understand the import of leading in litho.

ASML EUV Roadmap

Quora

EUV product roadmap

Wavelength	NA, Half pitch	2020	2021	2022	2023	2024	≥2025
EUV	0.33 NA, 13 nm	NXE:3400C 1.5 nm | 135 wph[1] / 145 wph[2]	NXE:3600D 1.1 nm | 160 wph		NXE:3800E <1.1 nm | >195 wph / 220 wph[2]		NXE:4000F <0.8 nm | >220 wph
	0.55 NA, 8 nm				EXE:5000 at ASML fab	EXE:5000 <1.1 nm | 150 wph[3]	EXE:5200B <0.8 nm | 220 wph

Wafers/hours (wph) are at dose 30mJ/cm² unless specified otherwise.
1) 170wph@20mJ/ cm²
2) Including throughput upgrade
3) 185wph@20mJ/ cm²

Product: Matched Machine Overlay (nm) | Throughput (wph)
Product status: Released | Development | Definition

ASML

SPIE. ADVANCED LITHOGRAPHY | For High NA, see: SPIE 12051-6
High NA EUV enabling cost efficient scaling for N+1 technology nodes, Greet Storms et al.

Page 15
Public

Figure 5. System Roadmap.

ASML EUV Mask Count

Jeff Drobman

Quora

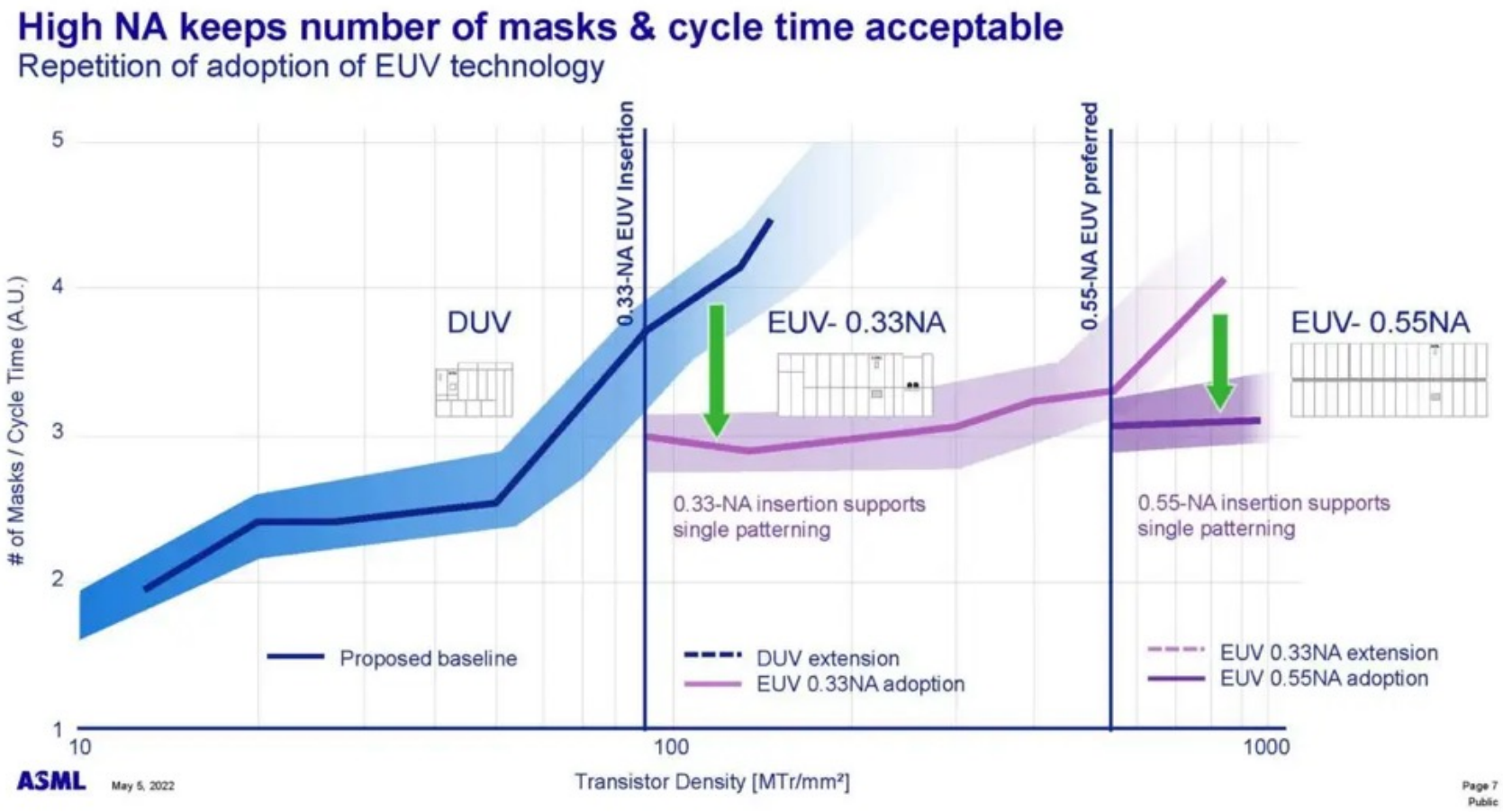

Figure 8. Mask Count Trends.

ASML EUV Wafers Out

Quora

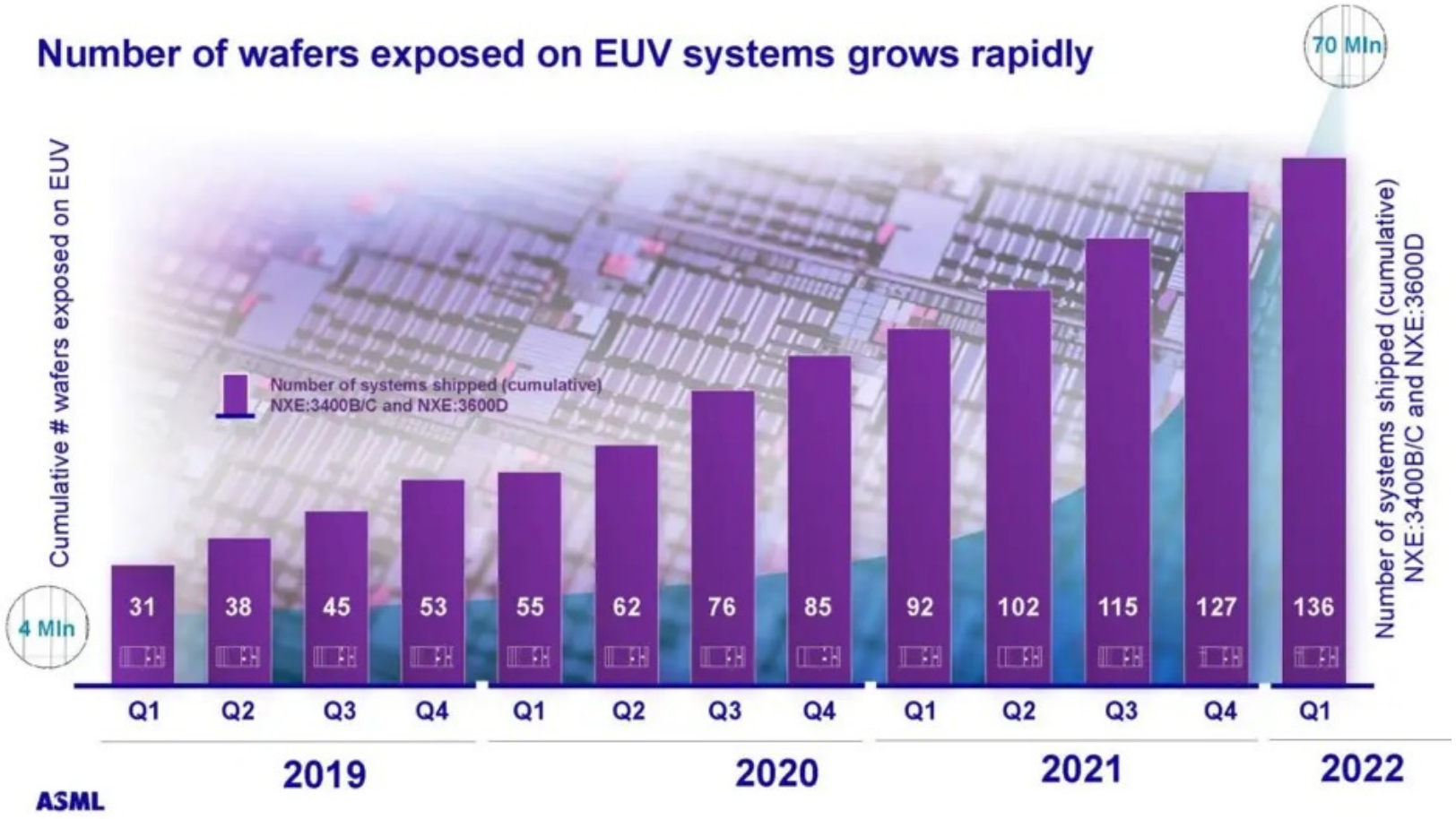

Figure 2. Number of EUV Wafers Exposed.

Chips/Fabs

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Chip Design/Fab

AMD/Intel

Fabs – AMD, Intel

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AMD Sunnyvale Fab 1 1970

$1M

Cost x10,000 in 40 years
averages to
250x per year

$10B

Intel's latest Fab in Hillsboro

An aerial view of Ronler Acres, Intel's largest silicon research and development hub.

Chip Fab

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INDIE APP DEVELOPER
Jeff Drobman

Bob McConnell
Former VP and Site Manager, Heilbronn, Germany at Atmel (company) (2003–2009) · Wed

Silicon wafer chip defects are said to happen on all chips produced. How/why does this occur, and are there ways to prevent it?

First, read Wikipedia: Semiconductor Device Fabrication. I think it explains the issues at a basic level. Secondly, there are many places for defects to occur. They DO NOT occur on the basic patterning information because that is computer generated. If it doesn't check out correctly the pattern is regenerated. The wafer can have defects due to crystal growth anomalies. This is very unlikely and causes negligible failures.

Particles are at a very low level. The wafers being processed are moved between process steps in sealed, super clean boxes. The boxes are only opened inside machines that are sealed and or have positive pressure.

Chip Fab

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Jeff Drobman

Bob McConnell
Former VP and Site Manager, Heilbronn, Germany at Atmel (company) (2003–2009) · Wed

The processing of a wafer involves deposition or growth in various ways of well over a hundred or more layers of material. This includes photoresist to be exposed as part of the photo lithography process, oxide layers that are grown to be later patterned and etched, metal layers to be patterned and have the interconnect defined, and dielectric layers to be insulators between the metal layer. The dielectric layers are patterned to produce the interconnect between metal layers.

Any of these layers might have a defect caused by a flaw in the material or by a particle that somehow escaped all the controls and filters. The processes are adjusted to, as much as possible, eliminate these defects. A photo layer might be processed twice through a photo lithography step. There might be a high temperature step to allow a material to flow and close a defect. (only works when that high temp doesn't hurt any thing below the current layer) This has been the basic fight of the industry to keep allowing transistor counts to increase. Looking out 4 years and doing some math tells the process engineer and equipment engineer what has to happen to stay on that exponential curve of Moore's Law.

Chip Design vs Mfg

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INDIE APP DEVELOPER
Jeff Drobman

Is designing computer chips the same as planning how to manufacture them?

Jeff Drobman, Lecturer at California State University, Northridge (2016-present)

Answered just now

there are many levels of design for all digital systems, including hardware and software. chips have CPU cores, GPU cores, cache memories, I/O, system logic and clocking, etc. first level is the “macro” architecture: layout of all those subsystems. Cores may be licensed (designed by others) or designed from scratch. other subsystems are usually licensed from the fab or others.

It is the design of the cores and other subsystems that is the most intricate design process. Each item needs to follow the detailed “design rules” given by the selected fab (manufacturer), as well as their interconnections.

AI in Chip Design

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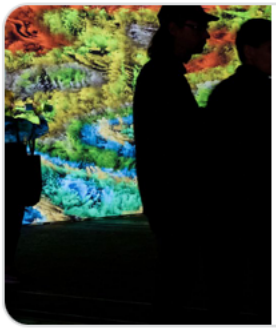
Jeff Drobman

8-31-21

Chuck Bluestein, A great deal of non-fiction reading.

Answered 34m ago

Here is an article that talks about this that you can read and share with others. The name of the article is:



Opinion: Computer chips are getting so advanced, companies are using artificial intelligence to make them

The introduction of AI in chip design is a necessity for performance an...

https://www.marketwatch.com/story/computer-chips-are-getting-s...

This is what the article says on it:

> **Thanks to a machine-learning technique known as reinforcement learning , artificial intelligence completed the task in only six hours, compared with weeks by humans.**

Foundries

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Intel

Founded 1968

Intel Fabs

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Fab name	Fab location	Production start year	Process (wafer, node)
D1B	USA, Oregon, Hillsboro	1996	300mm, Development
RB1	USA, Oregon, Hillsboro	2001	300mm, Development
D1C	USA, Oregon, Hillsboro	2001	300mm, Development
RP1	USA, Oregon, Hillsboro	2001	300mm, Research
D1D	USA, Oregon, Hillsboro	2003	300mm, Development
D1X	USA, Oregon, Hillsboro	2013	300mm, Development
Fab 11X	USA, New Mexico, Rio Rancho	1995 upgrade 2020/2021 with 22/14	300mm, 45 nm/32 nm, Packaging
Fab 12	USA, Arizona, Chandler	2006	300mm, 22 nm/14 nm/10 nm
Fab 22	USA, Arizona, Chandler	2002	300mm, 22 nm/14 nm/10 nm
Fab 24	Ireland, Leixlip	2006	300mm, 14 nm[2]
Fab 28a	Israel, Kiryat Gat	1996	300mm, 22 nm
Fab 28	Israel, Kiryat Gat	2023	300mm, 22nm/14nm/10nm[3][4]
Fab 38	Israel, Kiryat Gat	2024	300mm, 22 nm[5]
Fab 32	USA, Arizona, Chandler	2007	300mm, 22 nm/14 nm/10 nm
Fab 34	Ireland, Leixlip	2023	300mm, 7 nm[6]
Fab 42	USA, Arizona, Chandler	2020	300mm, 10 nm/5 nm (2024)
Fab 52	USA, Arizona, Chandler	(2024)[7]	300mm, 7 nm
Fab 62	USA, Arizona, Chandler	(2024)[7]	300mm, 5 nm
	USA, Ohio, Licking County	(2024-2025)	300mm, 5 nm
SC2	USA, California, Santa Clara		Reticle/Masks, Intel Mask Operations[8]
	Malaysia, Kedah, Kulim	(2024)	300mm, Packaging[9]
	Germany, Magdeburg, Saxony-Anhalt	(2027)	[10]
	Italy	(2025-2027)	300mm, Packaging[11]

Chip Shortage

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Intel New Fabs in Phoenix

Intel New Fabs

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Intel Breaks Ground on Two New Leading-Edge Chip Factories in Arizona

Daniel Nenni · Today at 5:44 AM

Daniel Nenni

ADMIN

Staff member

Today at 5:44 AM

New $20 billion capacity expansion will bring Intel's total Arizona investment to more than $50 billion.

Intel CEO Pat Gelsinger signals to the crowd from earth-moving equipment in Chandler, Arizona, on Friday, Sept. 24, 2021, for a groundbreaking ceremony to celebrate the largest private-sector investment in Arizona's history. The construction of two new computer chip factories is a $20 billion project that will bolster U.S. semiconductor leadership and help bring geographical balance to the global supply chain. (Credit: Intel Corporation)

Intel New Fabs

DR JEFF SOFTWARE
INDIE APP DEVELOPER
Jeff Drobman

September 24, 2021 03:21 PM Eastern Daylight Time

CHANDLER, Ariz.--(BUSINESS WIRE)--**What's New:** Intel today broke ground on two new leading-edge chip factories at the company's Ocotillo campus in Chandler, Arizona. In a groundbreaking ceremony attended by senior government officials and community leaders, Intel CEO Pat Gelsinger celebrated the start of construction on the largest private investment in state history and reiterated the company's commitment to investing in U.S. semiconductor leadership.

"Today's celebration marks an important milestone as we work to boost capacity and meet the incredible demand for semiconductors: the foundational technology for the digitization of everything. We are ushering in a new era of innovation – for Intel, for Arizona and for the world. This $20 billion expansion will bring our total investment in Arizona to more than $50 billion since opening the site over 40 years ago. As the only U.S.-based leading-edge chipmaker, we are committed to building on this long-term investment and helping the United States regain semiconductor leadership."

–Pat Gelsinger, Intel CEO

Why It's Important: Advanced domestic chipmaking capacity and capabilities are critical for the sake of both economic and national security. The United States has lost ground in semiconductor manufacturing and is at risk of falling farther behind. With its new IDM 2.0 strategy, Intel is doing its part to help rebuild U.S. leadership and bring more balance to the global supply chain. Intel is the only semiconductor manufacturer with leading-edge process and packaging research capabilities in the United States, and the company is investing in domestic capacity to support the surging worldwide demand for chips across multiple segments, from PCs to automobiles to the data center and more.

Intel New Packaging

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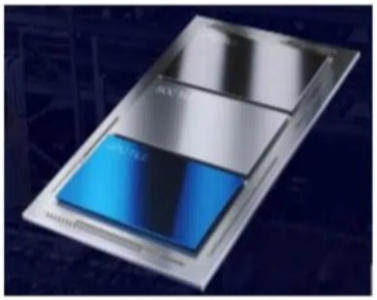
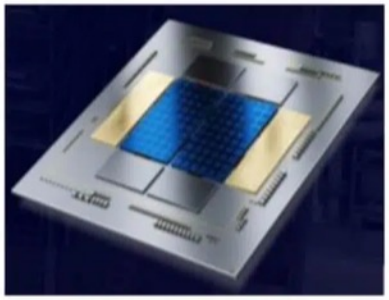
Chiplets (MCM)

Intel's Heterogenous System-in-Package Examples

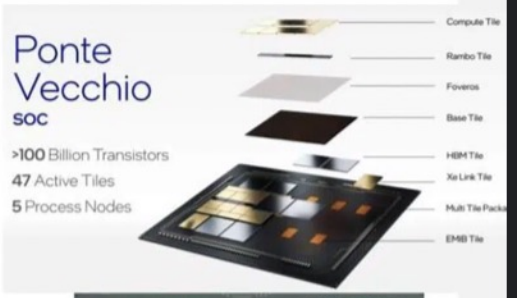
Intel Agilex™ (FPGA)
EMIB Technology

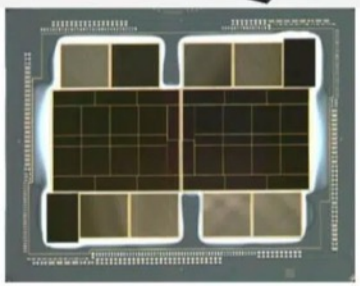


Intel Meteor Lake (Client)
Foveros Technology



Intel Granite Rapid (Server)
EMIB Technology





Ponte Vecchio – Xᵉ (HPC)
EMIB+Foveros Technologies

Heterogenous Packaging Technology Enabling Products Across All Market Segments

Sapphire Rapids is slated to be the first lineup from Intel to adopt the chiplet (MCM) or tiled design (plus some SKUs using on-die HBM) and Granite Rapids refining it. The former is expected to feature up to four (15-core, 1 disabled) tiles, resulting in a total core count of 56.

Intel New Processes

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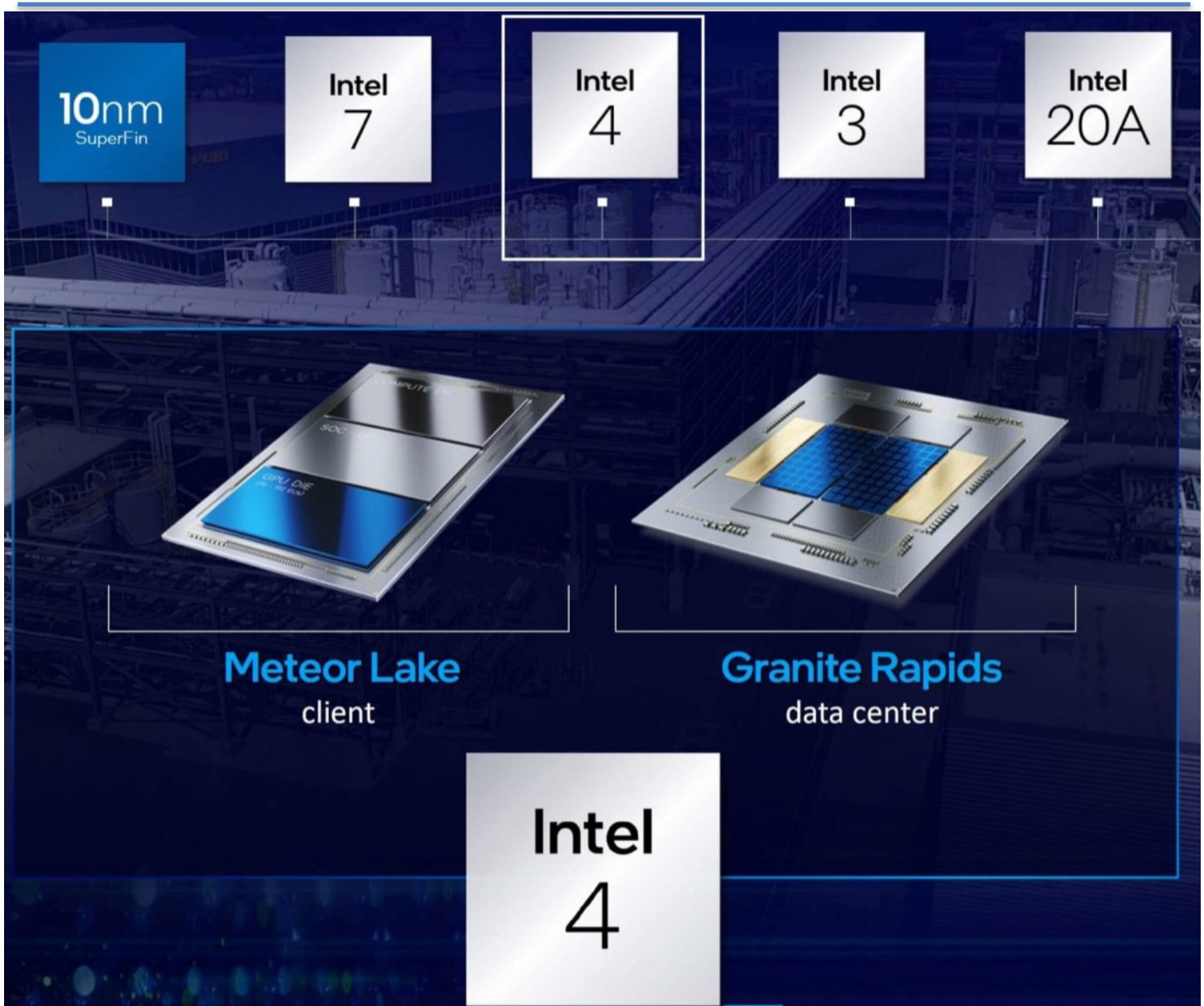

Intel's New Foundry Strategy

The central tenants of IDM 2.0 for Intel are:

1. Utilize the Intel internal factory network to build the majority of Intel's products internally.
2. Expand use of foundries so that all products have some level of foundry production.
3. Increasing engagement with TSMC, Samsung, GLOBALFOUNDRIES (GF) and UMC.
4. Plan to be a major foundry with US and European based manufacturing to balance the reliance on Asia.

There was slide that showed something like 80% of leading edge in Asia centered around Taiwan and South Korea, 15% in the US and 5% in Europe.

Intel’s New Foundry Strategy

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INDIE APP DEVELOPER
Jeff Drobman

Intel is said to have made a $2B takeover offer for chipmaker SiFive?!?!?

Daniel Nenni · Thursday at 11:51 AM

Daniel Nenni

ADMIN

Staff member

Thursday at 11:51 AM #1

Intel is said to have offered to purchase SiFive for more than $2B. SiFive, a designer of semiconductors, has been talking to its advisors to see how to proceed, according to a Bloomberg report, which cited people familiar. SiFive has received multiple bids from other interested parties and has also received offers for an investment. SiFive last raised more than $60M in a Series E financing round last year and was valued at about $500M, according to PitchBook. In June 2019, Qualcomm (NASDAQ:QCOM) participated in a $65.4M Series D round for SiFive, a fabless semiconductor company building customized silicon based on the open RISC-V instruction set architecture.

Wow, great move if it is true. If Intel wants to get into the foundry business doing turnkey ASICs is definitely the way to go. Intel already acquired eASIC. That way Intel can closely control and protect IP and make sure designs/chips are done the Intel way, absolutely.

The ASIC business has changed quite a over the last couple of years as fabless chip companies take control (Marvell, Broadcom, and Mediatek). Exciting times in the semiconductor ecosystem, absolutely!

Intel Process Nodes

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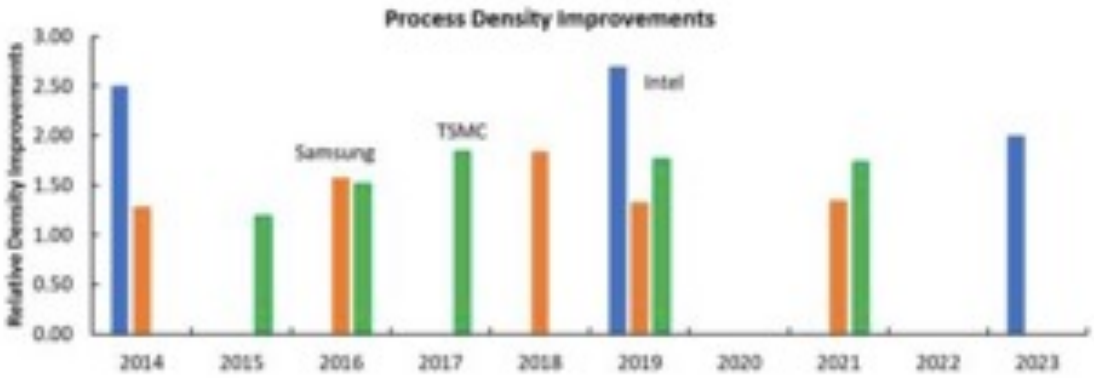
Slower Node Transitions Versus Foundries

IC KNOWLEDGE LLC

	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023
Intel	14nm					10nm				7nm
Samsung	14nm		10nm		7nm	5nm			3nm	
TSMC		16nm	10nm	7nm		5nm		3nm		2nm?

- Intel takes bigger density jumps but less often.
- TSMC and Samsung take smaller jumps more frequently, 5 nodes versus Intel's 3.



3/24/2021 4

Figure 4. Node Introductions.

Intel Process Nodes

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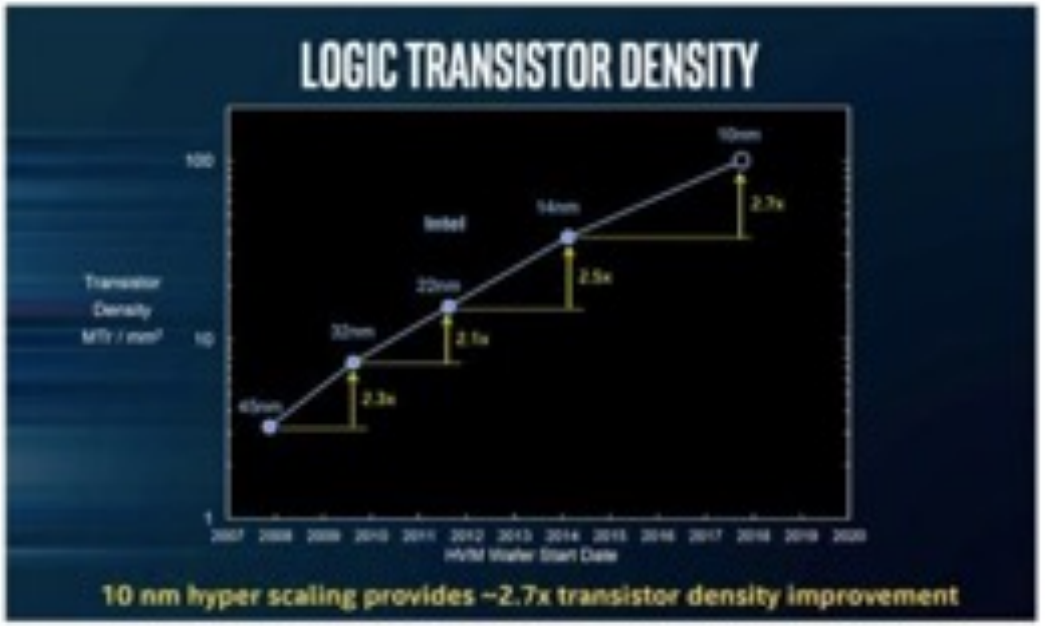
INDIE APP DEVELOPER
Jeff Drobman

Figure 3. illustrates Intel's hyper scaling.

Hyper Scaling

IC KNOWLEDGE LLC

- Intel started hyper scaling at the same time that scaling was getting harder.
- 2.5x density improvement for 14nm was 1 year late.
- 2.7x density improvement for 10nm was 2+ years late and still has yield issues.



Moore's Law Leadership, Mark Bohr, Intel Manufacturing Day 2017

Intel MOSFET

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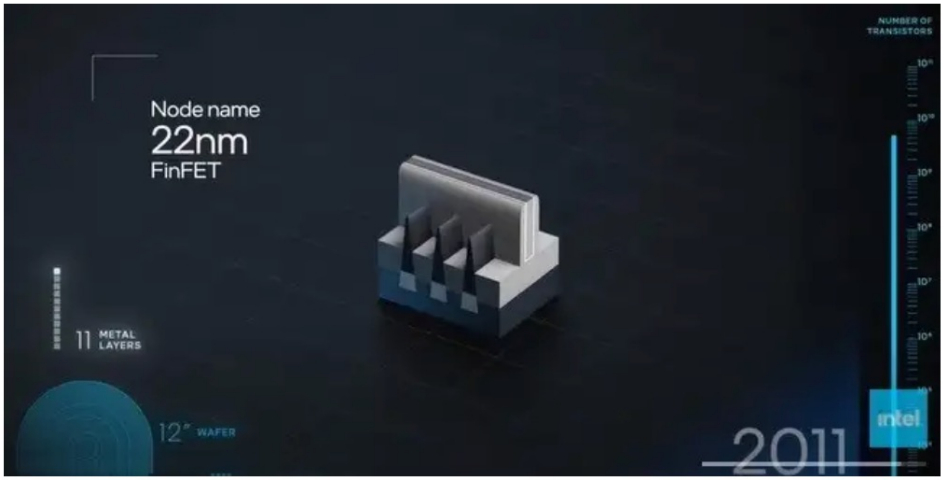
Intel video

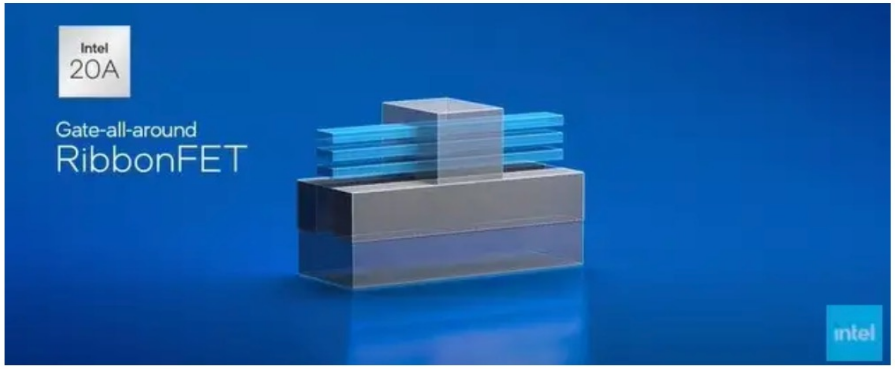
https://www.youtube.com/watch?v=Z7M8etXUEUU&t=47s

FinFET: 2011



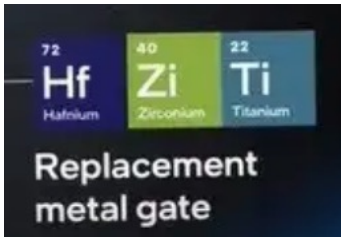
Intel amazed the industry with its aggressive adoption of a new transistor topology at the 22nm process node – the FinFET (also known as the "tri-gate FET").

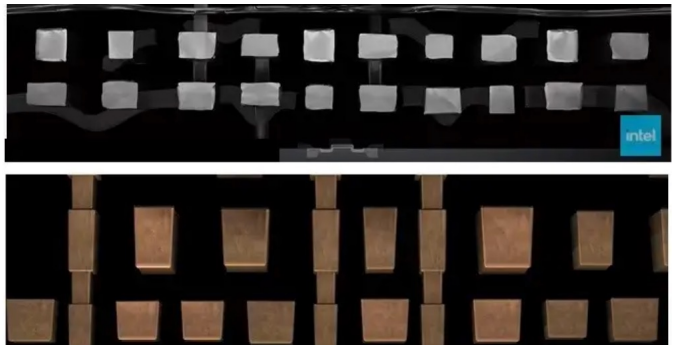
Gate-All Around (GAA) Ribbon FET: Intel 20A in 2024



To further improve the electrostatic gate control over the channel, another major evolution in the transistor topology is emerging to replace the FinFET. A gate-all-around configuration involves a vertical stack of electrically isolated silicon channels. The gate dielectric and gate input utilize an atomic layer deposition (ALD) process flow to surround all channel surfaces in the stack.

Intel will be releasing their GAA *Ribbon FET* 20A process in 1H 2024.





Intel's Newest Fabs

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Jeff Drobman

$**20B** in Ohio

Online end of **2025**

SATURDAY, JANUARY 22, 2022 A9

Intel to build chip factories in Ohio

Company will invest $20 billion as a global shortage highlights the risks of reliance on manufacturers in Asia.

Samsung in Texas

Chipmakers are diversifying their manufacturing sites in response to the shortages. Samsung said in November that it planned to build a $17-billion factory outside Austin, Texas.

Micron Technology, based in Boise, Idaho, said it would invest $150 billion globally over the next decade in developing its line of memory chips, with a potential U.S. manufacturing expansion if tax credits can help make up for the higher costs of American manufacturing.

Micron globally

10,000 jobs in Ohio

Two chip factories on the 1,000-acre site in Licking County, just east of Columbus, are expected to create 3,000 company jobs and 7,000 construction jobs, and to support tens of thousands of additional jobs for suppliers and partners, the com-

CHIPS for America Act

Lawmakers have been urging House and Senate leaders to fully fund a law meant to address the semiconductor shortage. They want Congress to fully fund the $52-billion CHIPS for America Act, allowing for stateside investment in semiconductor factories.

More on Intel's New Fabs

DR JEFF SOFTWARE
INDIE APP DEVELOPER
Jeff Drobman

Semi Wiki

$52B Chips for America is barely a rounding error

When you assume that the Chips for America act is a one time, one shot disbursement spread over a number of years and a number of companies it becomes clear that its not much against TSMC's spend.

It also does not compare to what China as a whole is spending on semiconductor technology.

Basically the US is being outclassed and outgunned by both China and Taiwan (probably part of China in the not too distant future).

Even if Intel got the whole $52B it still couldn't keep up as the spend would be over several years. Never mind that only $10B of the $52B is for fab projects with a $3B limit per project. Essentially the $52B will be spread so thin as to be ineffective versus the focused sharp spend of TSMC.

More on Intel's New Fabs

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Jeff Drobman

Semi Wiki

Can the US fabs being built make a difference?

Intel announced two fabs in Arizona at $10B each along with TSMC announcing a 5NM fab in Arizona which by the time its operational will be a drop in the bucket trailing edge fab perhaps meant to mollify the US.

Samsung has announced a $17B in Texas in addition to existing facilities there. It looks like Intel has chosen Ohio for its "megafab" project and Micron is eyeing North Carolina.

While details are scarce, it sounds like the Intel Ohio and Samsung Texas fabs are the most impactful on the US. Samsung would be somewhat less impactful as we assume that bleeding edge technology R&D will continue to be done in Korea making the Texas fab a "fast follower" much as the existing Samsung fab in Texas is today. That leaves Intel Ohio as the only trail blazing R&D facility in the US.

It also remains to be seen if the brain trust in Portland can either be moved or shared with Ohio or if Portland remains the R&D center with Ohio for production.

Intel's New Fab Equip.

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EUV from ASML

Intel Places Order for ASML's Extreme Ultraviolet Technology

04:49 AM EST, 01/19/2022 (MT Newswires) -- Intel (INTC) and ASML Holding (ASML) said Wednesday that the US chip maker has placed its first purchase order for ASML's TWINSCAN EXE:5200 extreme ultraviolet high-volume production system. The purchase ... (MT Newswires 04:49 AM ET 01/19/2022)

CHIPS Act in Ohio

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Sept 2022

CHIPS Act in Ohio

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Intel New Euro Fab

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INTEL CORP (INTC) (*47.70* *-0.01*) *I*

Market Chatter: Intel Reportedly Chooses Germany's Magdeburg as Location for New European Chip Factory

08:22 AM EST, 02/28/2022 (MT Newswires) -- Intel (INTC) has picked the city of Magdeburg in Germany as the location for a new European chip factory, Reuters reported on Saturday, citing an unnamed person familiar with the matter. The US ... (MT Newswires 08:22 AM ET 02/28/2022)

Read more

Intel – Italy Deal

Jeff Drobman
8-10-22

Italy, Intel close to $5 billion deal for chip assembly and packaging factory

I think Intel believes it can manage the cost in Italy that is comparable or cheaper to what other Intel assembly and packaging sites in Vietnam, Malaysia, Philippines, China, and Costa Rica. It's hard to believe it unless it's almost fully automated and use few workers.

Exclusive: Italy, Intel close to $5 billion deal for chip factory

Italy is close to clinching a deal initially worth $5 billion with Intel to build an advanced semiconductor packaging and assembly plant in the country, two sources briefed on discussions told Reuters on Thursday.

www.reuters.com

Intel News: Italy Fab

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Market Chatter: Intel, Italy Reportedly Pick Veneto Region as Location for Proposed Chip Factory

4:39 AM ET, 09/26/2022 - MT Newswires

04:39 AM EDT, 09/26/2022 (MT Newswires) -- Intel (INTC) and the Italian government have selected the town of Vigasio in the country's Veneto region as the location for a proposed chip factory, Reuters reported Sunday, citing anonymous sources familiar with the matter.

The factory, with an initial investment of some 4.5 billion euros ($4.36 billion), is part of the company's planned investment of 80 billion euros ($77.34 billion) to grow capacity in Europe, according to the report.

The new facility is expected to create 1,500 jobs and is slated to start operations between 2025 and 2027, Reuters reported.

Intel to Fab MediaTek

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Intel, MediaTek Enter Into Chip-Manufacturing Agreement

5:50 AM ET, 07/25/2022 - MT Newswires05:50 AM EDT, 07/25/2022 (MT Newswires) -- Intel (INTC) said Monday it entered into an agreement with MediaTek to manufacture chips using Intel Foundry Services.

The chipmaker said MediaTek aims to use Intel's process technologies to produce multiple chips for *smart edge* devices.

Financial details of the agreement were not disclosed.

Intel 14th Gen *Meteor Lake*

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SemiWiki.com
The Open Forum for Semiconductor Professionals

Rumor Mill 8-8-22

- Intel **14th Gen** *Meteor Lake* Rumored To Drop TSMC 3nm Node For tGPU, Might Be Used in **15th Gen** *Arrow Lake* CPUs

Meteor Lake is supposed to be **3 chipsets** - so they'll still need capacity for the I/O die and the iGPU from somewhere. N3 was only to be used for the iGPU where I/O was an older node. This seems like something specific to the iGPU (Intel design not ready) and/or N3 (capacity, timing, etc).

It is neither. ***Meteor Lake*** is yielding fine: Intel 4 CPU, TSMC N3 GPU, TSMC N5 base die and SoC.

Chips/Fabs

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Chip Design/Fab

Micron

- D/SRAM
- Flash

Micron Fab

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DRAM's Moore's Law Is Still Going Strong

Micron Technology pushes ahead with 35 percent density boost and does it without advanced lithography tool

SAMUEL K. MOORE
1 NOVEMBER 2022

Micron says it is shipping samples of **LPDDR5X** chips, memory made for power-constrained systems such as smartphones.
(LPDDR5X unpacked means: a revved-up twist on the low-power version of the 5th generation of the double data rate memory communications standard, capable of transferring 8.5 gigabits per second.)

It's the first chip made using Micron's new manufacturing process, called 1-beta, which the company says maintains the lead it took a year ago over rivals including Samsung and SK Hynix.

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Micron New US Fabs

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Micron Technology Plans US Manufacturing Investments, Welcomes Passage of Chips and Science Act

10:30 AM ET, 07/29/2022 - MT Newswires10:30 AM EDT, 07/29/2022 (MT Newswires) -- Micron Technology (MU) said Friday it plans to invest further in its US memory manufacturing capabilities as the semiconductor company welcomed the passage of the Chips and Science Act in Congress.

"The competitive incentives passed yesterday will allow Micron, *the only US-based manufacturer of memory*, to grow domestic production of memory significantly in the years ahead," the company said.

The legislation, which is expected to be signed into law in the coming days, will provide **$52 billion** in subsidies for domestic chip manufacturers and over **$100 billion** in technology and sciences investments, according to the Financial Times.

Micron in NY

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Chipmaker Micron to build $20 billion N.Y. factory amid semiconductor boom

Chipmaker Micron to build $20 billion N.Y. factory amid semiconductor boom

The company eventually could spend up to $100 billion over 20 years

BY JEANNE WHALEN
OCTOBER 4 AT 11:16 AM

Tech giant Micron said it will invest $20 billion in a new chip factory in Upstate New York, and up to $100 billion over twenty years if it decides to expand — another sign of a domestic semiconductor manufacturing boom.

Fabs

Jeff Drobman

Foundries

Global Foundries

Founded 2009

Global Foundries

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July 2021

GlobalFoundries

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4Q2021

Major 2021 Accomplishments and Key Fourth Quarter Business Highlights:

•In 2021, GF entered into 30 significant long-term customer agreements that provide assurance to our customers and provide revenue visibility to GF.

•In 2021, GF broke ground on a new fab on its **Singapore** campus, expanded capacity in Fab 1 (**Dresden**) by over 25%, and announced expansion plans for its most advanced manufacturing facility in **upstate New York**.

•GF set a "Journey to Zero Carbon" goal to reduce greenhouse gas emissions by 25% while expanding global manufacturing capacity.

•On October 28, 2021, GF began trading on **Nasdaq** Stock Market under the ticker "GFS."

•In the fourth quarter, GF announced an extension of its wafer supply agreement with **AMD**, increasing the number of chips GF will supply, as well as extending the terms of the agreement to secure supply through 2025.

•In the fourth quarter, **BMW** signed a direct supply assurance agreement with high-tech microchip developer INOVA Semiconductors and GF to secure long-term semiconductor supplies.

•In the fourth quarter, GF and **Ford** announced a non-binding strategic collaboration to advance semiconductor manufacturing and technology development within the US, aiming to boost chip supplies for Ford and the US auto industry.

AMD Orders Wafers

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News

ADVANCED MICRO DEVICES (AMD) (*154.36 +8.22*) *I*

Advanced Micro Devices to Buy $2.1 Billion of GlobalFoundries Wafers Under Expanded Deal

10:19 AM EST, 12/27/2021 (MT Newswires) -- GlobalFoundries (GFS) said Dec. 23 that semiconductor company Advanced Micro Devices (AMD) will now buy nearly $2.1 billion worth of its wafers starting 2022 through 2025 under an expanded deal. A wafer is ... (MT Newswires 10:19 AM ET 12/27/2021)

GlobalFoundries

12LP 12nm FinFET Technology

Ideal for high-performance, power-efficient SoCs in demanding, high-volume applications

GLOBALFOUNDRIES 12LP platform with 12nm 3D FinFET transistor technology provides best-in-class performance and power with significant cost advantages from 12nm area scaling. 12LP technology can provide up to 75% higher device performance and 60% lower total power compared to 28nm technologies. 12LP was **announced** in 2017 based on GF's proven existing 14nm offering, and the offering has transitioned from 14LPP to 12LP in 2018.

Global Foundries

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GlobalFoundries

From Wikipedia, the free encyclopedia

Coordinates: 37.415293°N 121.974448°W

> This article **contains content that is written like an advertisement**. Please help improve it by removing promotional content and inappropriate external links, and by adding encyclopedic content written from a neutral point of view. *(May 2021) (Learn how and when to remove this template message)*

GlobalFoundries Inc. (**GF**) is a United States-based semiconductor manufacturer headquartered in Malta, New York.[3] GlobalFoundries was created by the divestiture of the manufacturing arm of Advanced Micro Devices (AMD) and is owned by Mubadala Investment Company.

GlobalFoundries is the world's fourth largest semiconductor manufacturer[4][5] and produces chips for more than 7% of the $86 billion semiconductor manufacturing services industry. The company manufactures chips designed for high-growth markets such as mobility, automotive, computing and wired connectivity, consumer internet of things (IoT) and industrial.

As of 2021, GlobalFoundries is the only semiconductor manufacturer with simultaneous operations in Singapore, the European Union, and the United States. The company has one 200mm and one 300mm fabrication plants in Singapore; one 300 mm plant in Dresden, Germany; one 200 mm plant in Burlington, Vermont (where it is the largest private employer)[6] and two 300 mm plants in New York: one in East Fishkill and one in Malta.[7]

GlobalFoundries is a "Trusted Foundry" for the U.S. federal government and has similar designations in Singapore and Dresden including certified international Common Criteria standard (ISO 15408, CC Version 3.1).[8][9]

The company has more than 250 customers around the world and has 15,000 employees representing 92 nationalities in 14 countries. GlobalFoundries holds more than 10,000 patents and applications.

CEO Thomas Caulfield has said GlobalFoundries plans to become a publicly traded company in 2022.[10]

Contents [hide]

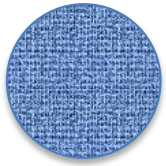
GlobalFoundries Inc.

GLOBALFOUNDRIES

Type	Private
Industry	Semiconductor manufacturer
Founded	March 2, 2009; 12 years ago
Headquarters	Malta, New York, U.S.
Key people	Dr. Thomas Caulfield (CEO)[1]
Products	Semiconductor
Number of employees	15,000
Parent	Mubadala Investment Company
Website	globalfoundries.com

Footnotes / references
[2]

200mm & 300mm wafers



Global Foundries

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Overview [edit]

On October 7, 2008, AMD announced it planned to go fabless and spin off their semiconductor manufacturing business into a new company temporarily called The Foundry Company. Mubadala announced their subsidiary Advanced Technology Investment Company (ATIC) agreed to pay $700 million to increase their stake in AMD's semiconductor manufacturing business to 55.6% (up from 8.1%). Mubadala will invest $314 million for 58 million new shares, increasing their stake in AMD to 19.3%. $1.2 billion of AMD's debt will be transferred to The Foundry Company.[11] On 8 December 2008, amendments were announced. AMD will own approximately 34.2% and ATIC will own approximately 65.8% of The Foundry Company.[12]

On March 4, 2009, GlobalFoundries was officially announced.[13] On September 7, 2009, ATIC announced it would acquire Chartered Semiconductor for S$2.5 billion (US$1.8 billion) and integrate Chartered Semiconductor into GlobalFoundries.[14] On January 13, 2010, GlobalFoundries announced it had finalized the integration of Chartered Semiconductor.[15]

On March 4, 2012, AMD announced they divested their final 14% stake in the company, which concluded AMD's multi-year plan to divest its manufacturing arm.[16]

On October 20, 2014, IBM announced the sale of its microelectronics business to GlobalFoundries.[17]

As of 2015, the firm owned ten fabrication plants. Fab 1 is in Dresden, Germany. Fabs 2 through 7 are in Singapore. Fabs 8 through 10 are in the northeast United States. These sites are supported by a global network of R&D, design enablement, and customer support in Singapore, China, Taiwan, Japan, India, the United States, Germany, and the United Kingdom.[18] In February 2017, the company announced a new 300 Fab [Fab 11] in China for growing semiconductor market in China.[19]

In 2016, GlobalFoundries licensed the 14 nm 14LPP FinFET process from Samsung Electronics. In 2018, GlobalFoundries developed the 12 nm 12LP node based on Samsung's 14 nm 14LPP process.[20]

On August 27, 2018, GlobalFoundries announced it had cancelled their 7LP process due to a strategy shift to focus on specialized processes instead of leading edge performance.[21]

On January 29, 2019, AMD announced an amended wafer supply agreement with GlobalFoundries. AMD now has full flexibility for wafer purchases from any foundry at 7 nm or beyond. AMD and GlobalFoundries agreed to commitments and pricing at 12 nm for 2019 through 2021.[22]

On May 20, 2019, Marvell announced it would acquire Avera Semi from GlobalFoundries for $650 million and potentially an additional $90 million. Avera Semi was GlobalFoundries' ASIC Solutions division, which had been a part of IBM's semiconductor manufacturing business.[23] On February 1, 2019, GlobalFoundries announced the $236 million sale of its Fab 3E in Tampines, Singapore, to Vanguard International Semiconductor (VIS) as part of their plan to exit the MEMS business by December 31, 2019.[24] on April 22, 2019, GlobalFoundries announced the $430 million sale of their Fab 10 in East Fishkill, New York, to ON Semiconductor. GlobalFoundries has received $100 million and will receive $330 million at the end of 2022 when ON Semiconductor will gain full operational control. The 300mm fab is capable of 65 nm to 40 nm and was a part of IBM.[25] On August 15, 2019, GlobalFoundries announced a multi-year supply agreement with Toppan Photomasks. The agreement included Toppan acquiring GlobalFoundries' Burlington photomask facility.[26]

Process Technology

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Fabs

- Spanning three continents across 14 locations

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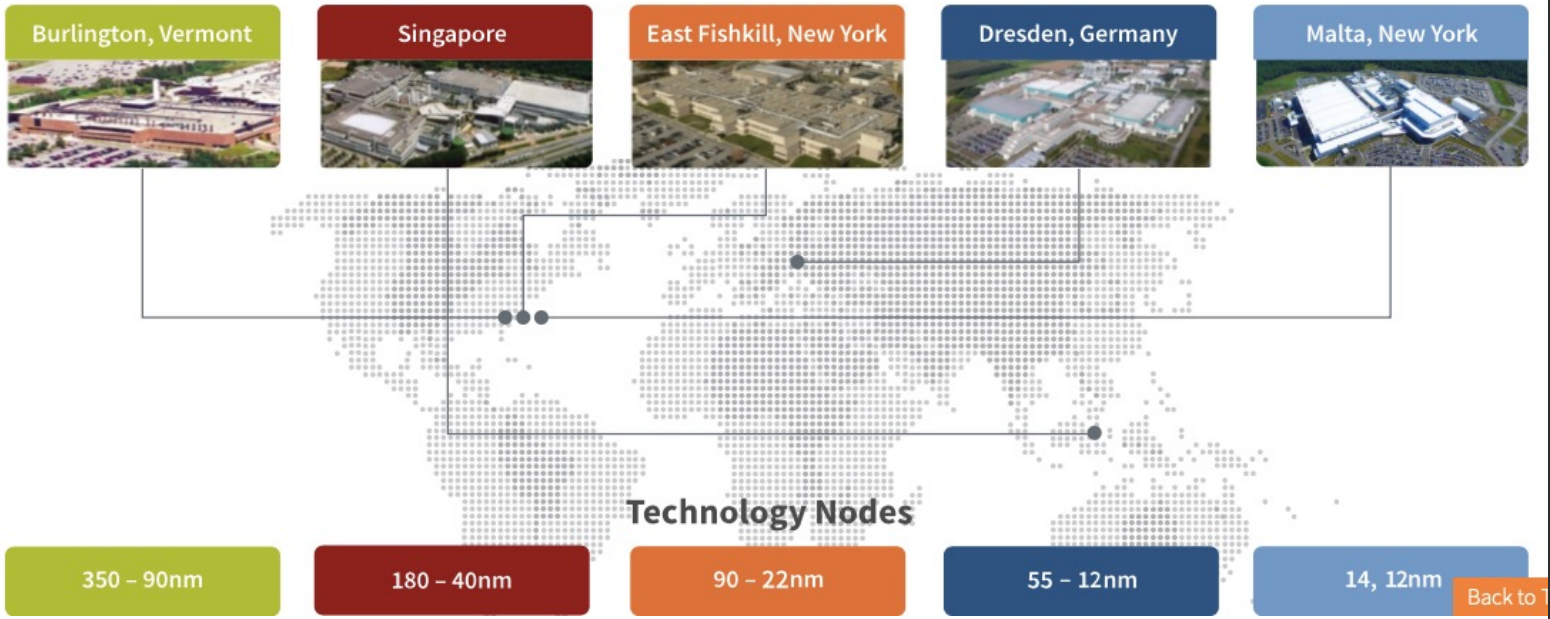
Our Manufacturing Capabilities



Back to T

Technology Solutions

CMOS

- Performance
- FDX
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- SiGe HP
- SiGe PA
- RF SOI
- RF CMOS

ASICs

Silicon Photonics

Global Foundries Fabs

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Fabrication foundry [edit]

Name	Wafer	Location		Process
Fab 1	300 mm	Dresden, Germany	51.125°N 13.716°E	55, 45, 40, 32, 28, 22 nm, 12 nm
Fab 2	200 mm	Woodlands, Singapore	1.436°N 103.766°E	600–350 nm
Fab 3/5	200 mm	Woodlands, Singapore	1.436°N 103.766°E	350–180 nm
Fab 3E	200 mm	Tampines, Singapore (2019: sold to VIS)	1.371°N 103.929°E	180 nm
Fab 6	200 mm	Woodlands, Singapore (converted to 300 mm and merged into Fab 7)	1.436°N 103.766°E	180–110 nm
Fab 7	300 mm	Woodlands, Singapore	1.436°N 103.766°E	130–40 nm
Fab 8	300 mm	Luther Forest Technology Campus, Saratoga County, New York, United States	42.970°N 73.756°W	28, 20, 14 nm
Fab 9	200 mm	Essex Junction, Vermont, United States	44.48°N 73.10°W[44]	350–90 nm
Fab 10	300 mm	East Fishkill, New York, United States (2019: started transfer to ON Semiconductor)	41.540°N 73.822°W	90–22 nm, 14 nm

Global Foundries Financials

Written by

KHAVEEN Investments

Khaveen Investments

Khaveen Investments is a Global Macro Quantamental Hedge Fund managing a tactical asset-allocated portfolio... more

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Revenue Forecast ($ mln)	2018	2019	2020	2021	2022F	2023F	2024F
Wafer Shipments 300mm equivalents ('000s) ('a')	1,863	1,758	2,030	2,374	2,586	3,036	3,358
Growth %		-5.6%	15.5%	16.9%	8.9%	17.4%	11%
Wafer ASP (Revenue per wafer) ('b')	3,326	3,306	2,389	2,774	3,051	3,034	3,017
Growth %		-0.6%	-27.7%	16.1%	10.0%	-0.6%	-0.6%
Revenue ($ mln) ('c')	**6,196**	**5,813**	**4,851**	**6,585**	**7,890**	**9,212**	**10,133**
Growth %		**-6.2%**	**-16.6%**	**35.8%**	**19.8%**	**16.7%**	**10.0%**

Foundries

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TSMC

Founded 1987

Chip Shortage

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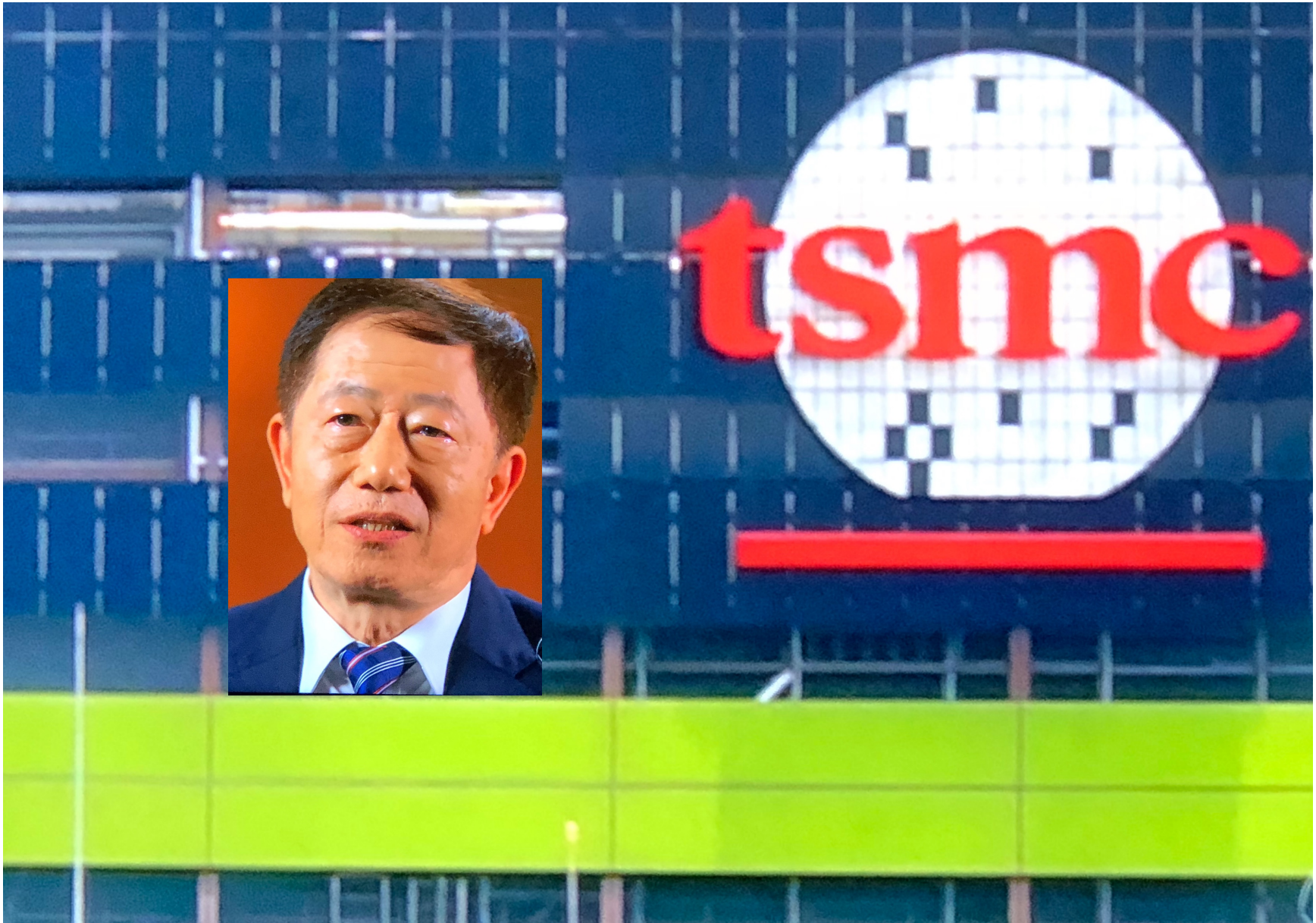

Chip Shortage

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- TSMC also building new fabs (6) in AZ

TSMC

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Table 4 – TSMC Customer Share of Revenues 2019-2021			
	2019	2020	2021
Apple	24.0%	24.2%	25.4%
Hi-Silicon	15.0%	12.8%	0.0%
Qualcomm	6.1%	9.8%	7.6%
NVIDIA	7.6%	7.7%	5.8%
Broadcom	7.7%	7.6%	8.1%
AMD	4.0%	7.3%	9.2%
Intel	5.2%	6.0%	7.2%
Mediatek	4.3%	5.9%	8.2%
Source: The Information Network (www.theinformationnet.com)			

TSMC Process Revenue

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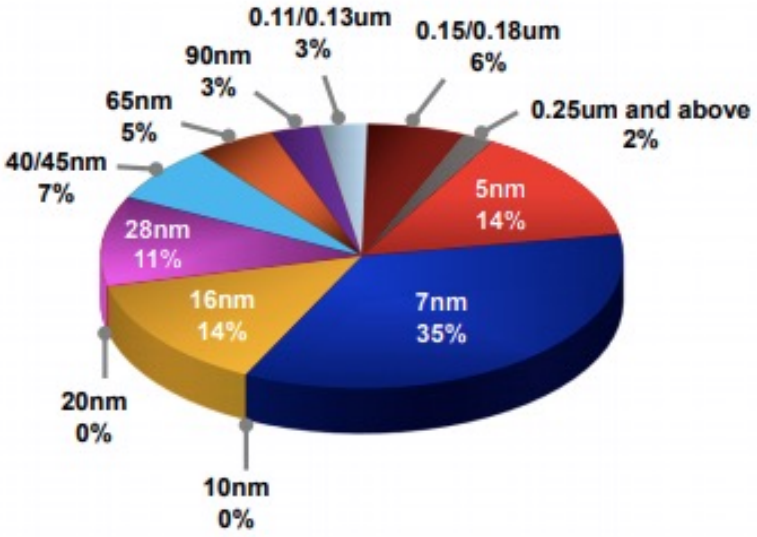
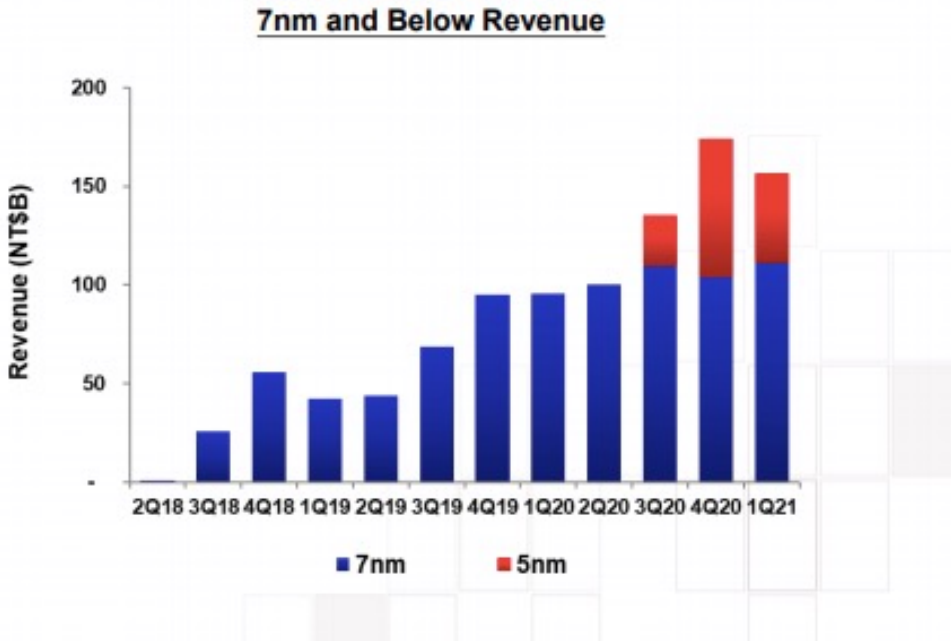
tsmc
Unleash Innovation

1Q21 Revenue by Technology





TSMC vs Samsung 5nm

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	Samsung[24]	TSMC[25]
Process name (nm)	5LPE	N5
Transistor density (MTr/mm^2)	127	173[27]
SRAM bit-cell size (μm^2)	0.026	0.017–0.019
Transistor gate pitch (nm)	57	48
Interconnect pitch (nm)	36	28[29]

TSMC vs Samsung 5/7nm

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5nm

Samsung[24]	TSMC[25]
5LPE	N5
127	173[27]
0.026	0.017–0.019
57	48
36	28[29]

These are real sizes for 7nm node from TSMC, Samsun

7nm

	TSMC N7FF[71]	Samsung 7LPP[72][73]	Intel 10 nm
Transistor density (MTr/mm^2)	96.5[75]	95.3 (7LPE)[76] 81.07 (57PP) 85.57 (54PP)[77]	100.76[78]
SRAM bit-cell size	0.027 µm^2[79]	0.0262 µm^2[79]	0.0312 µm^2
Transistor Gate Pitch	54 nm	54 nm	54 nm
Transistor Fin Pitch	Unknown	27 nm	34 nm
Transistor Fin Height	Unknown	Unknown	53 nm
Minimum (metal) pitch	40 nm	46 nm	36 nm

TSMC's New Fabs in US

Jeff Drobman

TSMC

TSMC Plans Six Wafer Fabs in Arizona

by Scotten Jones on 03-10-2021 at 10:00 am
Categories: Foundries, TSMC
7 Comments

Larger than Taiwan?

$35B

There are reports in the media that TSMC is now planning six Fabs in Arizona (the image above is Fab 18 in Taiwan). The original post I saw referred to a Megafab and claimed six fabs with 100,000 wafers per month of capacity (wpm) for $35 billion dollars. The report further claimed it would be larger than TSMC fabs in Taiwan.

TSMC New Fabs in AZ

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Now here is a YouTube channel doing the same thing at TSMC's new Phoenix fab.

TSMC New Fabs in AZ

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https://www.youtube.com/watch?v=GU87SH5e0eI

https://semiwiki.com/forum/index.php?threads/tsmc-mega-factory-north-phoenix-video-5.15643/

TSMC MEGA Factory North Phoenix Video 5

TSMC on Moore's Law

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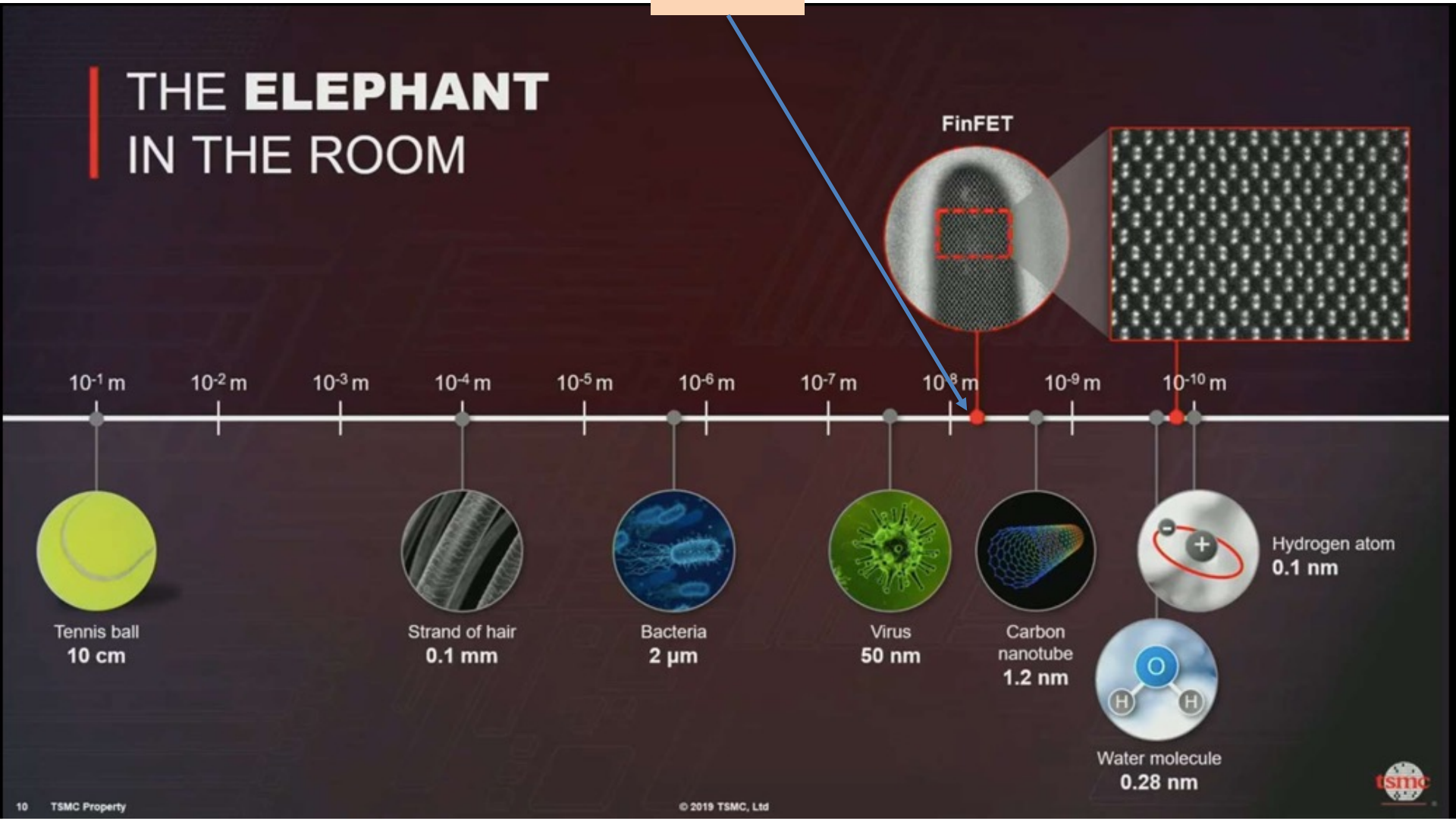
7-10 nm



TSMC Roadmap

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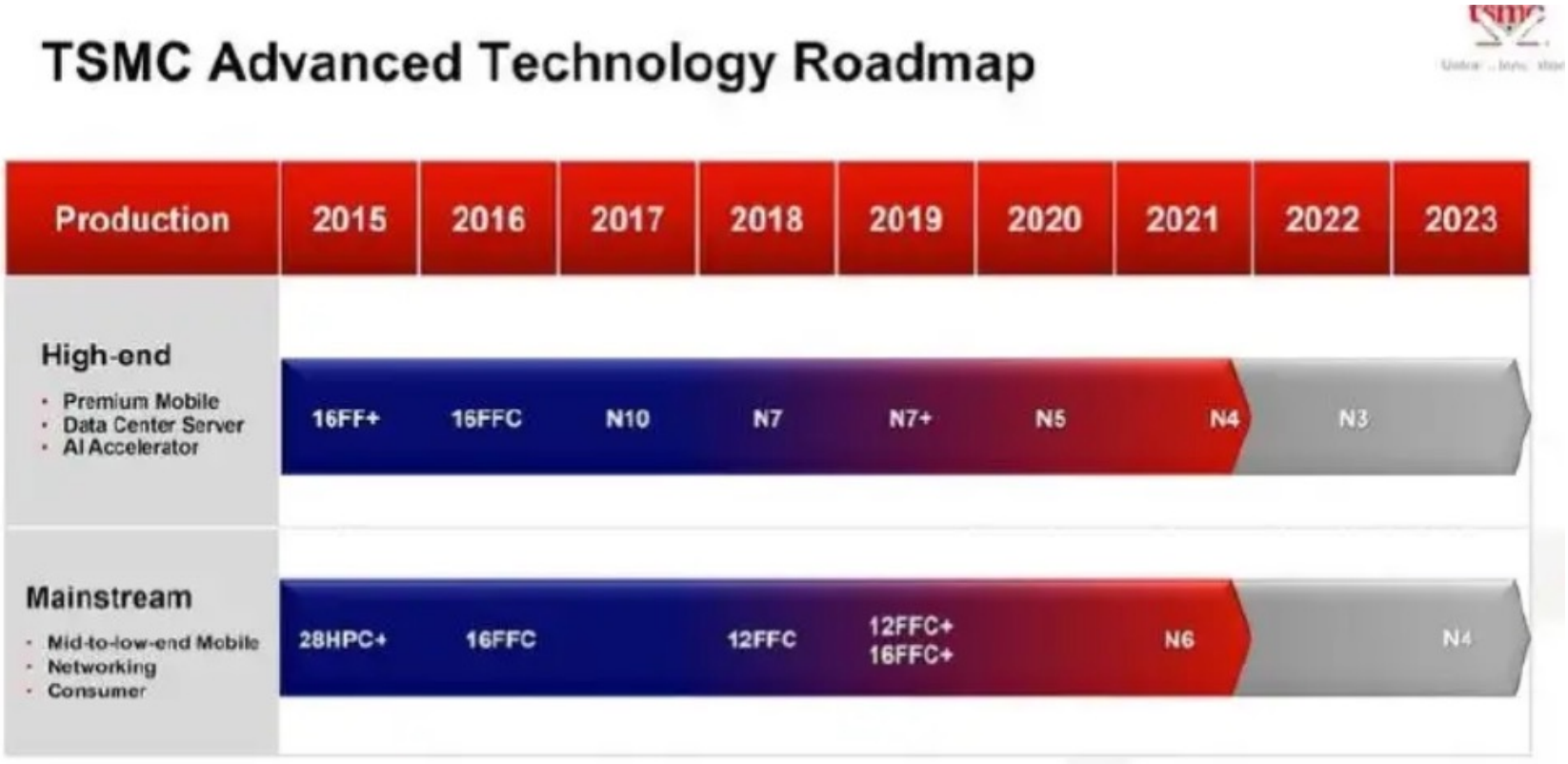
June 2021



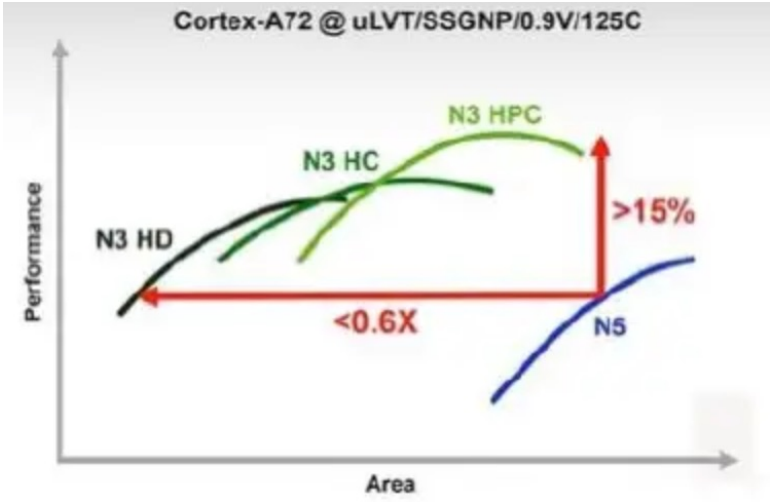
TSMC Roadmap

June 2021

N7+ represents the introduction of EUV lithography to the baseline N7 process. N5 has been in volume production since 2020.

N3 will remain a FinFET-based technology offering, with volume production starting in 2H2022. Compared to N5, N3 will provide:

- +10-15% performance (iso-power)
- -25-30% power (iso-performance)
- +70% logic density
- +20% SRAM density
- +10% analog density



TSMC foundation IP has commonly offered two standard cell libraries (of different track heights) to address the unique performance and logic density of the HPC and mobile segments. For N3, the need for "full coverage" of the performance/power (and supply voltage domain) range has led to the introduction of a third standard cell library, as depicted below.

TSMC Roadmap- RF

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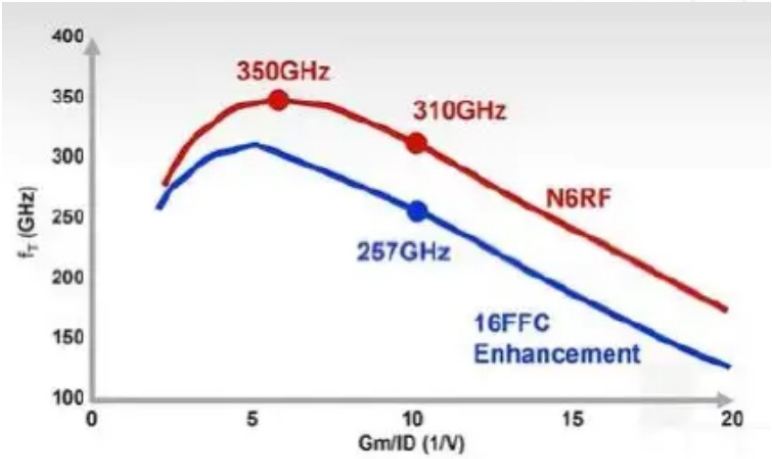
Jeff Drobman

June 2021

TSMC RF Technology Roadmap

Production		2018	2019	2020	2021	2022	2023
General RF (<=10GHz)	Premium	16FFC RF Enh I			N6RF		N6RF Enh
	Mainstream	28HPC+ RF V1.0			22ULP/ULL RF V1.2		
mmWave RF (>=24GHz)	Premium	16FFC RF Enh I					
	Mainstream	22ULP/ULL RF V1.2					
RF Frontend (<= 10GHz)	Premium	N40SOI			N40SOI Enh		
	Mainstream	0.13SOI					

General RF applications: 5G (sub 6 GHz)/4G RF transceiver, WLAN, Bluetooth and etc.
mmWave RF applications: 5G mmWave FEM, automotive radar and etc.
RF Frontend applications: LNA and switch



TSMC Roadmap: Packaging

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INDIE APP DEVELOPER
Jeff Drobman

New Plant June 2021

TSMC's planned U.S. plant would involve its latest 3D stacking technologies to arrange chips with different functions in one package, sources told Nikkei Asia.

TSMC is also building an advanced chip packaging facility in the Taiwanese city of Miaoli that is set to go into production in 2022. Advanced Micro Devices and Google will be among the first customers, Nikkei Asia has reported.

The facility would be TSMC's first chip packaging plant outside of Taiwan so this is a very big deal. Chip packaging is an increasingly competitive field but TSMC is on par or even ahead of Intel and Samsung in a short amount of time. The big TSMC advantage is the tight collaboration with big name customers and ecosystem partners.

Per the 2021 TSMC Symposium:

In 2020, TSMC extended their support to encompass 281 distinct process technologies, shipping 11,617 products to 510 customers. As in previous years, TSMC proudly stated “we have never shut down a fab.”

Current capacity in 2020 exceeds 12M (12” equivalent) wafers, with expansion investments for both advanced (digital) and specialty process nodes.

TSMC plans to invest a total of US$100 billion over the next three years, including a US$30 billion capital expenditure this year, to support global customer needs.

TSMC’s global 2020 revenue was $47.78B – the $30B annual commit to fab expansion certainly would suggest an expectation of significant and extended semiconductor market growth, especially for the 7nm and 5nm process families. For example, new tapeouts (NTOs) for the 7nm family will be up 60% in 2021.

TSMC has begun construction of a US fab in Phoenix, AZ – volume production of the N5 process will commence in 2024 (~20K wafers per month).

TSMC + ARM in 3D

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ARM quad core A72

7nm ***chiplet***

Technology

3D Multi-chip Systems

The world's largest foundry joined with partner Arm to announce their new 7nm chiplet system using TSMC's advanced packaging at TSMC's Open Innovation Platform Ecosystem Forum in Santa Clara, Calif., last week.

Rather than the typical SoC with system components arranged on a single die, a chiplet system is optimized for modern HPC processors that partition large multi-core designs into smaller chipsets. This approach allows each chiplet — each die in a package of multiple dice — to be built in different process technologies. The approach is expected to deliver better yields and overall cost-effectiveness.

The TSMC/Arm system is a dual-chiplet implemented in 7nm, with each chiplet containing four Arm Cortex-A72 processors and an on-die interconnect mesh bus. The die-to-die inter-chiplet connection features scalable 0.56pJ/bit (pico-Joules per bit) power efficiency, 1.6Tbps/mm^2 (terabits per second per square millimeter) bandwidth density, and 0.3V LIPINCON low-voltage interface reaching 8GT/s (giga transactions per second) and 320 Gpbps bandwidth.

"TSMC has the most advanced semiconductor nodes in production, and that gives them some advantages from a silicon side," TechSearch President Jan Vardaman told EE Times. "From a packaging side, each company has an approach that could deliver a similar solution, with TSMC and Intel releasing the most information so far."

TSMC, Arm Show 3DIC Made of Chiplets

Source: EE Times (02 Oct 2019)

TSMC New Techs

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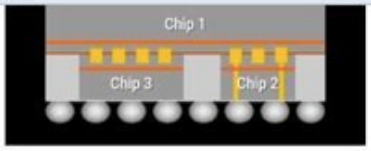
Abbreviation	What does it stand for?	What is it?
3DIC	Three-dimensional integrated circuit	
CoWoS	Chip on Wafer on Substrate	TSMC's CoWoS (Chip-on-Wafer-on-Substrate) packaging technology integrates logic and memory chips in a three-dimensional configuration. CoWoS packaged chips are used in artificial intelligence, cloud computing, data center and super computer applications.
InFO	Integrated Fan-Out	TSMC's InFO (Integrated Fan-Out) packaging technology eliminates the substrate used in traditional electronic packages, enabling smaller size, lower power and higher interconnect density.
LIPNCON	Low voltage In Package INterConect	Low-voltage-In-Package-INterCONnect (LIPINCON) is a proprietary system interconnect architecture that facilitates data transmission across all linked components. LIPINCON is an interconnect architecture designed for chiplet designs with advanced packaging technologies such as InFO and CoWoS.
RDL	Redistribution Layer	A redistribution layer (RDL) is an extra metal layer on a chip that makes the IO pads of an integrated circuit available in other locations of the chip, for better access to the pads where necessary.
SoIC		SoIC is a frontend wafer-process that integrates multi-chip, multi-tier, multi-function and mix-and-match technologies to enable high speed, high bandwidth, low power, high pitch density and minimal footprint and stack-height heterogeneous 3DIC integration.

SoC

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TSMC operates four major 300mm manufacturing sites in Taiwan and one in China. The four sites in Taiwan are all GigagFab sites, Fab 12, Fab 14, Fab 15 and Fab 18 are each made up of 6 or 7 wafers fabs sharing central facility plants. This Gigafab approach is believed to reduce construction costs by about 25% versus building a single stand-alone fab. The china fab location is smaller with 2 fabs at one location but the fab was equipped with used equipment transferred from fabs in Taiwan because the fab is trailing edge. If TSMC really builds a single US fab running 20,000 wpm the resulting cost to produce a wafer will be roughly 1.3% higher than for a GigaFab location due to higher construction costs. I believe it is unlikely the site will be equipped with used equipment transferred from Taiwan. The cost to build and equip the fab for 20,000 wpm should be approximately $5.4 billion dollars.

Gigafabs

Locating a fab in the US versus Taiwan will result in the fab incurring US labor and utility costs, this will add approximately 3.4% to the wafer manufacturing cost.

The capacity of the fab is also smaller than a "typical" fab at advanced nodes, the three 5nm fabs TSMC is operating or planning for Taiwan are all 30,000 wpm. A 20,000 wpm fab will have an approximately 3.8% increase in costs versus a 30,000 wpm fab under the same conditions.

20-30K wpm

In total, wafers produced at the TSMC Arizona fab will be approximately 7% more expensive to manufacturer than a wafer made in Fab 18 in Taiwan. This does not account for the impact of taxes that are likely to be higher in the US than in Taiwan.

In the announcement TSMC has said the total spending on the project between 2021 and 2029 would be $12 billion dollars. That leaves money for a future expansion or conversion to 3nm. That would be almost enough money to add a second 20,000 wpm fab running 3nm as one possible example.

$12B

In summary the "announced" fab would likely be TSMC's highest cost production site. It will be interesting to see if the fab materializes.

TSMC in US

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Cost Analysis of the Proposed TSMC US Fab

by Scotten Jones on 05-19-2020 at 10:00 am
Categories: IC Knowledge, Semiconductor Services, TSMC
29 Comments

On May 15th TSMC "announced its intention to build and operate an advanced semiconductor fab in the United States with the mutual understanding and commitment to support from the U.S. federal government and the State of Arizona."

The fab will run TSMC's 5nm technology and have a capacity of 20,000 wafers per month (wpm). Construction is planned to start in 2021 and production is targeted for 2024. Total spending on the project including capital expenditure will be $12 billion dollars between 2021 and 2029.

This announcement is undoubtedly the result of intense pressure on TSMC by the US government and it is also coming out today that TSMC will stop taking orders from Huawei also under pressure from the US.

New Chip Fabs

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THE VERGE

TSMC in Arizona

The chip-making industry has production capacity increases planned, but many of the new plants won't be online anytime soon. TSMC and Sony's new $7 billion chip factory in Japan won't see production start until the end of 2024, the same year as TSMC's new $12 billion Arizona plant. TSMC has said it plans to invest over $100 billion in new chip factories over the next three years, while Intel plans to spend a similar amount over the next decade on investments in the US and Europe.

New Chip Fabs

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Quora

TSMC in Arizona

What is Intel's plan to regain chip market dominance from the likes of TSMC? What are its chances of doing so?

Jeff Drobman, Lecturer at California State University, Northridge (2016-present)

Answered just now

Apple's mobile A14/15 and MacBook M1 chips are fabbed by TSMC at 5nm. TSMC is the world leader in process density — first to 5nm, with Samsung a close 2nd, and are now testing 3nm. Intel has now joined AMD in using TSMC to fab its high-end chips at 7nm and 5nm. Intel has new plans to catch up, according to this estimate (see slide).

TSMC 4nm

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Apple Orders 4nm Chip Production for Next-Generation Macs

Tuesday March 30, 2021 12:35 am PDT by Sami Fathi

Apple has booked the initial production capacity of 4nm chips with long-time supplier TSMC for its next-generation Apple silicon, according to industry sources cited in a new report today from *DigiTimes*.

Apple & TSMC

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> *Apple has already booked the initial capacity of TSMC's N4 for its new-generation Mac series, the sources indicated. Apple has also contracted TSMC to make its next-generation iPhone processor dubbed A15, built using the foundry's N5 Plus or N5P process node, the sources said.*
>
> *TSMC is expected to kick off production for Apple's A15 chip that will power the upcoming iPhone 13 series by the end of May, the sources noted.*

The latest Apple silicon, the M1 chip, is the first of its kind in the industry based on the 5nm process. The A14 Bionic chip in the iPad Air and iPhone 12 lineup is also based on the 5nm process. According to the report, Apple is already looking to the 4nm chip process for its next-generation Apple silicon.

A timeframe for when these new 4nm chips will debut isn't provided, but *DigiTimes* does report that TSMC will move to volume production of the new process in Q4 of 2021, ahead of the previously set 2022 timeframe. Additionally, Apple plans to use an enhanced version of the 5nm process for the A15 chip in the iPhone 13, with production set to get underway by the end of May.

The smaller process reduces the chips' actual footprint and provides better efficiency and performance. Apple's expected to launch multiple new Macs this year with more powerful Apple silicon chips; however, there's no indication that any will be based on the 4nm process.

TSMC $ Apple

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Taiwan Semiconductor asked for 2023 price increase from Apple, tech giant said no: report

Sep 28, 2022 11:23 AM ET | **Taiwan Semiconductor Manufacturing Company Limited (TSM)** | Chris Ciaccia, SA News Editor

Taiwan Semiconductor (NYSE:TSM) is slated to raise prices on its customers starting in 2023, but the company's largest customer, Apple (NASDAQ:AAPL), has reportedly told the global foundry no deal.

According to Chinese news outlet Economic Daily News, Taiwan Semiconductor (TSM) wanted to increase the price of the process for its 3 nm process by 3%, which may be used in the A17 chip in some of Apple's (AAPL) Mac computers and perhaps next year's iPhone. However, the tech giant refused and said no, the news outlet said, citing sources.

In May, it was reported that Taiwan Semiconductor Manufacturing (TSM) had started to tell some of its customers that it will raise its prices between 5% and 9%, starting next year, due to inflation concerns, rising costs and its expansion.

Cupertino, California-based Apple (AAPL) is Taiwan Semiconductor's (TSM) largest customer and some reports have suggested that it accounts for as much as 25% of the global foundry's annual revenue.

25%

Apple

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Technology

Apple Prepares to Get Made-in-US Chips in Pivot From Asia

- Company plans to source chips from Arizona plant in 2024
- CEO Tim Cook makes comments about expansion during meeting

TSMC new fabs in Arizona will open in 2024

TSMC 3nm

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SemiWiki.com
The Open Forum for Semiconductor Professionals

8-17-22

TSMC's Initial 3nm HVM Yield To Be Better Than Its 5nm

TSMC **N3e** is the HPC version for Intel, AMD, Nvidia, etc... The SoC companies Apple, Mediatek, will use **N3**. Please remember that TSMC sets expectations on the conservative so they don't disappoint. According to my sources N3 for Apple was frozen in December and the N3e process is now frozen with HVM starting in 1H 2023.

- Apple now in production (HVM) with **4nm**

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TSMC at VLSI Conf 2021

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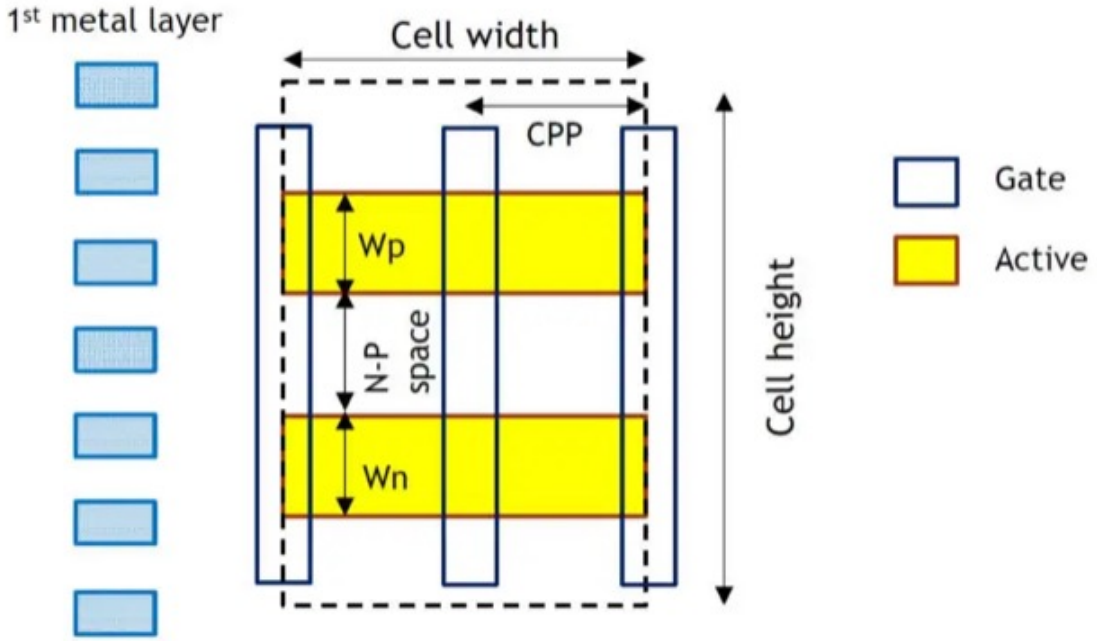
IC Knowledge

VLSI Symposium – TSMC and Imec on Advanced Process and Devices Technology Toward 2nm

by Scotten Jones on 07-02-2021 at 6:00 am
Categories: Events, IC Knowledge, Semiconductor Services, TSMC

CMOS Density Improvement

- Logic standard cell area ~ CPP x Cell height



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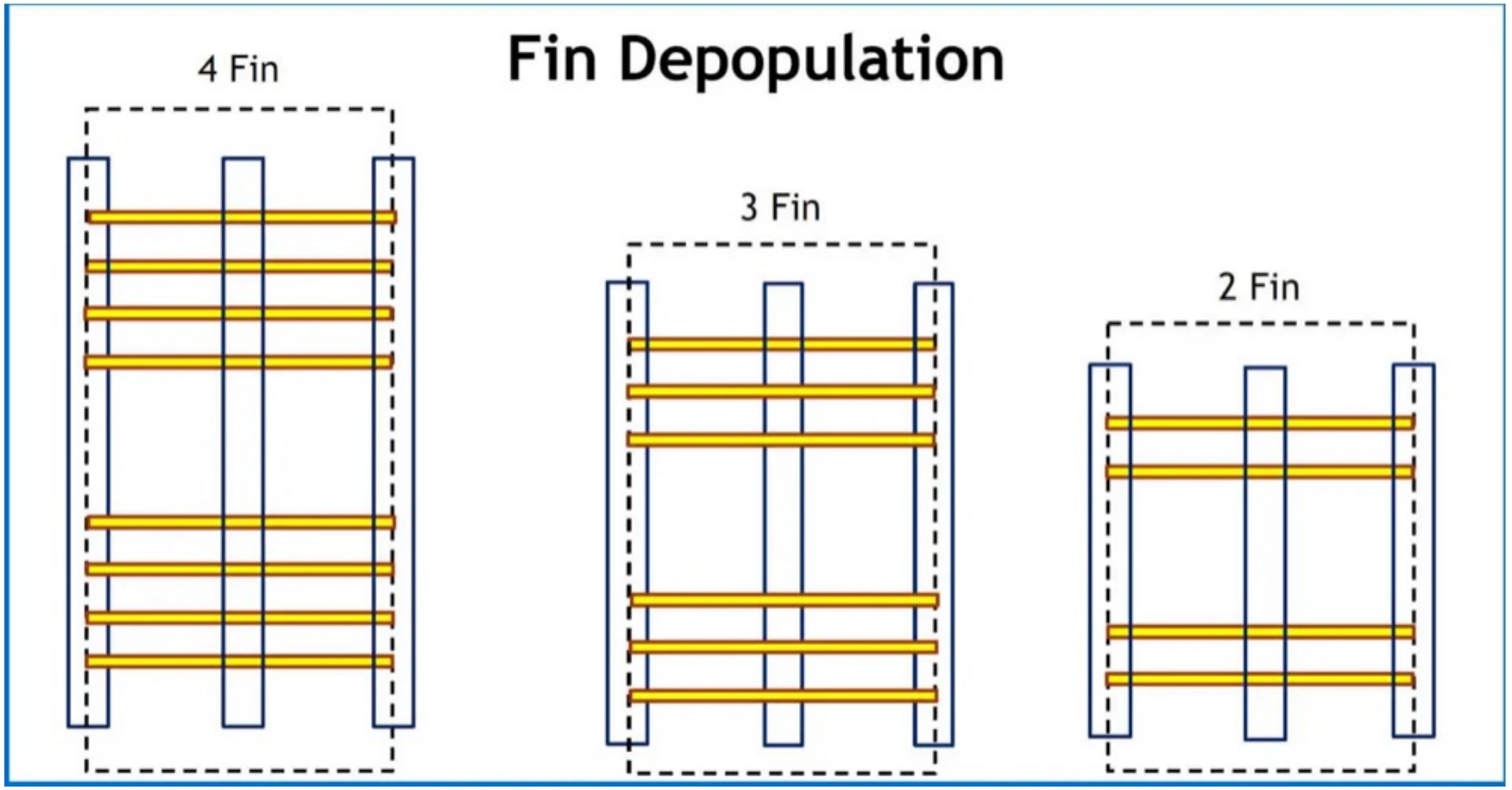

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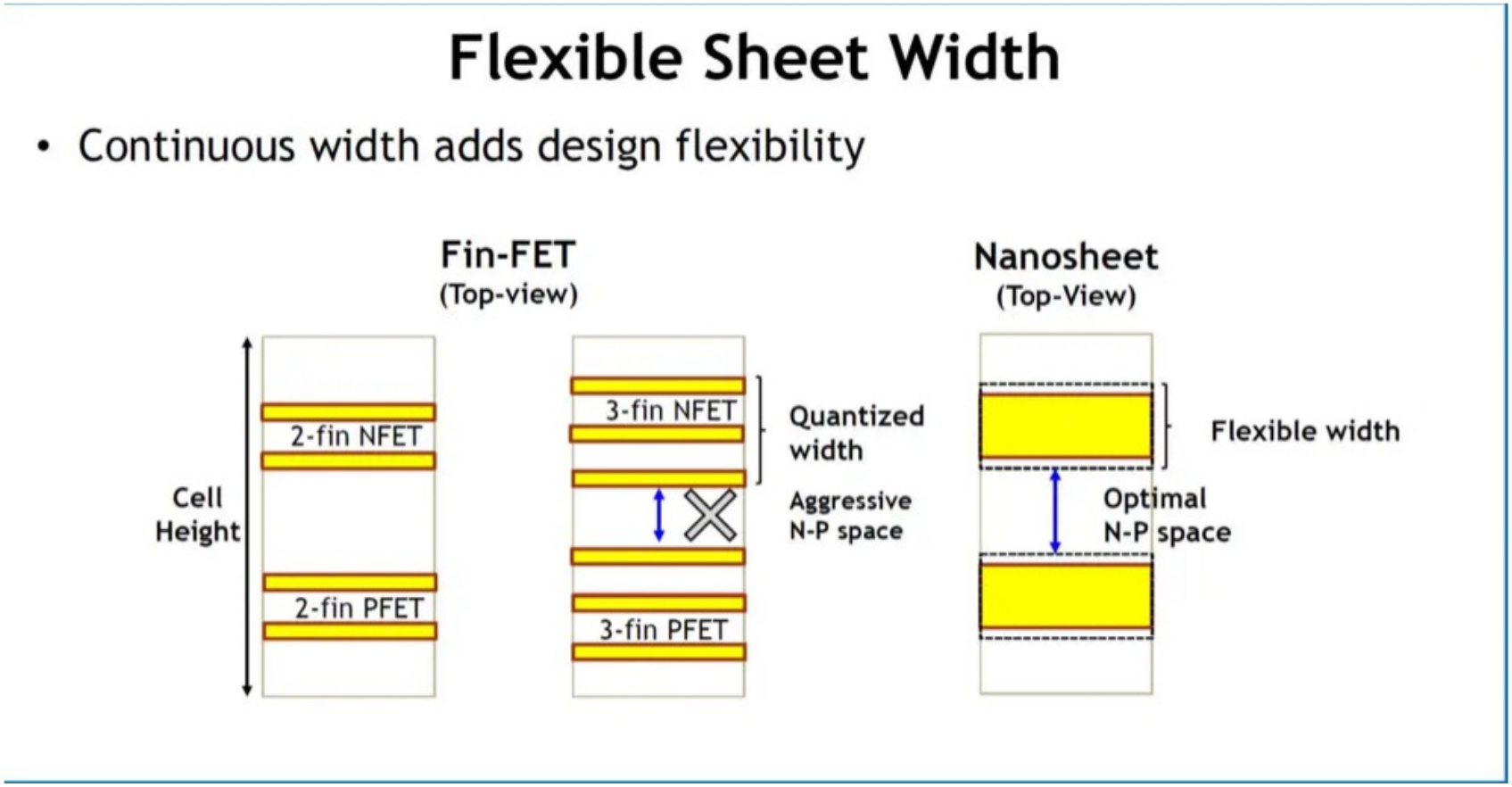

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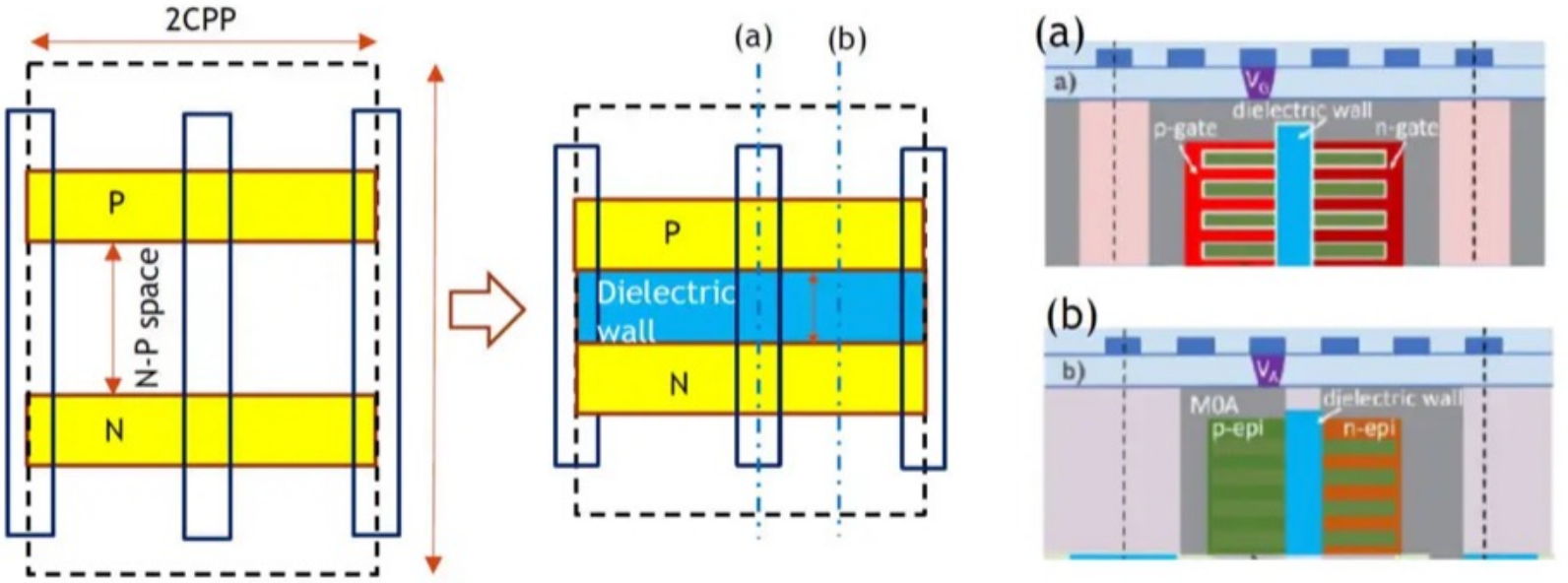
Standard Cell height Scaling: Forksheet

- Dielectric wall between N and P: gate isolation, S/D isolation, end cap ↓



Challenge: Short channel control

P. Weckx et.al., 2019 IEDM (IMEC)

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by Scotten Jones on 07-02-2021 at 6:00 am
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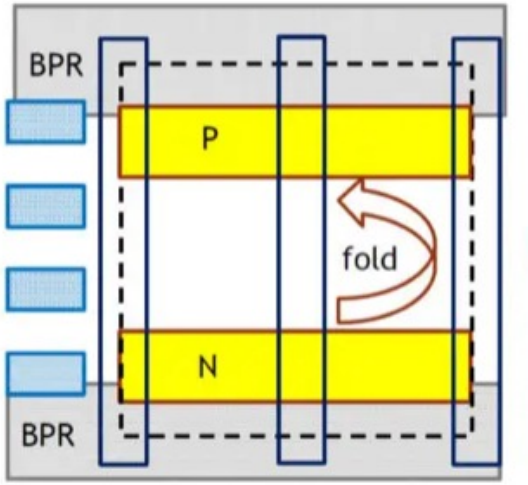
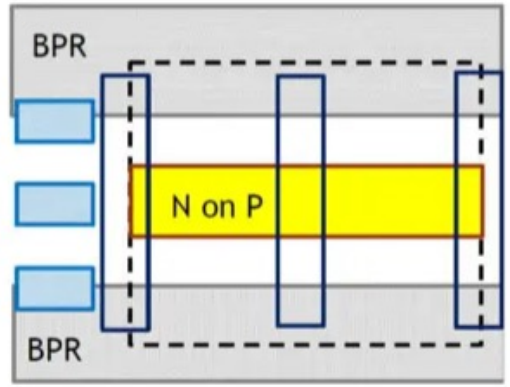
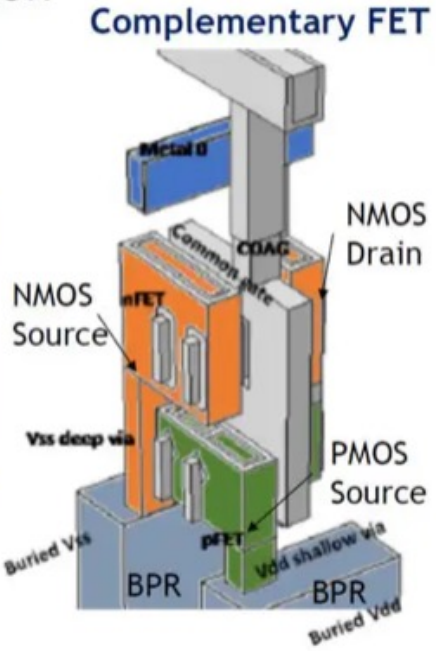
Stacked CMOS

- NMOS and PMOS stacking enables further CH reduction
  - CH limited by signal routing tracks (>=3) and metal pitch







J. Ryckaert et.al. 2018 VLSI (IMEC)

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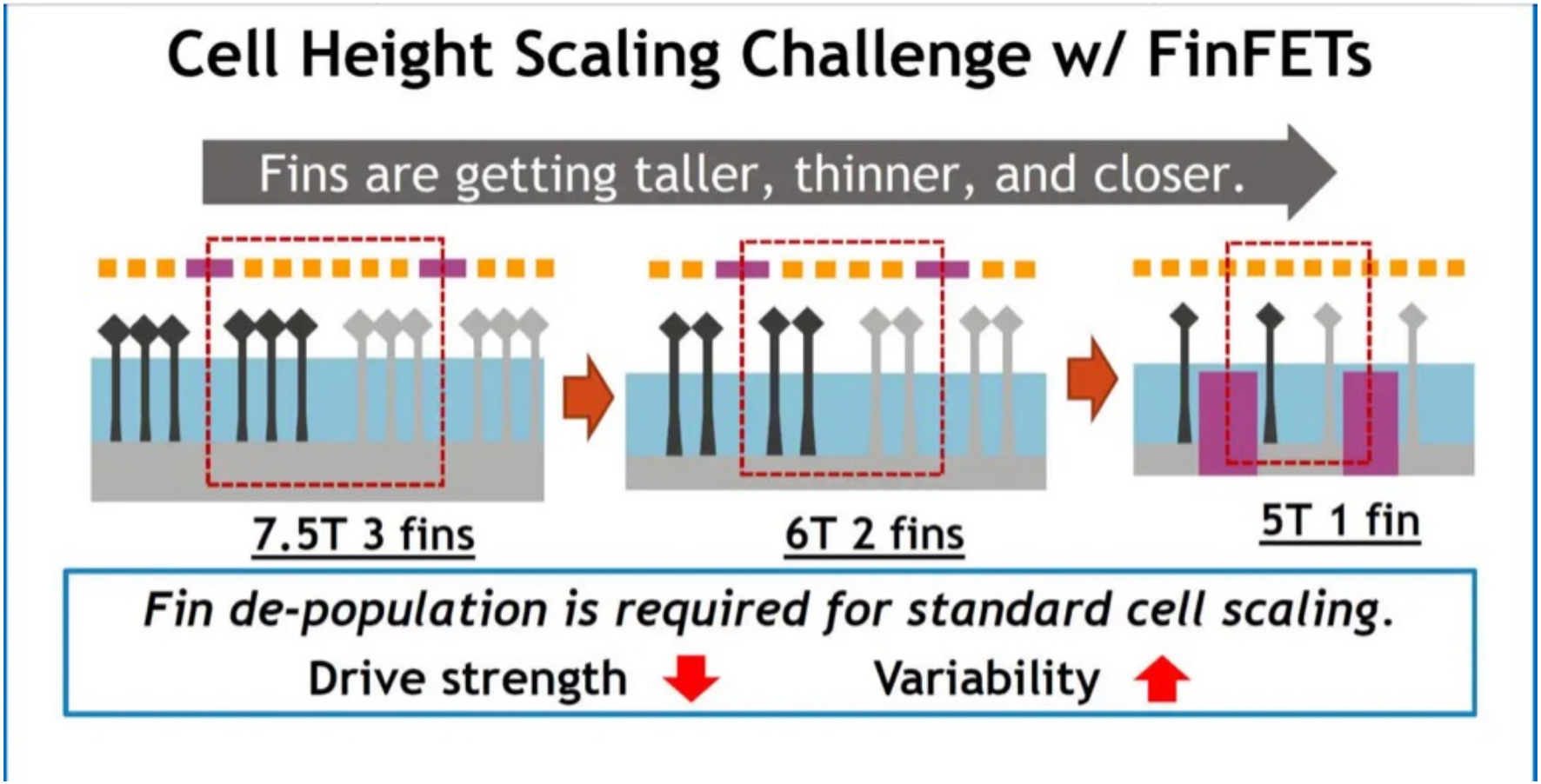

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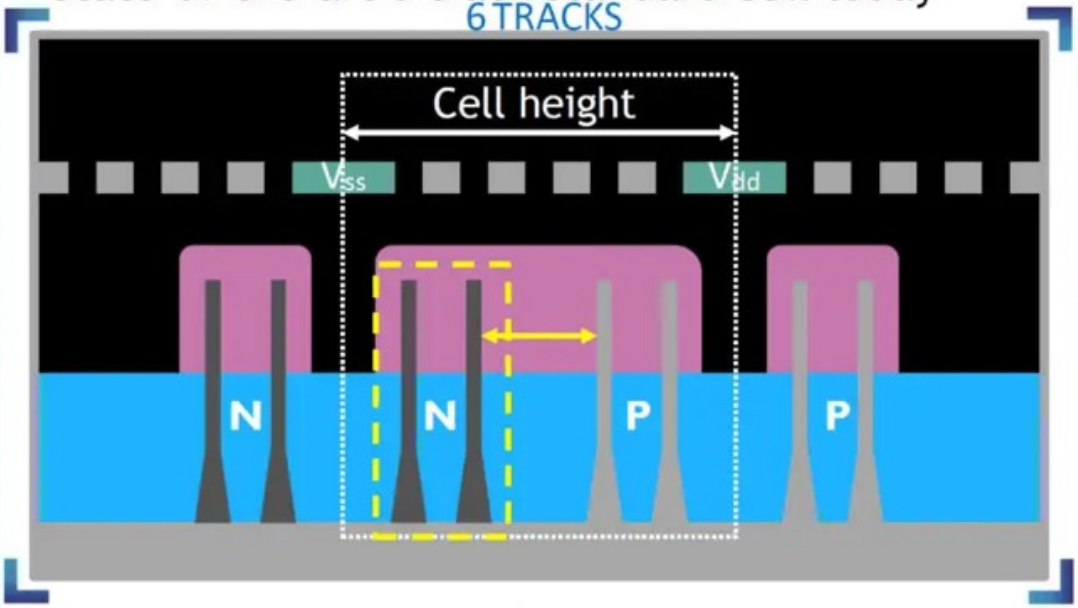
Standard cell scaling options

- State-of-the-art 6 track standard cell today



CMOS scaling trend
- Slow pitch scaling
- Cell height scaling driven:
  6T → 5T → 4T → .....

Cell height scaling enablers
- Single fin device
- NP space scaling

New device architecture is necessary for single fin and N-P space scaling

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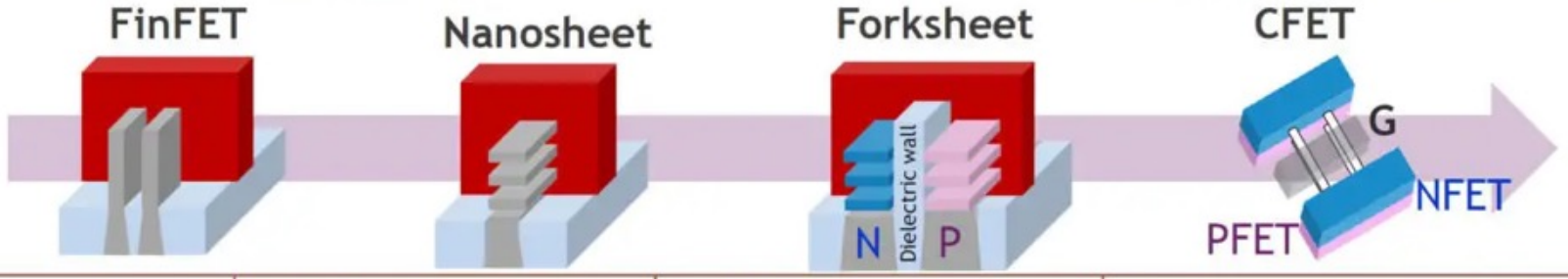
Nanosheet architectures for continuous CMOS scaling

Single Device → *CMOS device architecture*



	Nanosheet	Forksheet	CFET
Wider effective width in single fin	• Stacked nanosheet ch.	• Stacked nanosheet ch. • Small N-P → Wider NS	• Stacked nanosheet ch. • Stacked N&P → Wider NS
N-P space scaling		• Dielectric wall	• Stacked N&P

Nanosheet architectures enable wider effective width and small N-P space

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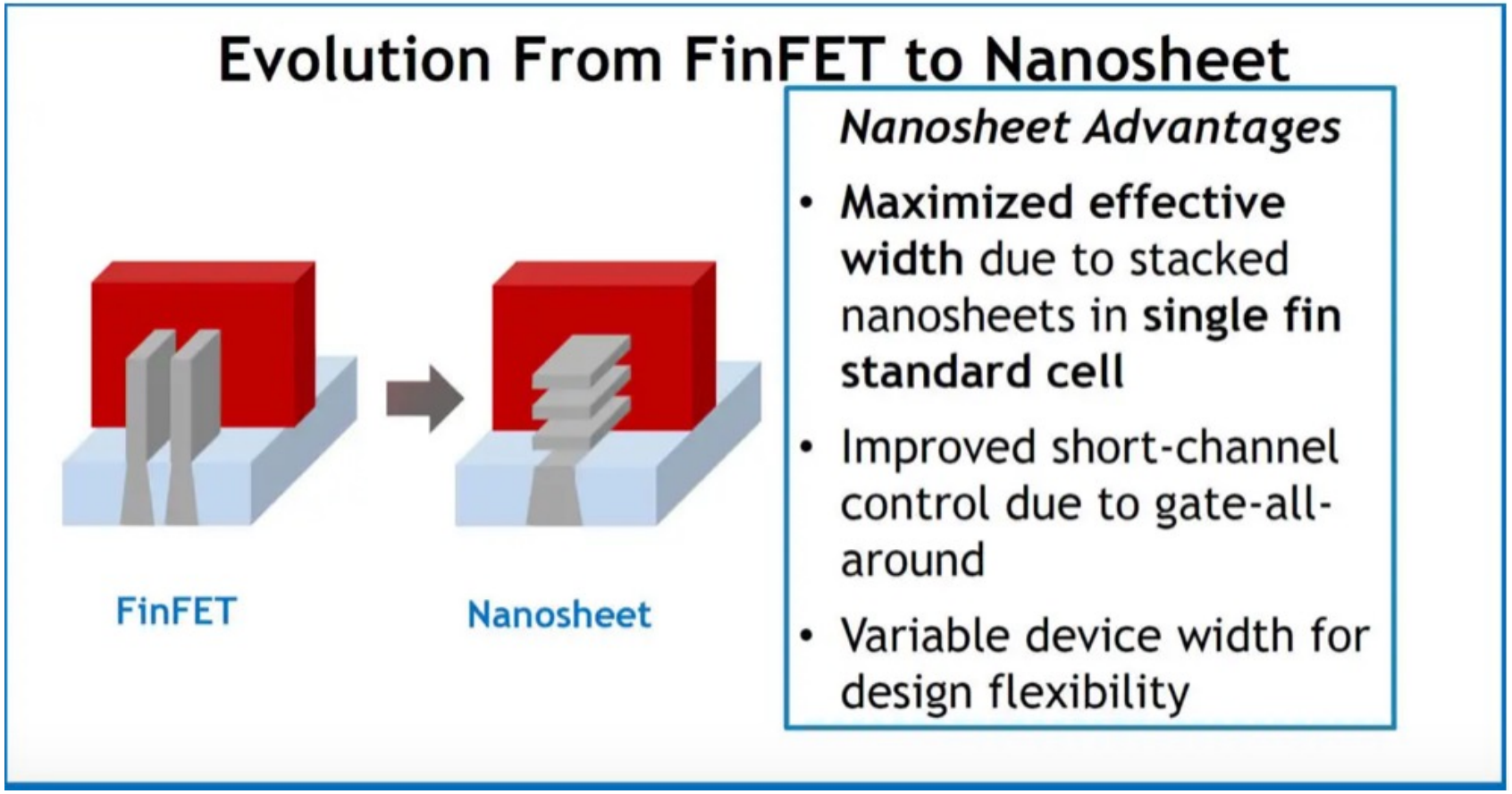

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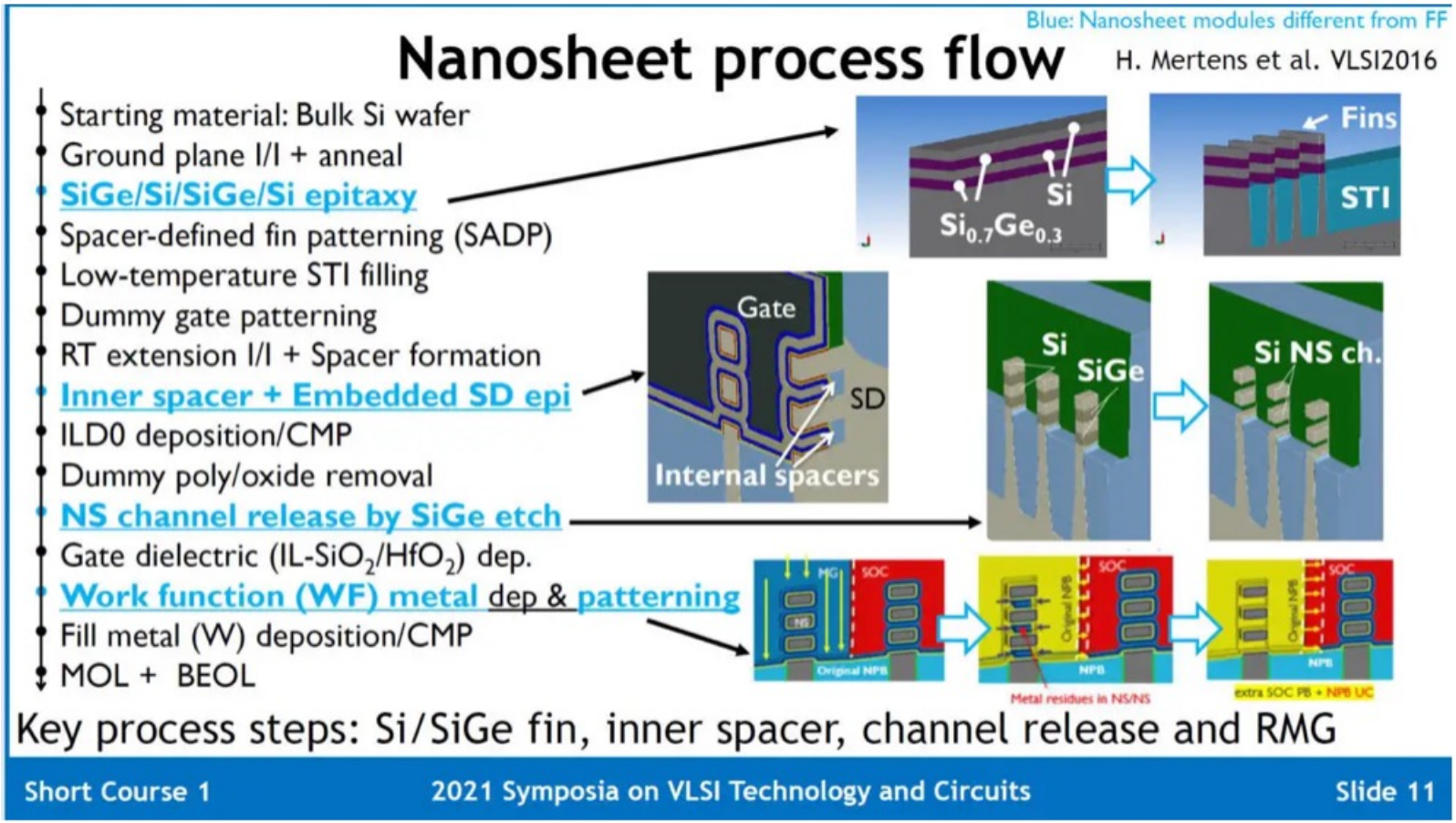

Figure 10. HNS Process Flow.

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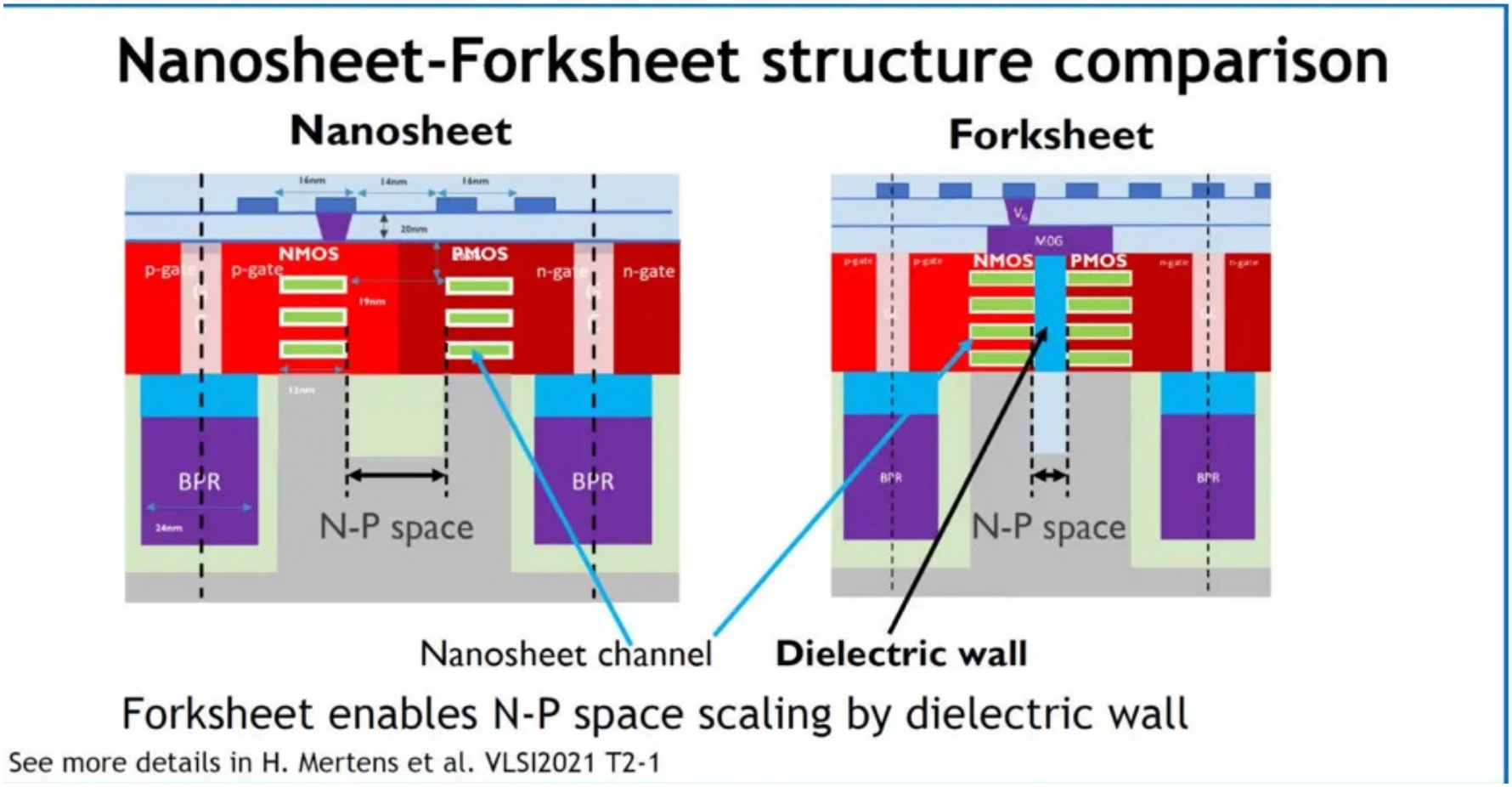

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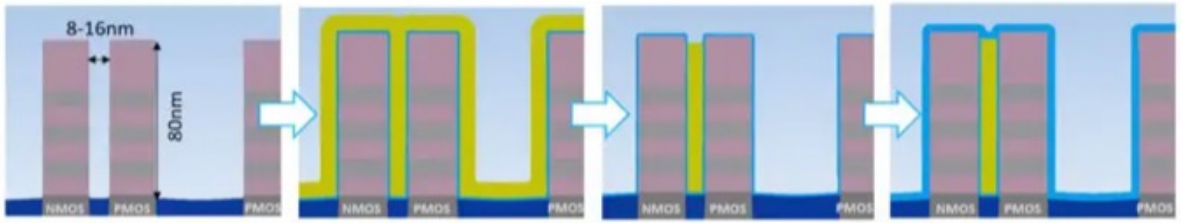
by Scotten Jones on 07-02-2021 at 6:00 am
Categories: Events, IC Knowledge, Semiconductor Services, TSMC

Forksheet process flow

Light Blue: New modules in FS
Blue: Modified modules from NS

- Nanosheet STI
- **Dielectric wall formation**
- Gate patterning
- Spacer and fin recess
- **Inner spacer**
- **Source/drain epitaxy**
- ILD0 CMP
- Dummy poly/oxide removal
- NS channel release by SiGe etch
- **RMG**
- MOL + BEOL



See more details in H. Mertens et al. VLSI2021 T2-1

Forksheet flow is similar as nanosheet flow. Dielectric wall formation and modified inner spacer/SD epi/RMG are key process steps.

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by Scotten Jones on 07-02-2021 at 6:00 am

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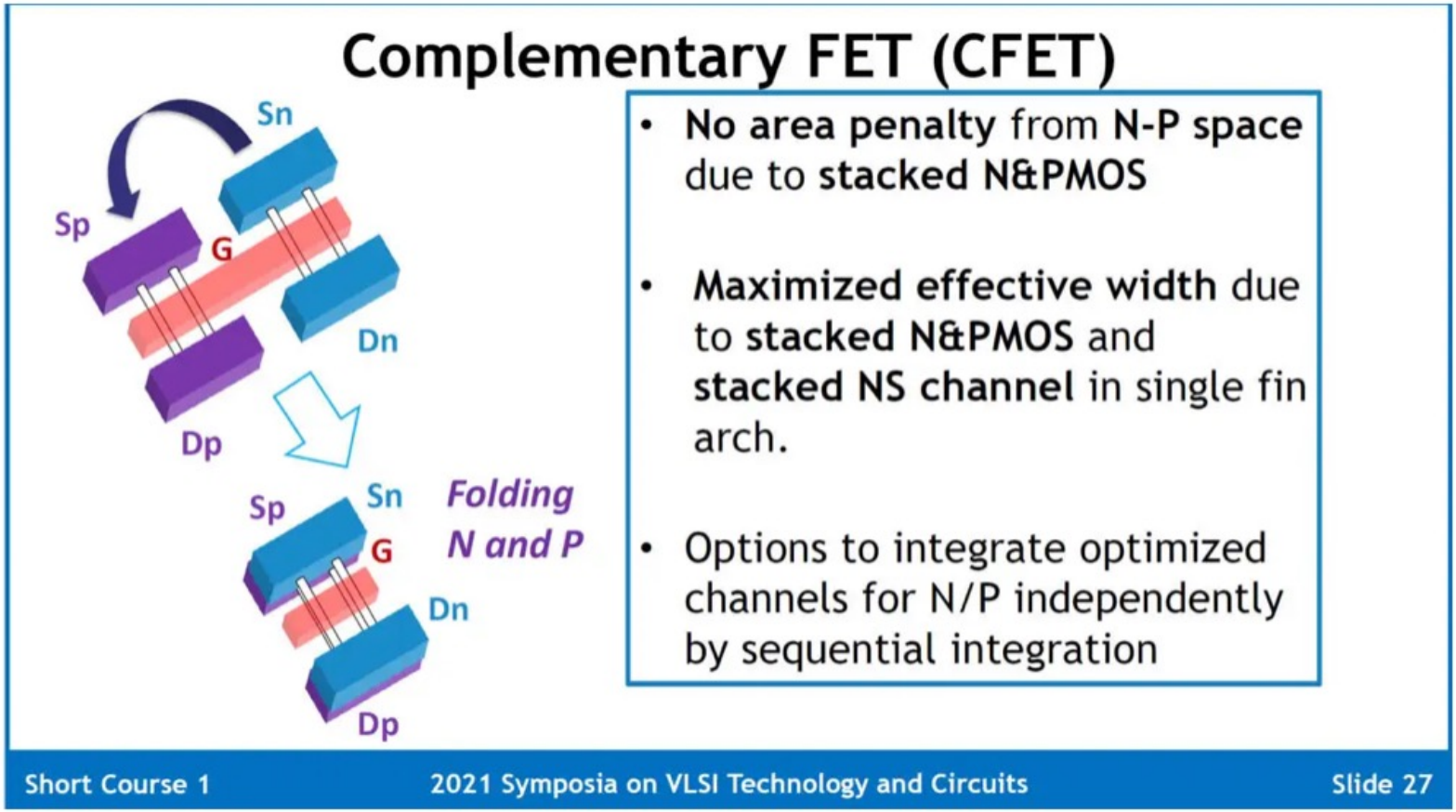

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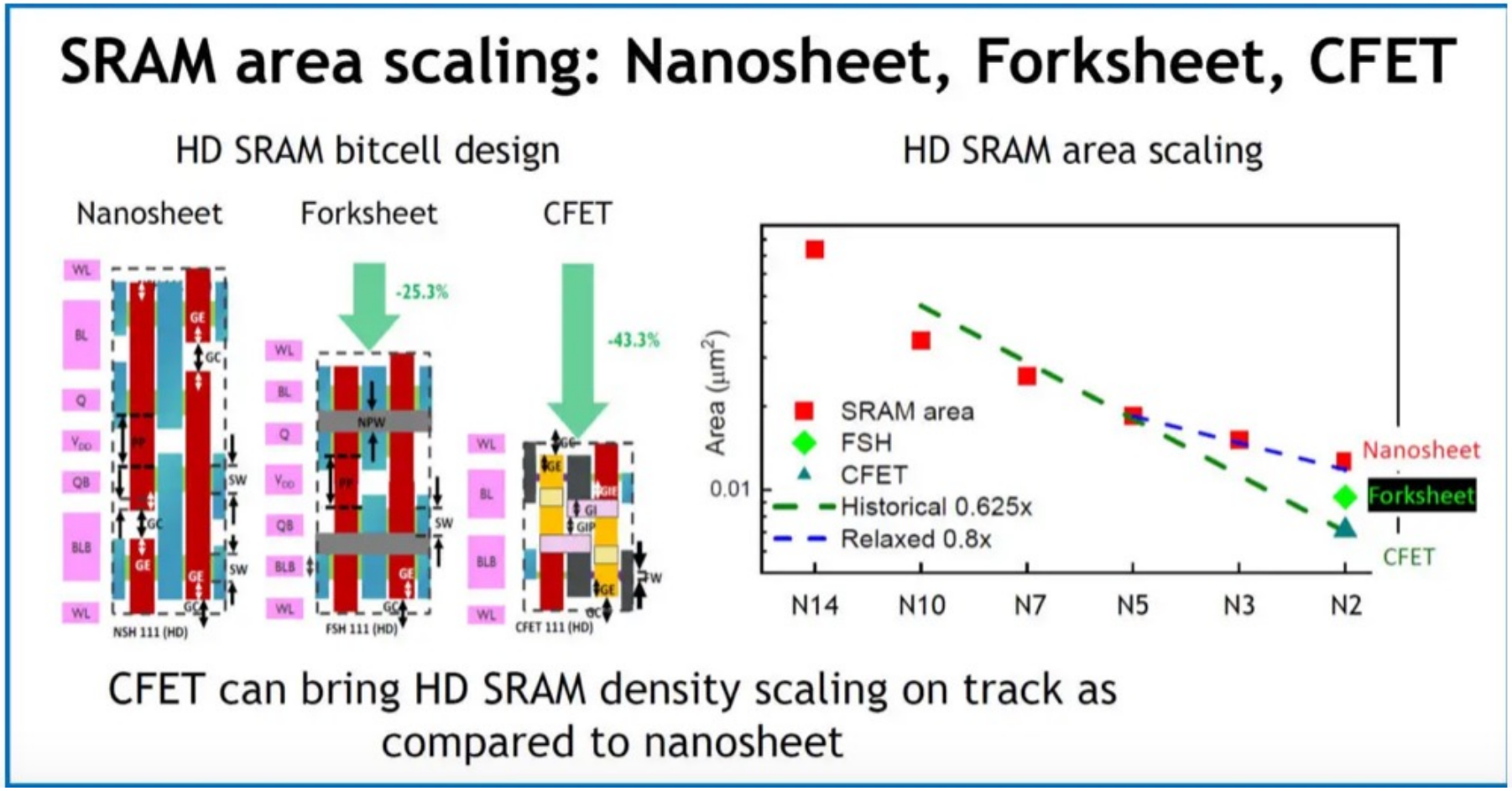

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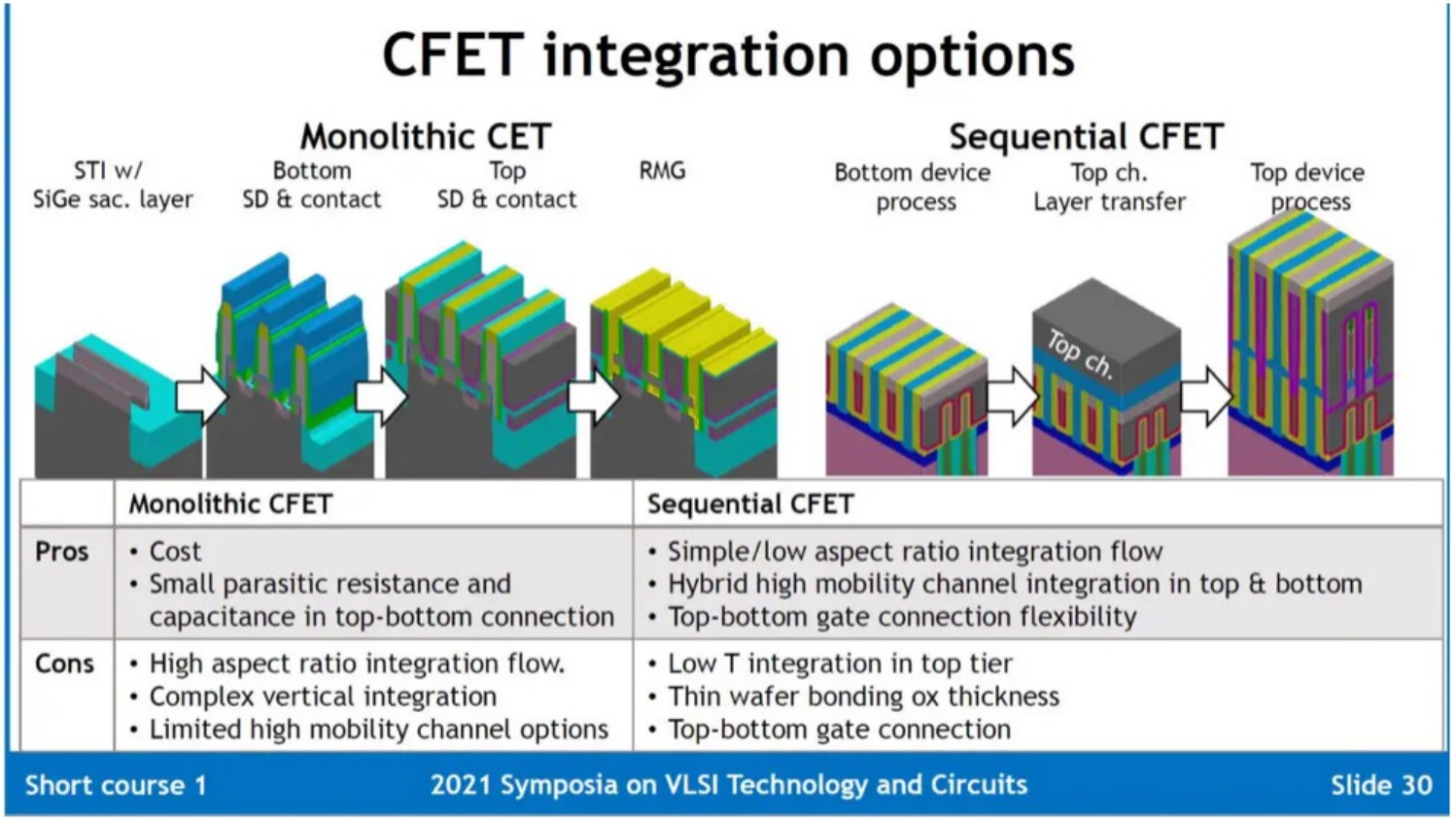

Figure 15. CFET Fabrication Options.

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TSMC at VLSI Conf 2022

TSMC at VLSI Conf ‘22

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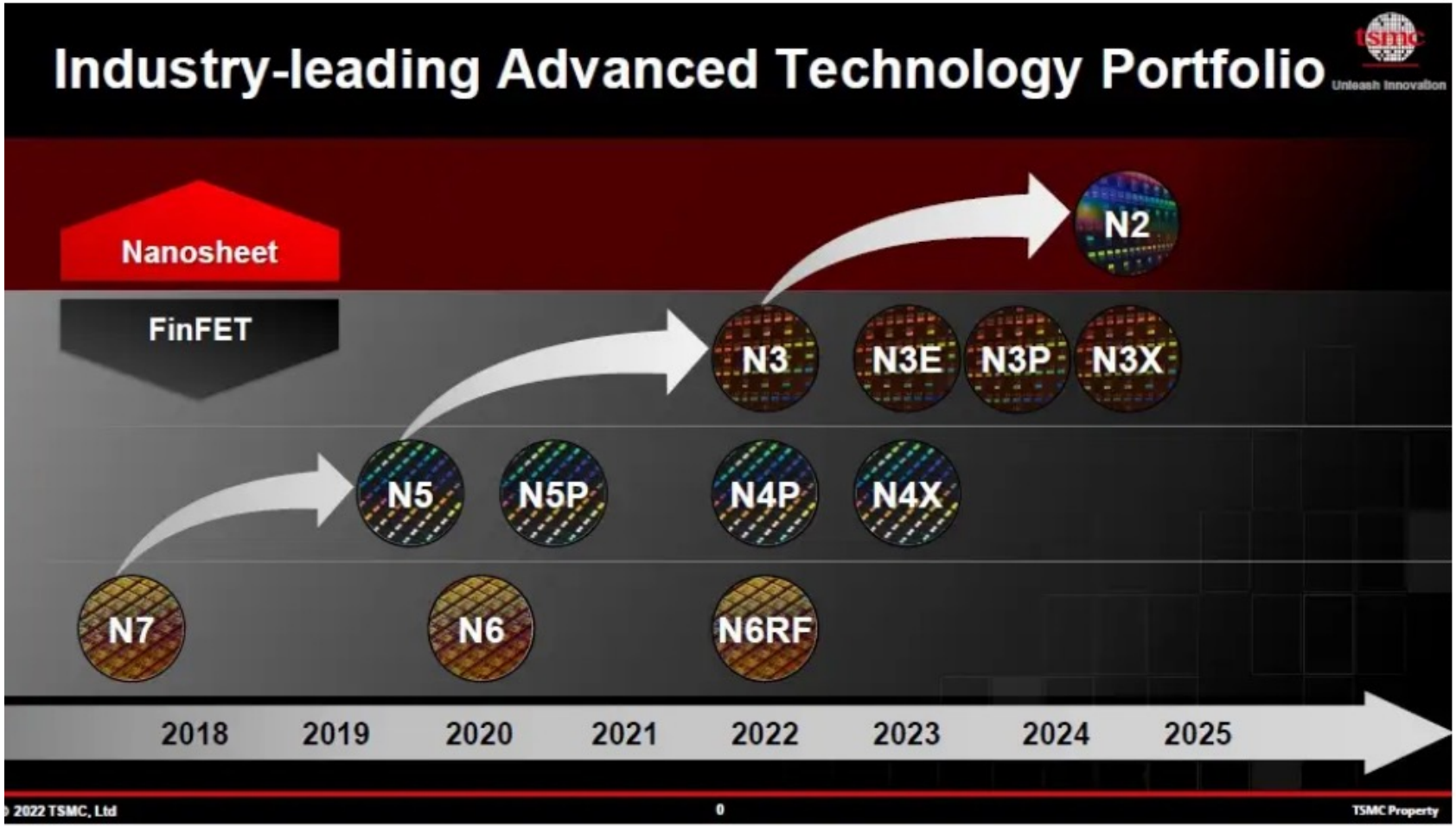

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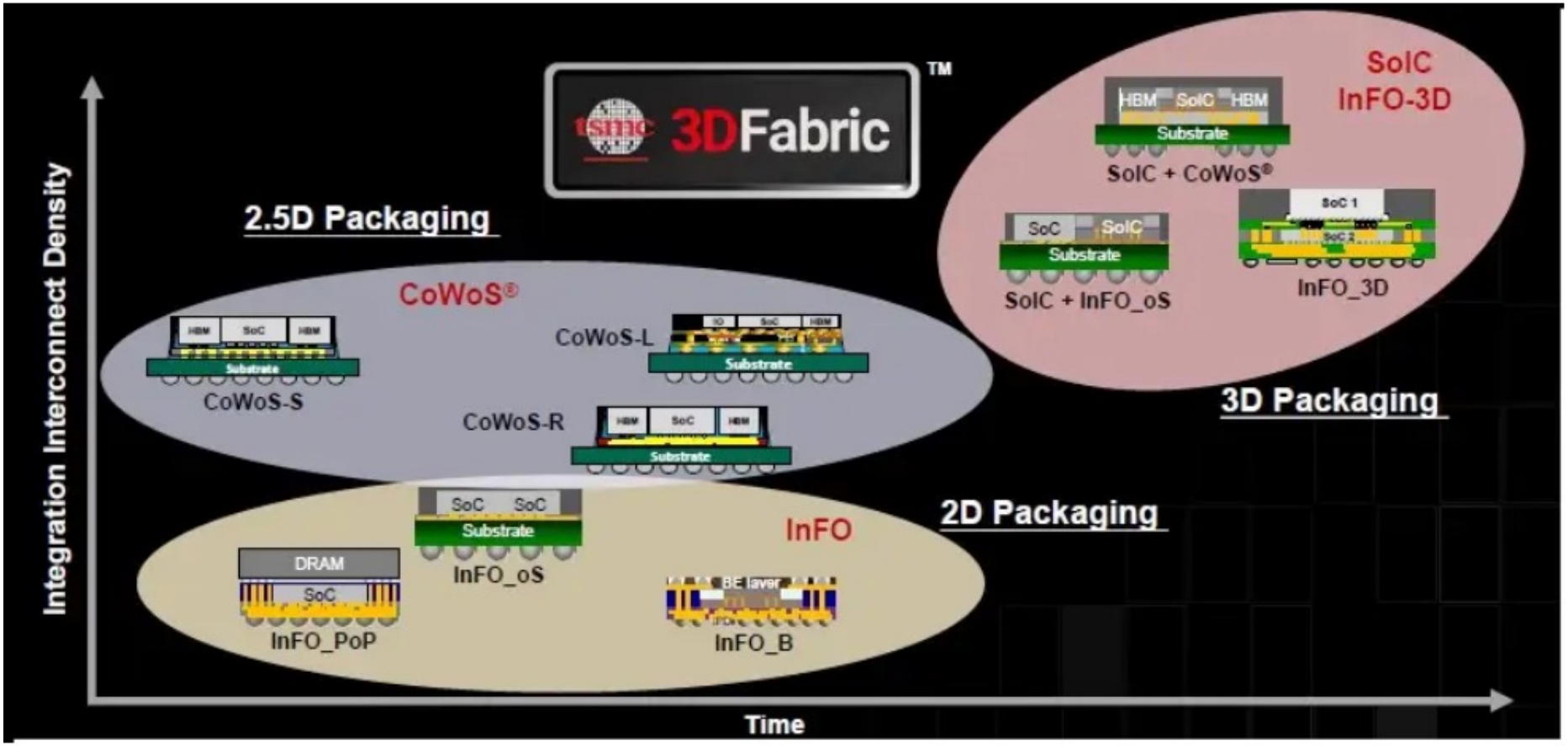

TSMC has merged their 2.5D and 3D packaging offerings into a single brand – “3D Fabric”. The expectations are that there will be future customers that pursue both options to provide dense, heterogeneous integration of system-level functionality – e.g., both “front-end” 3D vertical assembly, combined with “back-end” 2.5D integration.

TSMC at VLSI Conf '22

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Jeff Drobman

N5/N4

- in the 3rd year of production, with over 2M wafers shipped, 150 NTOs by year-end 2022
- mobile customers were the first, followed by HPC products
- roadmap includes ongoing N4 process enhancements
- N4P foundation IP is ready, interface IP available in 3Q2022 (to the v1.0 PDK)
- there is an N5HPC variant (not shown in the figure above, ~8% perf improvement, HVM in 2H22)

Node (compared to N5)	N5	N5P	N4P	N4X
Performance	1X	1.05X	1.11X	1.15X
Density	1X	1X	1.06X	1.06X

TSMC at VLSI Conf ‘22

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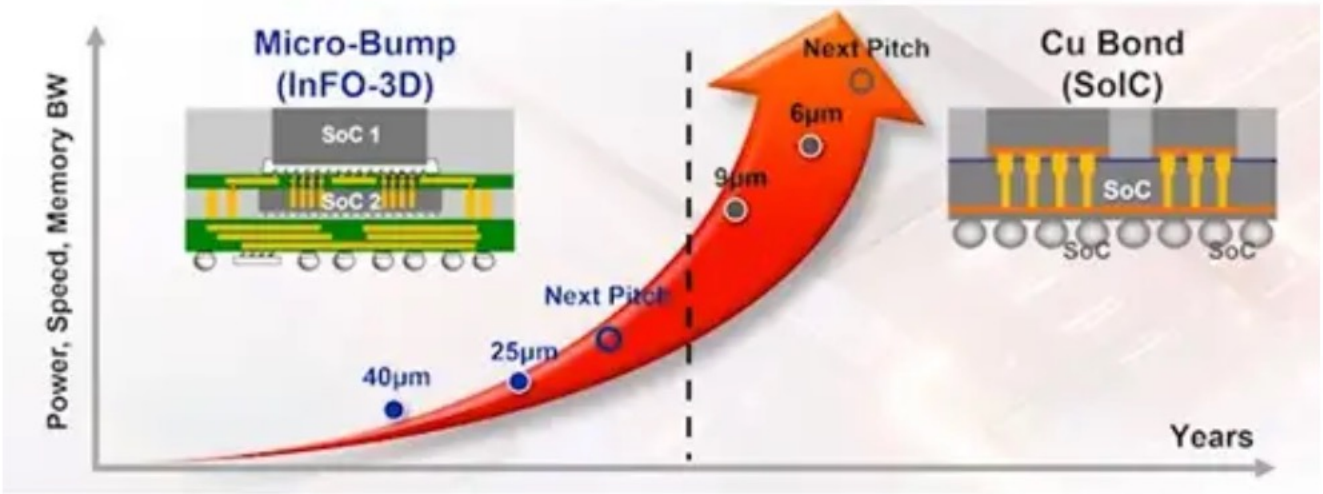
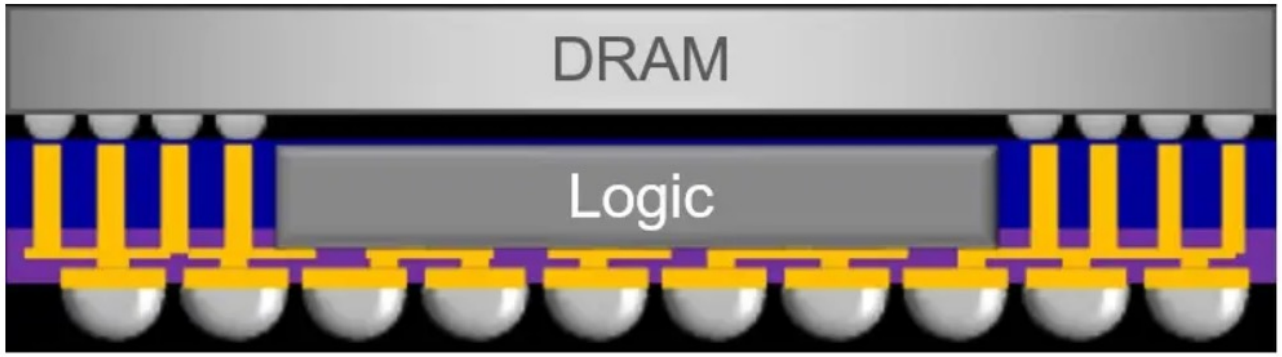
3D packaging



As shown below, InFO_PoP denotes a package-on-package configuration, and is focused on integration of a DRAM package with a base logic die. The bumps on the DRAM top die utilize through-InFO vias (TIV) to reach the redistribution layers.



Foundries

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Samsung

Founded 1938

Intel vs Samsung

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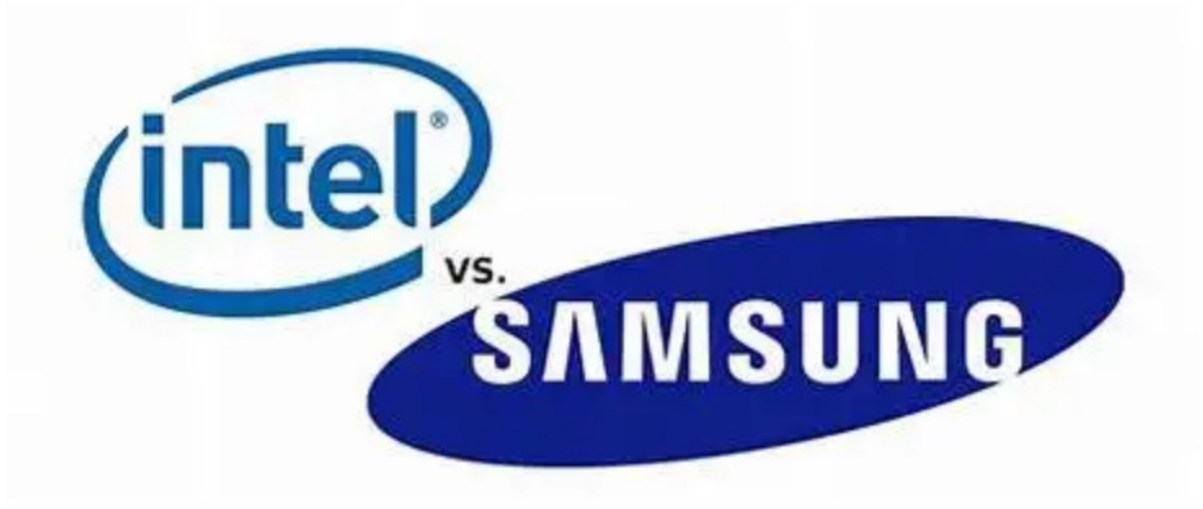
FOUNDRIES

How Intel will Beat Samsung

by Daniel Nenni on 03-09-2022 at 6:00 am
Categories: Foundries
7 Comments



Now that Intel is back in the foundry business, and with the Tower Semiconductor acquisition they are definitely back in the foundry business, Samsung will be the biggest foundry loser here.

You can break the IDM foundry business into two parts: First, and foremost, the NOT TSMC Business. Second is the the Better PPA (Power/Performance, Area) Business.

Samsung 12” Wafers

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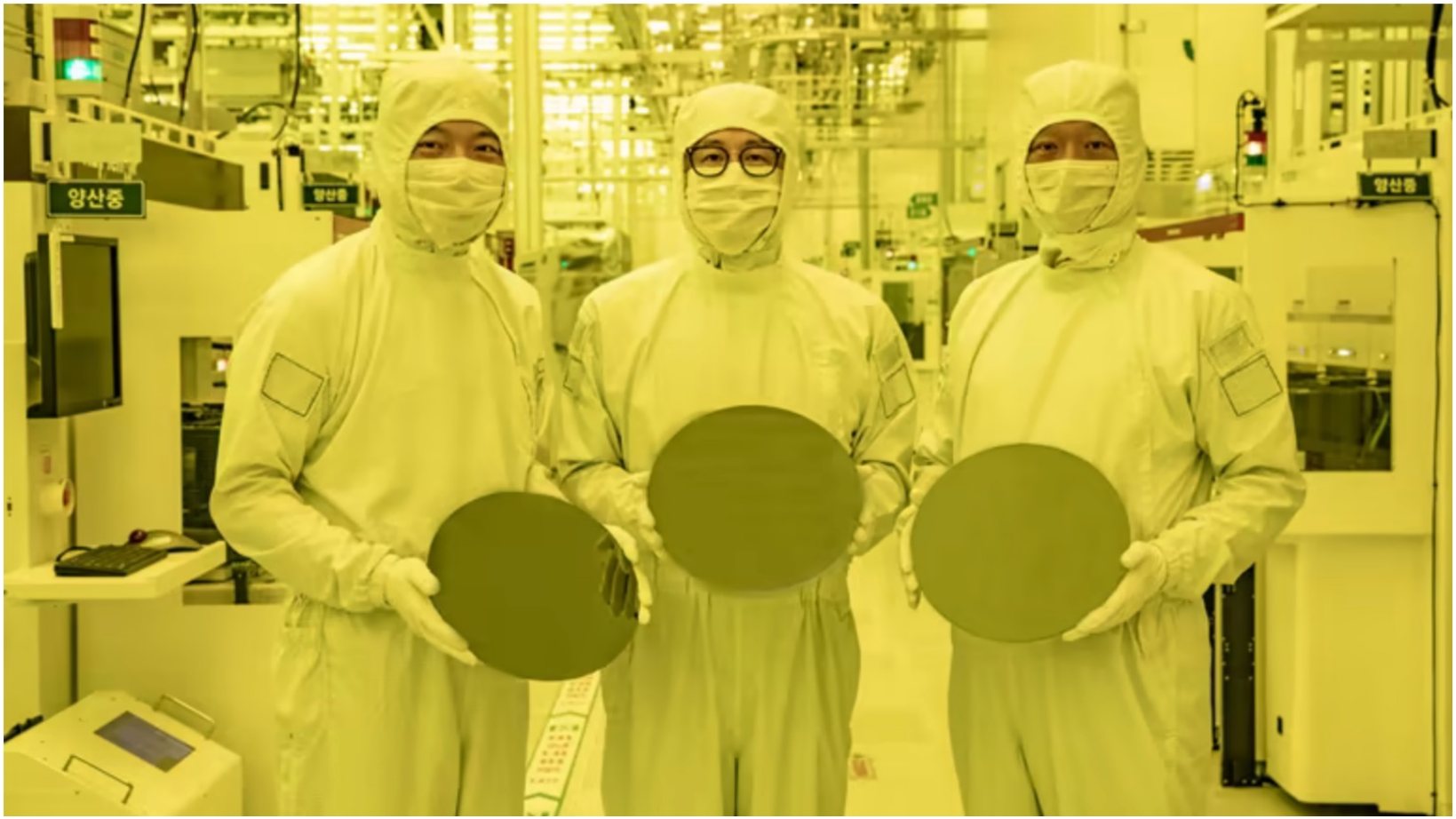

Chip Fabs

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Samsung in Texas

THE VERGE

Samsung is building a new $17 billion advanced chip plant in Texas

Creating 1,800 jobs in the city of Taylor

By Mitchell Clark and Jon Porter | Updated Nov 23, 2021, 6:15pm EST

Samsung Austin Semiconductor — The new plant will be even larger than this | Image: Samsung

Chip Fabs

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THE VERGE

Samsung in Texas

Kinam Kim, the vice chairman and CEO of Samsung Electronics Device Solutions Division says in a statement that "With greater manufacturing capacity, we will be able to better serve the needs of our customers and contribute to the stability of the global semiconductor supply chain." He continued, "In addition to our partners in Texas, we are grateful to the Biden Administration for creating an environment that supports companies like Samsung as we work to expand leading-edge semiconductor manufacturing in the U.S. We also thank the administration and Congress for their bipartisan support to swiftly enact federal incentives for domestic chip production and innovation."

In response, the Biden administration is attempting to bolster US chip production, reducing the potential for supply chain disruption and reversing the country's declining share of manufacturing in recent decades. The Senate recently approved $52 billion in subsidies for new chipmaking plants, though the CHIPS Act is yet to pass in the House of Representatives, according to *Bloomberg*.

Samsung 3nm

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July 2021

Samsung 3nm GAA HVM in 2024?

Samsung Foundry 3nm Gate All Around Process Node, 3GAE, Delayed to 2024

Samsung Foundry 3nm Gate All Around Process Node, 3GAE, Delayed to 2024! This would arrive in a similar time frame to TSMC's denser 2nm GAA technology.Samsung and Intel continue to slip further behind TSMC in leading edge technology. Will they ever be able to catch up?

Samsung Processes

Jeff Drobman

Logic

IC Knowledge

Samsung Keynote at IEDM
by Scotten Jones on 01-27-2022 at 6:00 am

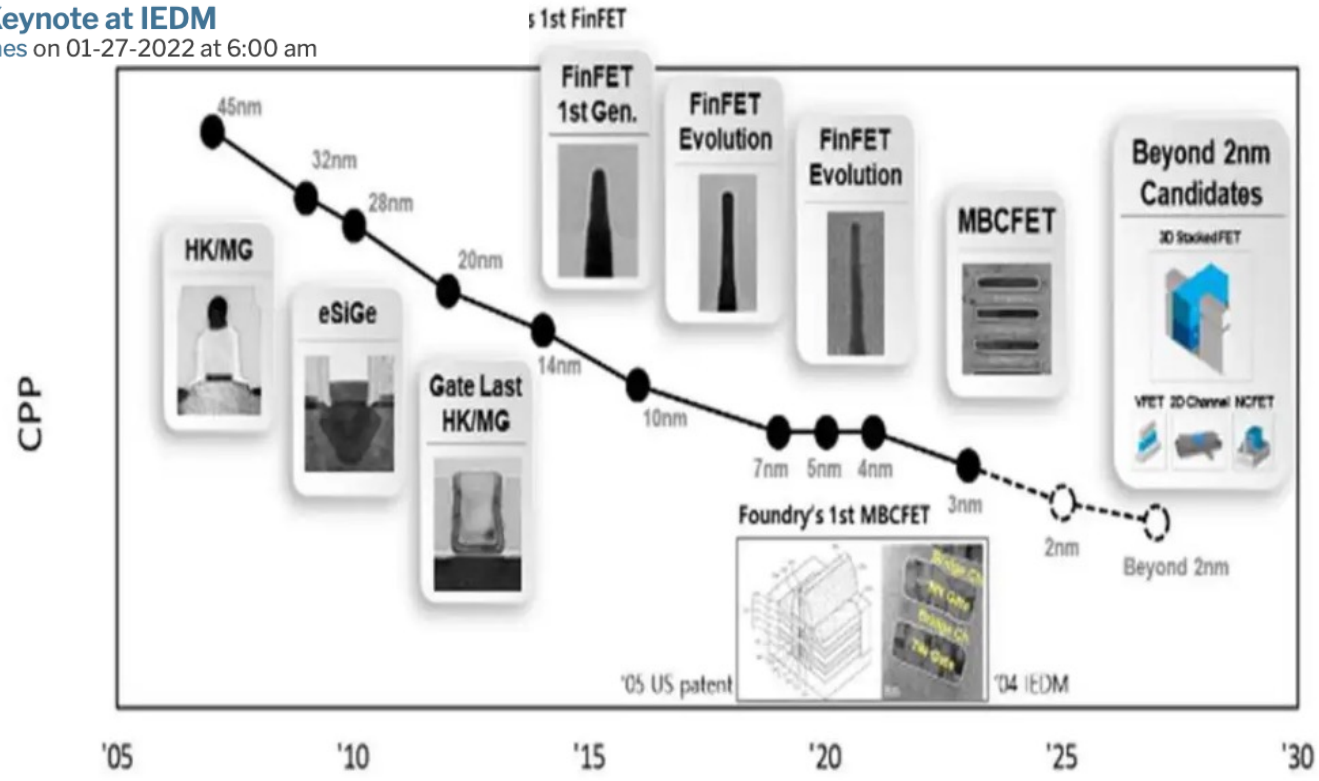

Figure 1. Logic Roadmap.

n figure 1 we can see how the contacted poly pitch (CPP) of logic processes has caled over time. In the planar era we saw high-k metal gate (HKMG) introduced by ntel at 45nm and by the foundries at 28nm as well as innovations like embedded

Samsung DRAM Processes

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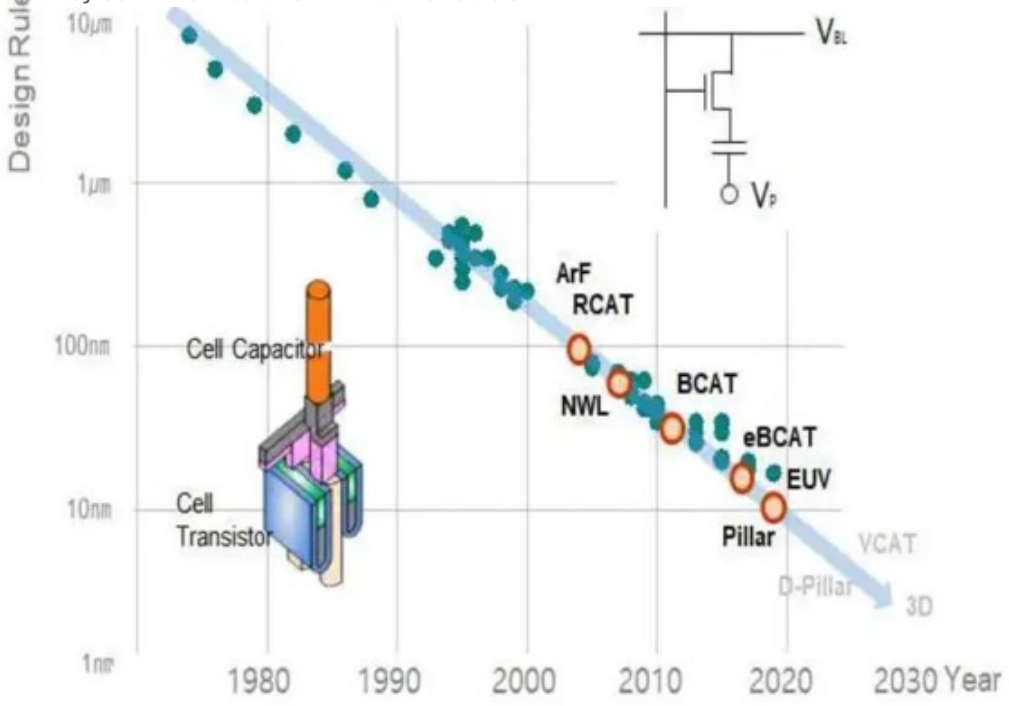
IC Knowledge — DRAM

Samsung Keynote at IEDM

by Scotten Jones on 01-27-2022 at 6:00 am



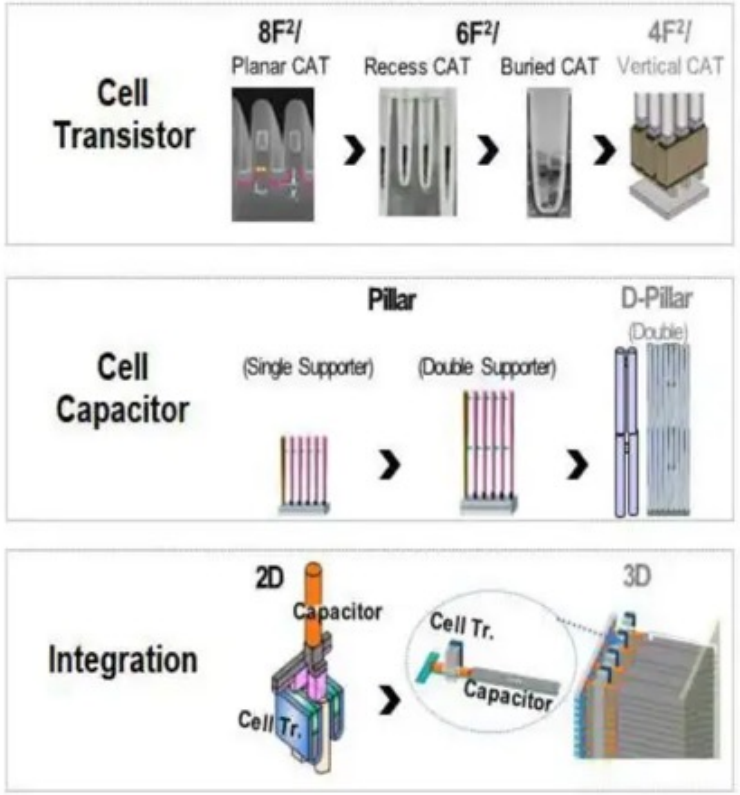


Figure 2 DRAM Roadmap

With EUV already ramping up in DRAM, the next challenges are shrinking the memory cell. Samsung is anticipating staking two layers of capacitors soon. A switch

Samsung NAND Processes

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IC Knowledge

NAND (Flash)

· NAND.

Samsung Keynote at IEDM

by Scotten Jones on 01-27-2022 at 6:00 am

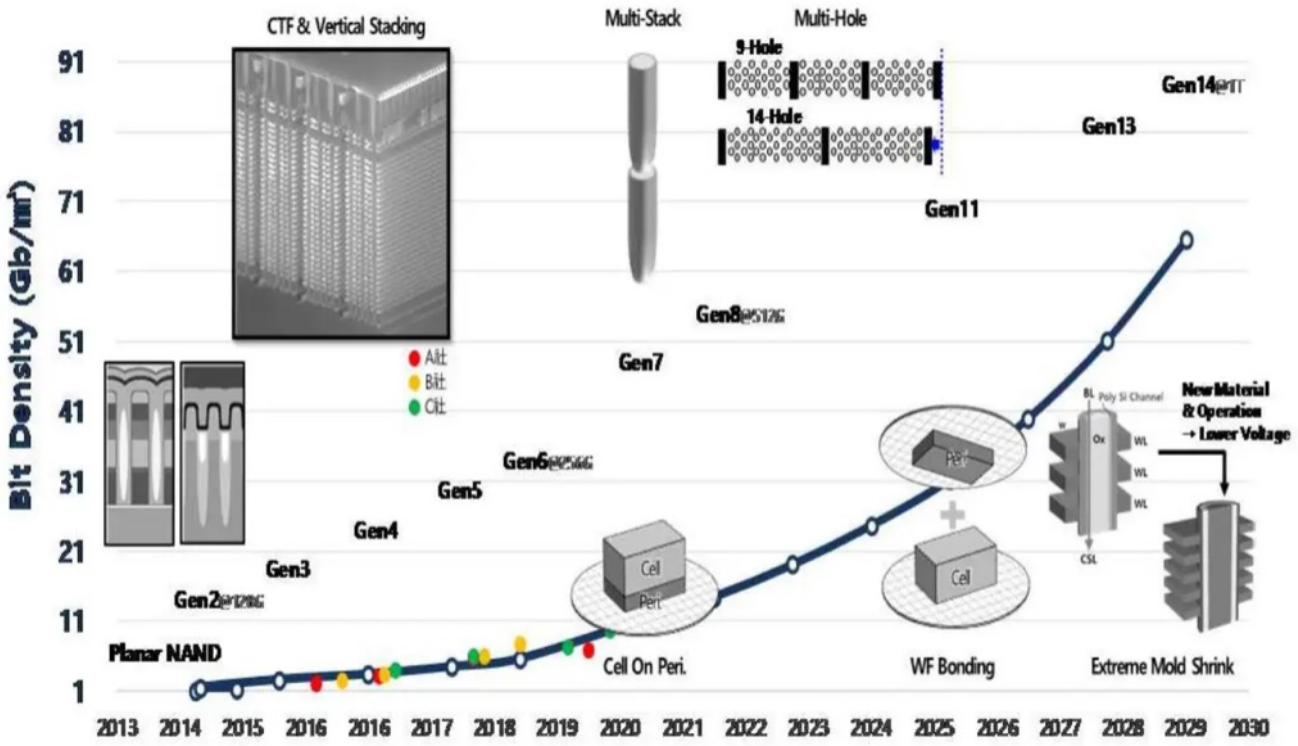

Figure 3 NAND Roadmap

Samsung's latest 3D NAND is a 176-layer process that uses string stacking for the first time (first time string stacking for them, others have been string stacking for multiple generations) and peripheral under the array for the first time (once again the

SemiWiki.com

Via Apple

Fabless: The Transformation of the Semiconductor Industry

Samsung entered the foundry business with Apple 15+ years ago. The first Apple ASIC (iPod) was actually done by fabless ASIC vendor eSilicon and the volumes were drastically underestimated so eSilicon profited greatly. In 2006 Steve Jobs went to Intel CEO Paul Otellini and pitched the iPhone in hopes of getting a manufacturing agreement. Paul did not share Steve's vision and passed on the deal:

"*We ended up not winning it or passing on it, depending on how you want to view it. And the world would have been a lot different if we'd done it. The thing you have to remember is that this was before the iPhone was introduced and no one knew what the iPhone would do. At the end of the day, there was a chip that they were interested in that they wanted to pay a certain price for and not a nickel more and that price was below our forecasted cost. I couldn't see it. It wasn't one of these things you can make up on volume. And in hindsight, the forecasted cost was wrong and the volume was 100x what anyone thought.*"

As a result, not only did Intel miss the mobile market, they missed the opportunity of being a world class foundry like TSMC is today.

SemiWiki.com

Via Apple

Apple then went to Samsung which produced the first A4 SoC for the iPhone 4 using the Samsung 45nm process. The A5 SoC was also 45nm. Back then we named processes different so it was not unusual to reuse a process so all was well and the iPhone dynasty had begun. The A6 was Samsung 32nm and the A7 was Samsung 28nm.

Unfortunately, Samsung showed their true IDM colors by competing directly with Apple and even borrowed some Apple IP. The result was Apple filing more than 50 legal actions around the world which would ultimately be settled for billions of dollars in Apple's favor.

For the A8 (iPhone 6) Apple turned to TSMC 20nm. The iPhone 6 was one of the better smartphones (I had one). Unfortunately, when Apple turned to FinFETs TSMC could not supply enough chips so they also used Samsung 14nm for the A9. Apple was back to TSMC for the A9x and there on after.

SemiWiki.com

Via Apple

Apple absolutely did change the foundry business by writing some really big checks, accounting for 20+% of TSMCs annual revenue, but also for the yearly process cadence. Rather than taking big risky steps TSMC did yearly half nodes matched with the yearly fall iProducts launch. This allowed them to perfect double patterning before adding FinFETs, introduce partial EUV before going to full EUV, and many other process innovations. It's called yield learning for a reason.

Now Samsung and Intel both follow the half node process methodology and you can thank Apple for that, absolutely.

Which brings us back to the recent Samsung missteps. Samsung did VERY well at 14nm getting a piece of the Apple business and many other customers including Qualcomm. Globalfoundries also licensed Samsung 14nm for their Malta fab and has done quite well with it so Samsung 14nm customers are far reaching. Unfortunately, 10nm was not so kind to Samsung with single digit yields at launch time. Samsung was forced to ship good die instead of wafers causing Qualcomm and others to miss market windows and customer commitments.

SemiWiki.com

Via Apple

Samsung did a much better job at 7nm but now we are hearing about a serious unreported yield problem at 5nm. In fact, there is a formal investigation inside Samsung:

"The company's management suspects a forgery of the report on the release of microcircuits by the Samsung Semiconductor Foundry division. Information about the production of 5-, 4- and 3-nm products is now being verified..."

Foundries

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IBM

Founded 1911

IBM $20B

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10-6-22

New Nodes: IBM 2nm

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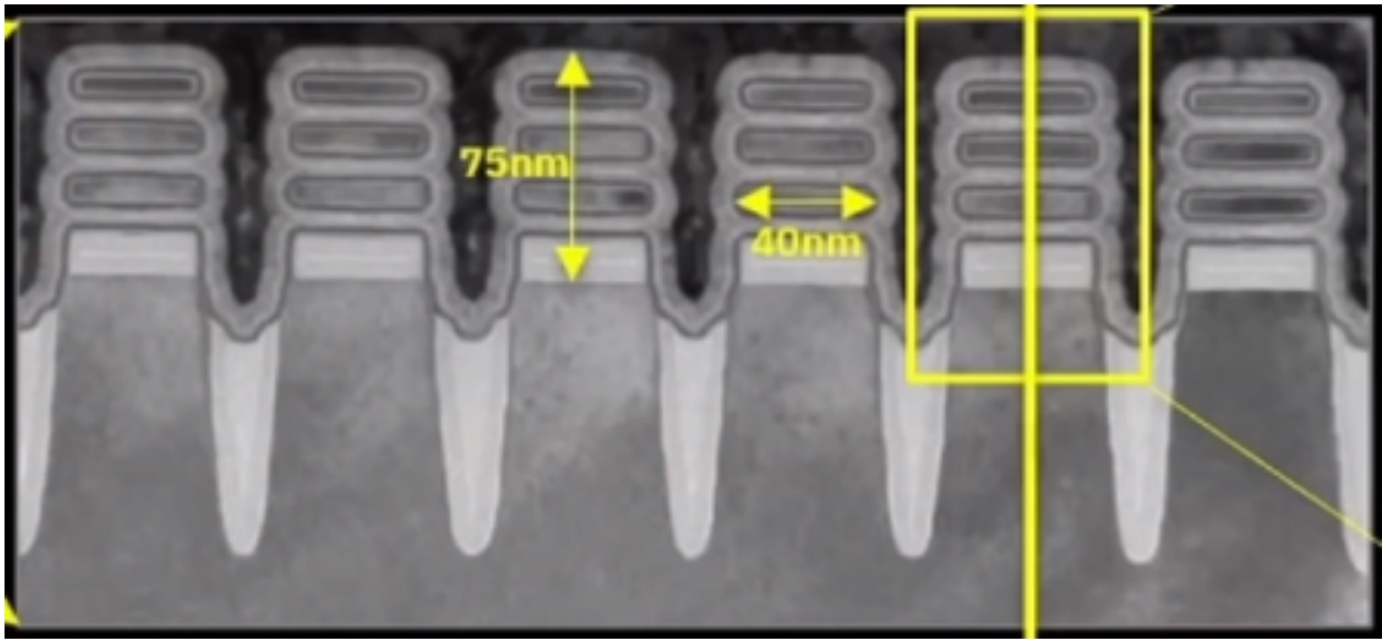

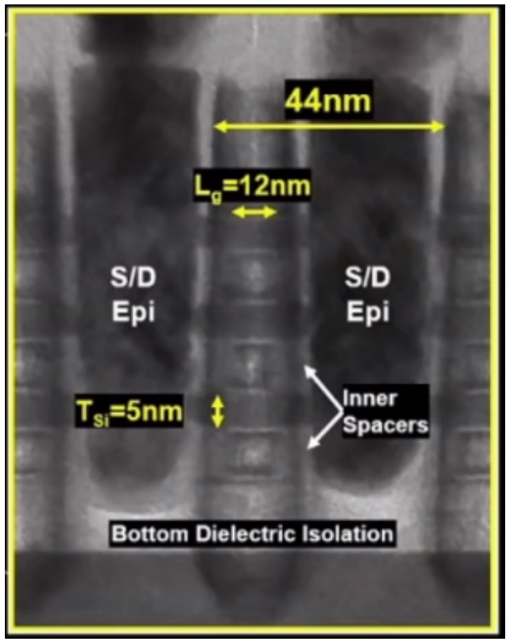

Images of IBMs 2nm Chip architecture

New Processes

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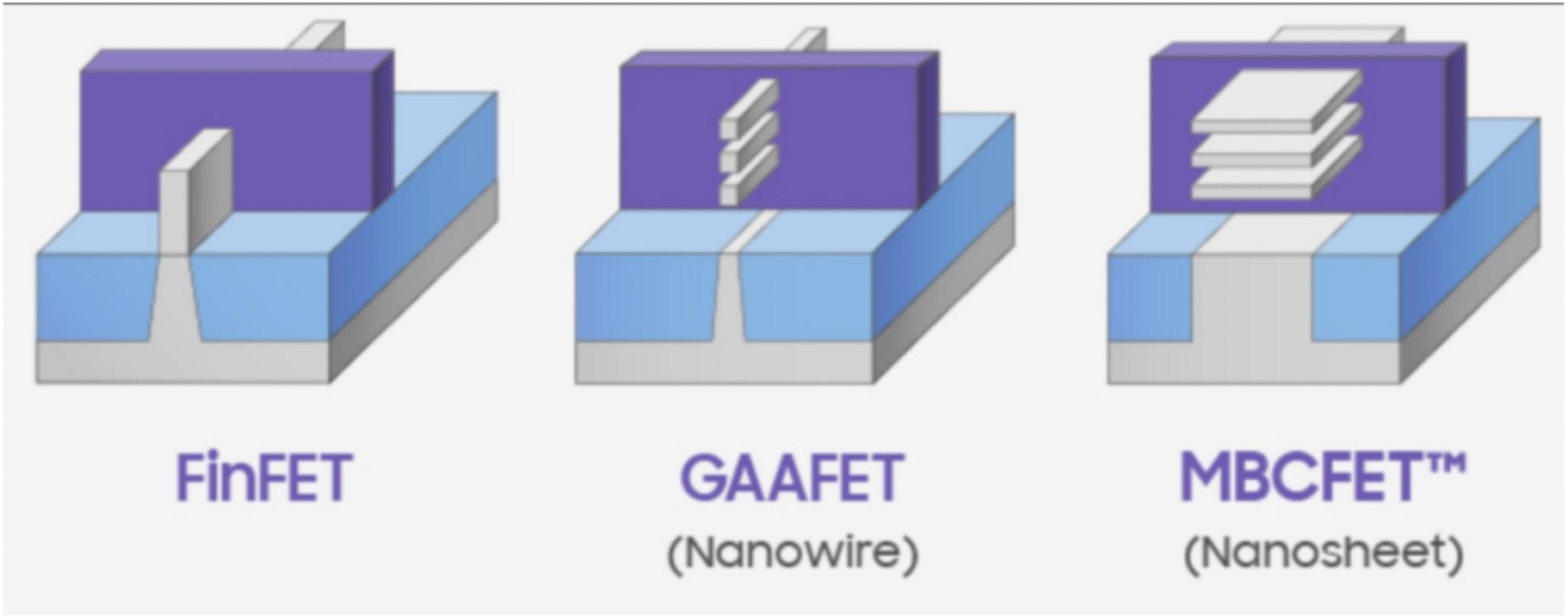

2-3-5-7 nm Comps

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Peak Quoted Transistor Densities (MTr/mm2)				
AnandTech	IBM	TSMC	Intel	Samsung
22nm			16.50	
16nm/14nm		28.88	44.67	33.32
10nm		52.51	100.76	51.82
7nm		91.20	237.18*	95.08
5nm		171.30		
3nm		292.21*		
2nm	333.33			

Data from Wikichip, Different Fabs may have different counting methodologies
*** Estimated Logic Density**

Wikichip

Chips

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China

Process Nodes in China

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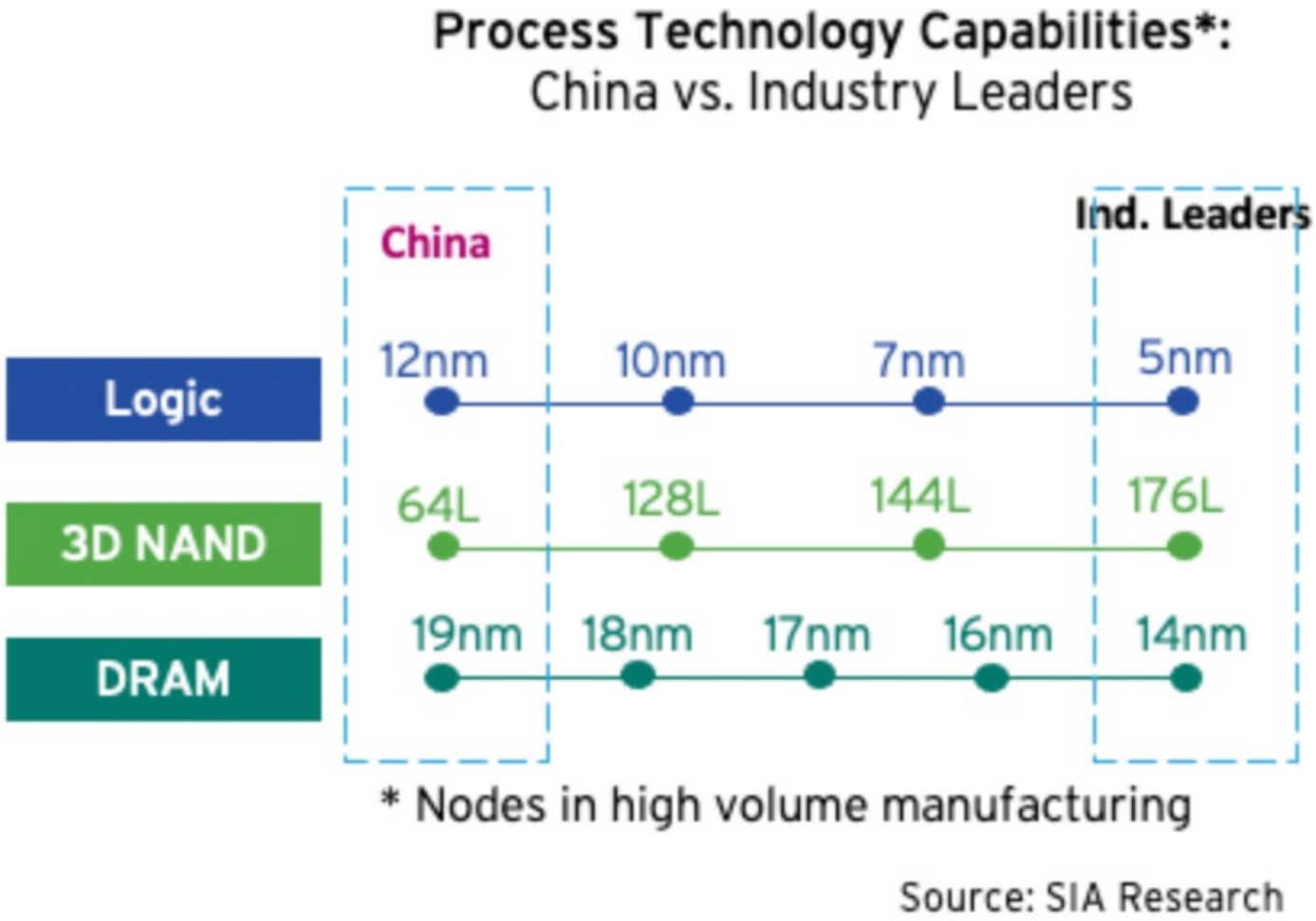
SEMICONDUCTOR INDUSTRY ASSOCIATION



China Chip Segments

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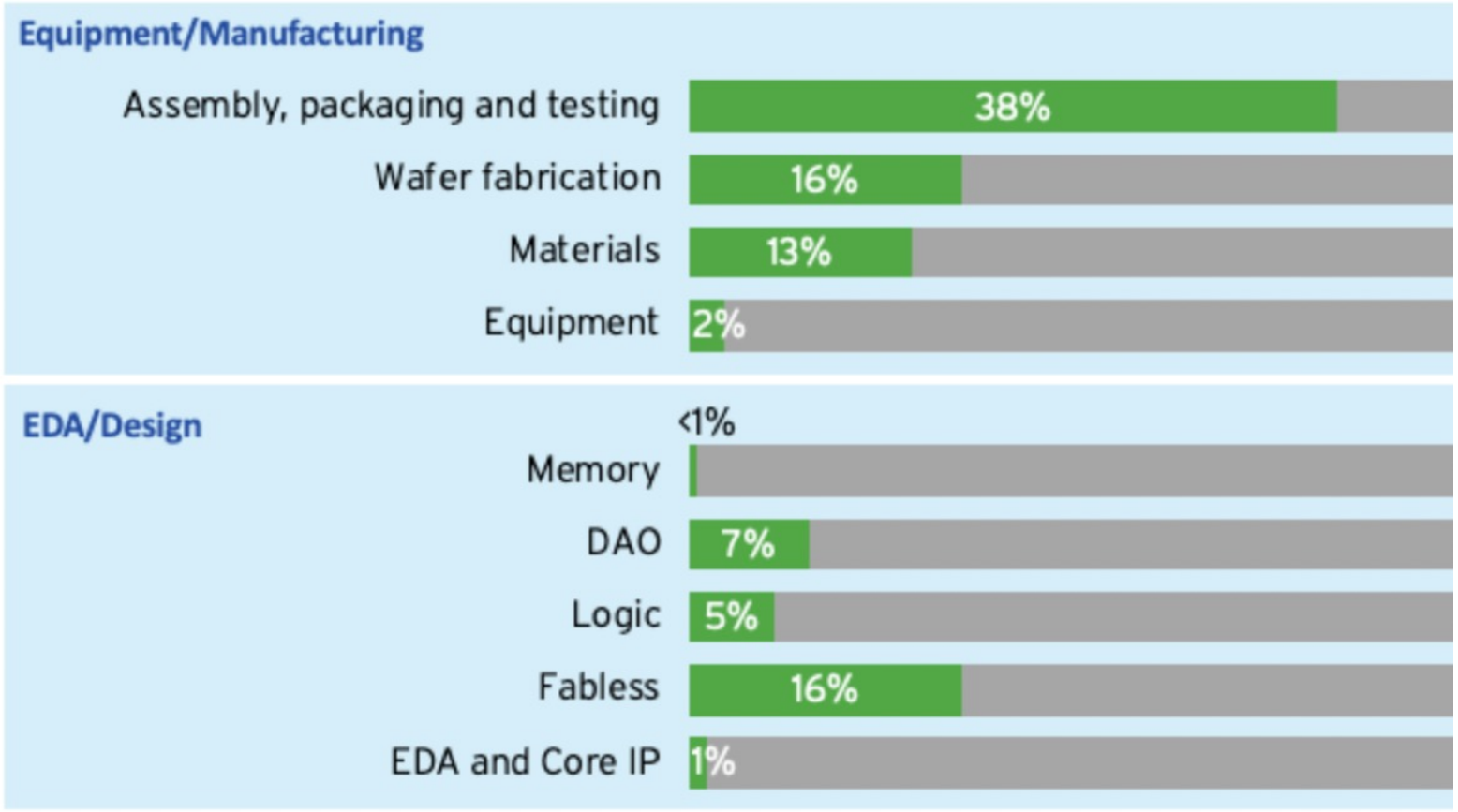
Chinese Share in the Global Semiconductor Supply Chain by Major Segment

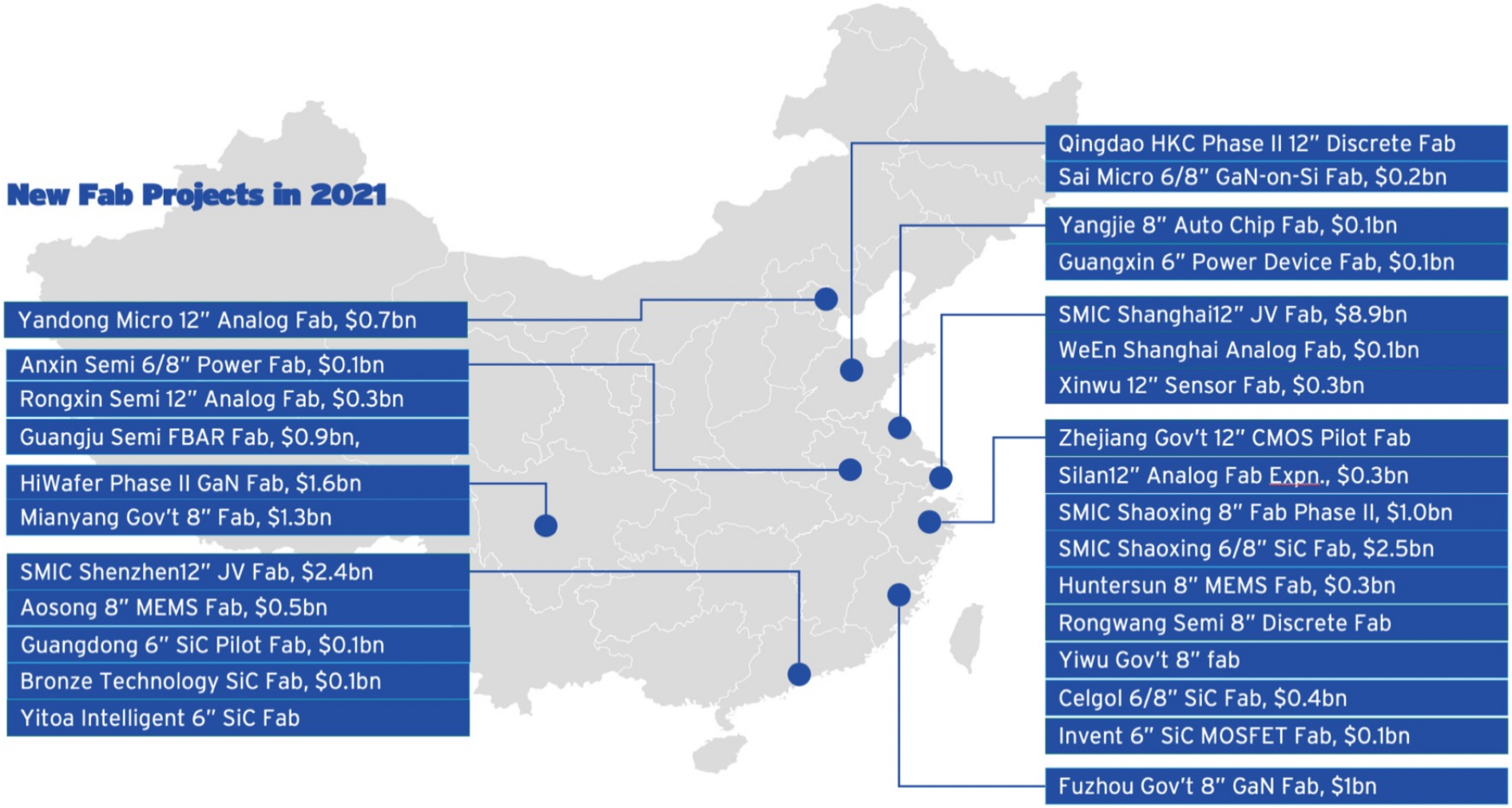


Source: BCG x SIA: Strengthening the Global Semiconductor Supply Chain in an Uncertain Era

China Map

SEMICONDUCTOR INDUSTRY ASSOCIATION

SMIC



Top China Chip Firms

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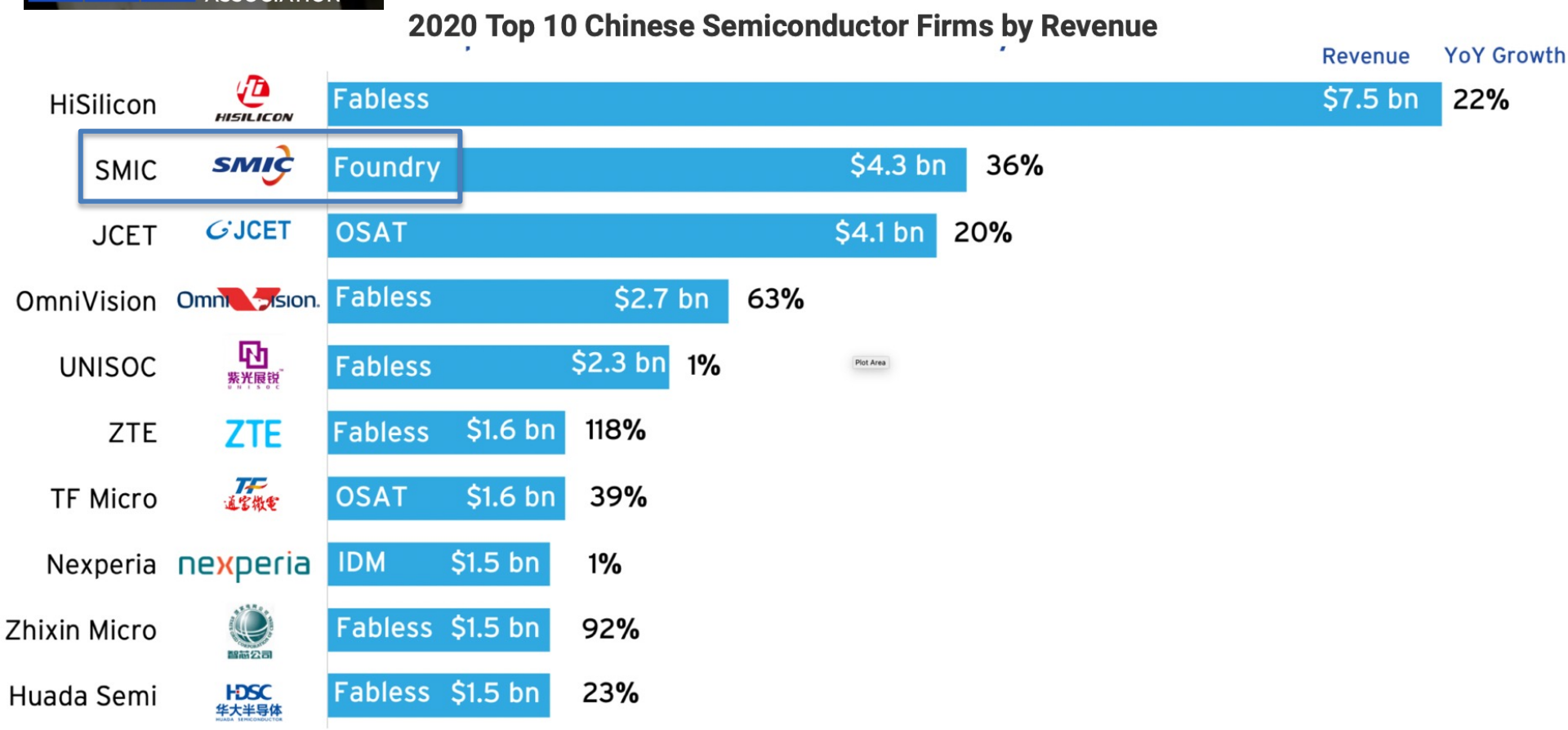

Source: SIA analysis

China OEM's

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SEMICONDUCTOR INDUSTRY ASSOCIATION

Chinese OEMs and Their Commercially Available Chip Products

OEM Vertical	Company	Semiconductor Efforts
Consumer Electronics	mi	• Jun. 2021, recruiting new chip design team • As of Aug. 2021, Xiaomi's VC fund invested in over 60 semiconductor companies
	oppo	• Feb 2020, unveiled "Mariana" chip development plan
	vivo	• Aug. 2021, invested in power semiconductor company
	huami	• Jul. 2021, launched dual-core RISC-V wearable device processor
Home Appliances	KONKA	• Feb. 2020, developed samples of GaN-based MicroLED chip • May. 2020, started memory ATP project
	Galanz	• Jan. 2021, testing RISC-V home appliance chips in foreign markets
	Midea	• Jan. 2021, incorporated semiconductor subsidiaries
	TCL	• Mar. 2021, incorporated two semiconductor subsidiaries
	CHANGHONG 长虹	• Aug. 2020, teams up with HiSilicon on 5G chip development
Internet Cloud Service	Alibaba Group 阿里巴巴集团	• May 2021, launched Xuantie 907 RISC-V processor • Oct. 2021, unveiled 5nm Yitian 710
	Baidu 百度	• Jun. 2021, incorporated chip subsidiary • Aug. 2021, 2nd generation XPU
	ByteDance 字节跳动	• Mar. 2021, developing AI and server chips in-house
	Tencent	• Jul. 2021, developing special purpose processors in-house
	美团 Meituan	• Jul. 2021, set up chip subsidiaries • Aug. 2021, invested in chip IDM
Telecom and Network Equipment	HUAWEI	• As of Aug. 2021, Hubble Technology invested in 44 companies in semiconductor supply chain
	H3C	• Oct. 2020, launched first switch chip • Apr. 2021, launched first network processor

Source: SIA analysis

China Chip Designers

SEMICONDUCTOR INDUSTRY ASSOCIATION

Chinese Advanced Logic Chip Tapeouts [6], 2020-2021

Alibaba
- October 2021
- 5nm server CPU
- 7nm could AI chip

Baidu
- August 2021
- 7nm cloud server chip

H3C
- April 2021
- 7nm network accelerator

SiEngine
- November 2021
- 7nm autonomous driving SoC

ZTE
- October 2020
- 5nm 5G base station processor

Iluvatar CorX
- March 2021
- 7nm GPU

Horizon Robotics
- August 2021
- 7nm L4 self-driving processor

Cambricon
- January 2021
- 7nm AI accelerator chip

Source: SIA analysis

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Wafer Scale

Wafer Scale

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2019

Cerebras Wafer Scale Integration

400,000 cores!

15kW

Startup Cerebras will describe at Hot Chips the world's largest semiconductor device, a 16nm wafer-sized processor array that aims to unseat Nvidia's GPUs dominance in training neural networks. The whopping 46,225mm2 die consumes 15kW, packs 400,000 cores, and is running in a handful of systems with at least one unnamed customer.

...

The Cerebras device packs 84 tiles in a 7x12 array. Each includes about 4,800 cores geared for AI's sparse linear algebra with 48 KBytes SRAM each, their sole memory source.

The Cerebras device packs 84 tiles in a 7x12 array. Each includes about 4,800 cores geared for AI's sparse linear algebra with 48 KBytes SRAM each.

Cerebras WSE 2

Wafer Scale Engine

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--Cerebras Systems

Cerebras Wafer Scale Engine 2

Shift to 7-nanometer process boosts the second-generation chip's transistor count to a mind boggling 2.6-trillion

Almost from the moment Cerebras Systems announced a computer based on the largest single computer chip ever built, the Silicon Valley startup declared its intentions to build an even heftier processor. Today, the company announced that its next-gen chip, the Wafer Scale Engine 2 (WSE 2), will be available in the 3rd quarter of this year. WSE 2 is just as big physically as its predecessor, but it has enormously increased amounts of, well, everything.

...

As big as possible, meaning the size of an entire wafer of silicon (with the round bits cut off), or 46,225 square millimeters.

	WSE 2	WSE	Nvidia A100
Size	46,255 mm^2	46,255 mm^2	826 mm^2
Transistors	2.6 trillion	1.2 trillion	54.2 billion
Cores	850,000	400,000	7,344
On-chip memory	40 gigabytes	18 GB	40 megabytes
Memory bandwidth	20 petabytes/s	9 PB/s	155 GB/s
Fabric bandwidth	220 petabits/s	100 Pb/s	600 gigabytes/s
Fabrication process	7 nm	16 nm	7 nm

UCLA Wafer Scale

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UCLA Samueli School of Engineering

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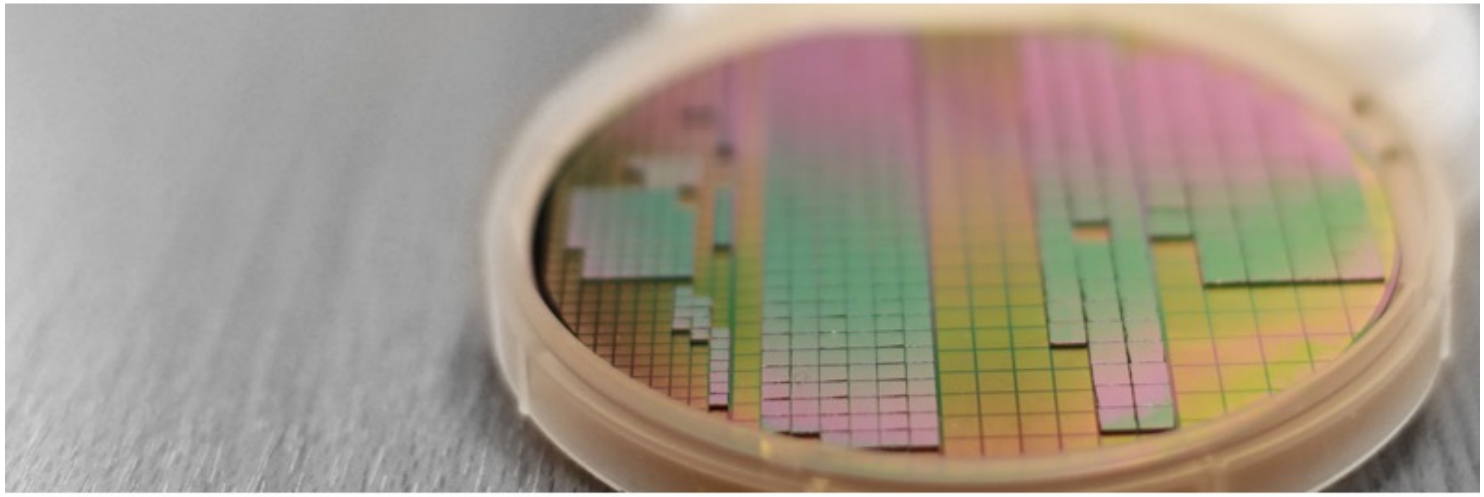
Flextrate

Chiplets?

At Cal State Los Angeles, physiology and neuroscience researcher Selvan Joseph is one such innovator. He's using the Flextrate platform developed at CHIPS to design sensors that can track the physical movements and muscle activity of patients with movement disorders, or those recovering from spinal cord injuries. Flextrate allows him to put these sensors in a small flexible patch that patients can wear unobtrusively on their skin.

"This technology is definitely a game-changer in that you can create devices with more flexibility, pliability and portability," Joseph said. "We can send this device home with our patients and then remote collect data in real time in their day-to-day lives."



Faster Communication

While these platforms have the potential to revolutionize data centers, and consumer and medical electronics, the CHIPS team is also working on ways to make supercomputers and artificial intelligence machines more powerful in the wake of Moore's Law.